Enhancing the Robustness of System on FPGA by Routing Isolation

POSTER: Enhancing the Robustness of System on FPGA by Routing Isolation

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ABSTRACT

Due to their high performance and flexibility, FPGAs have become an attractive solution for space applications. However, SRAM-based FPGAs are particularly sensitive to radiation-induced Single Event Effects that may lead to configuration memory corruption. We propose a methodology for enhancing the reliability of redundant design implemented on FPGAs. Statically analyzing the implementation of the circuit to identify and reduce the single points of failure of redundant systems, we can increase the system's robustness by controlling the placement phase.

CCS CONCEPTS

•Hardware~Robustness~Hardware reliability~Circuit hardening

KEYWORDS

SEU, Fault injection, Reliability, FPGA, TMR

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1 Introduction

https://doi.org/10.1145/3649153.3653000Field Programmable Gate Arrays (FPGA) are attracting interest in different fields, including the space industry. However, space is a hostile environment for electronic devices. Cosmic radiation is the source of single-event effects (SEE) that may lead to malfunctions [1][2]. Particularly for SRAM-based reconfigurable hardware platforms, a Single Event Upset (SEU) can corrupt the configuration memory (CRAM), altering the programmed circuit. To address this problem, Triple Module Redundancy (TMR) is a standard solution [3][4] adopted to mitigate radiation-induced errors. However, if an SEU-induced fault is the source of a malfunction in different TMR domains, it can nullify the TMR mechanism. Such a problem is known as Cross-Domain Error or Common-Mode Failure.

This paper proposes a methodology to identify single points of failure in the programmable routing of TMR-based designs. Proposing a dedicated strategy to minimize such an effect, we demonstrate how to increase the overall reliability of a redundant system. A case study is presented for UltraScale+ architectures by AMD, but the approach applies to any FPGA architecture.

2 Methodology

The routing infrastructure of FPGAs is based on Programmable Interconnect Point (PIP). PIPs are programmable routing segments. As a result of a SEU in CRAM, PIPs may create involuntary communication between two parts of the circuit (Figure 1). Such a mechanism is a well-known source of malfunctions in the routing infrastructure [5]. We focus our methodology on identifying and reducing the single point of failure generated in the programmable routing.

To detect all single points of failure that affect the design, a static analysis phase is performed with the assistance of the PyXEL framework [6], relying on gathering implementation and architectural data about the design and specific FPGA, respectively. Two pieces of information are needed:

1. PIPs and wires were used in the design.
2. PIPs and wires that are available in the device fabric.

Using such information, it is possible to find PIPs that can be a source of common-mode failures. In particular, we detect a couple of driven PIPs (i.e., used ones) that can be short-circuited by a third PIP that is currently disabled. We define

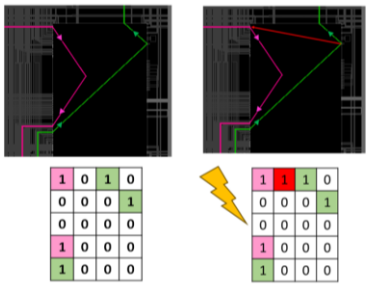

Fig. 1: A conceptual representation of how a SEU in CRAM can modify FPGA routing.

those PIPs as critical PIPs. This procedure is applied to a domain of the TMR, discovering intra-domain critical PIPs. Then, all the cross-domain critical PIPs are detected by the difference between the whole set of critical PIPs in the design and the intra-domain one.

Following the identification of critical PIPs, it was possible to remove them from the design with the help of user-defined constraints that allow the manual placement of designated components, such as the TMR modules, within user-defined zones inside the FPGA.

By employing this methodology, it became feasible to isolate specific domains within the design and subsequently analyze the improvements achieved by eliminating cross-domain PIPs. This approach allowed for a comprehensive comparison of the design's performance, highlighting the impact of strategically placing components and optimizing the configuration for enhanced fault tolerance.

3 Experimental Results

A case study is proposed. The proposed approach is applied to improve the reliability of a TMR version of the NEORV32 [7] RISC-V processor. The Whetstone benchmark has been selected as the software application. Whetstone consists of a set of mathematical routines, including iterations of floating-point arithmetic, trigonometric functions, conditional statements, and array manipulations.

A fault injection platform was developed to emulate errors affecting the configuration memory, simulating the effect a SEU would have had. The output of the software benchmark after each emulated fault is utilized to detect errors in the computation by comparing the output of the faulty design with the expected results.

Two solutions for the implementation phase of the same design are evaluated. The first is the baseline version provided by the vendor tool, while the second one is generated with the proposed methodology for minimizing the number of critical PIPs. The results of the static analysis phase on the two solutions for the implementation phase are reported in Table I. For each version, a fault injection campaign of 3,000 experiments is performed. During each experiment, SEUs are accumulated in CRAM to evaluate the robustness of the system against SEUs. Comparing the outcome in terms of the reliability of the two systems, reported in Figure 3, it is possible to notice an improvement of reliability that reaches up to 4% in the accumulation range of 75-150. The gain is highlighted in Figure 2. Please notice that such improvement is the result of a fault-tailored place and route phase, so no resource overhead is involved.

Table I. Static Analysis Results

Design	All PIPs [#]	Cross-domain PIPs [#]
Baseline	260,019	1,103
Isolated Domains	254,131	1

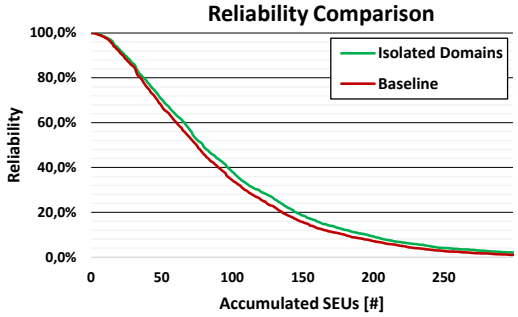

Fig. 2: Reliability variation by accumulated SEUs in the baseline circuit and the version with isolated domains.

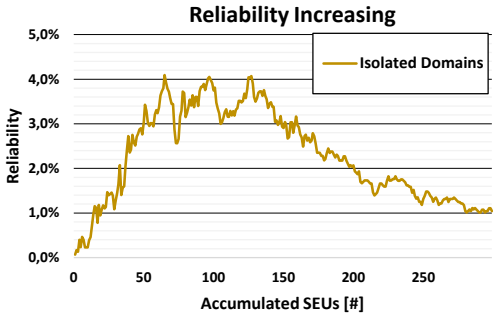

Fig. 3: Reliability improvement using the proposed approach.

4 Conclusion

This paper shows how, by forcing domain separation of TMR designs, it is possible to increase the overall reliability against SEUs with the elimination of single points of failures.

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