Assessment of RISC-V Processor Suitability for Satellite Applications

Assessment of RISC-V Processor Suitability for Satellite Applications

Invited Paper

Eleonora Vacca, Giorgio Cora, Sarah Azimi, Luca Sterpone
Department of Control and Computer Engineering (DAUIN)
Politecnico di Torino, Turin, Italy
eleonora.vacca@polito.it, giorgio.cora@polito.it, sarah.azimi@polito.it, luca.sterpone@polito.it

ABSTRACT

This research addresses the challenges faced by space applications due to high-energy ionizing particles in the space environment, particularly when using commercial Off-The-Shelf (COTS) components like Field Programmable Gate Arrays (FPGAs) and soft-core processors like RISC-V. Our study introduces a methodology for evaluating the reliability of a state-of-the-art RISC-V processor intended for space missions, establishing a connection between space conditions, Single Event Upset (SEU) fault estimation, and emulation. Focusing on the space environment around a telecommunication satellite, we analyze particle fluxes and their impact on SRAM-based FPGAs using proton radiation test data. By integrating this data, we estimate the SEU rate per mission day caused by the specific radiation environment. Subsequently, we assess the suitability of the NEORV32 processor for operation in such an environment by implementing it in the target FPGA and conducting SEU emulation through fault injection campaigns. Our primary goal is to determine the design mean time to failure within the space environment where the processor is expected to function, a critical metric for implementing effective mitigation strategies for space mission designs. The obtained results, covering worst-case scenarios, suggest that RISC-V-based architectures prove resilient and adaptable for successful deployment in space missions.

CCS CONCEPTS

Hardware ~ Robustness ~ Safety critical systems

KEYWORDS

FPGA, Radiation Effects, RISC-V, Fault Injection, GEO.

ACM Reference format:

Eleonora Vacca, Giorgio Cora, Sarah Azimi, Luca Sterpone. 2024. Assessment of RISC-V Processor Suitability for Satellite Applications. In *Proceedings of 21st ACM International Conference on Computing Frontiers Workshops and Special Sessions (CF'24 Companion), May 7-9,2024, Ischia, Italy. ACM, New York, NY, USA, 6 pages,*
https://doi.org/10.1145/3637543.3652978

CF '24 Companion, May 7–9, 2024, Ischia, Italy

ACM ISBN 979-8-4007-0492-5/24/05.
https://doi.org/10.1145/3637543.3652978

1 Introduction

Space applications require devices characterized by high computational capabilities as well as reliable and dependable architectures. Indeed, the space environment is marked by high-energy ionizing particles that interact with matter, inducing charge deposition and altering the proper functioning of electronic devices. A single radiation-induced fault in a device may propagate throughout the entire system, compromising mission success. Therefore, one of the crucial phases in space mission design is the characterization of the space environment[1]. This involves defining the radiation source and the effects related to the space environment surrounding the satellite throughout the mission. Specifically, the radiation scenario changes depending on the proximity to the Sun and Earth [2]. Consequently, both the type of particles and the induced effects on electronic components vary. Understanding these factors is crucial in defining and adopting appropriate mitigation methodologies, aligned with the mission's objectives and tailored to the specific context in which it is to be carried out.

The challenges posed by the space environment are further accentuated by the frequent use of Commercial Off-The-Shelf (COTS) components rather than radiation-hardened ones, primarily due to cost-effectiveness. In this scenario, the current trend in space missions is to employ Field Programmable Gate Arrays (FPGA) devices[3][4]. Despite not being radiation-hardened, their online reconfigurability, flexibility, and performance enable the implementation of custom design solutions and mitigations tailored for the specific mission without increasing the area or cost. This is crucial for meeting mission specifications such as budget constraints, spacecraft dimensions, and weight.

Along with FPGA, the adoption of soft-core processors[5] for space applications is growing [6]. The primary reason for choosing an FPGA for the implementation of processors and, consequently, embedded systems, is its capability to finely balance between hardware and software. This balance maximizes system efficiency and performance while ensuring considerable flexibility. In addition to this, implementing an embedded system on an FPGA offers several advantages over conventional microprocessors, with the most significant ones being the customization and the reduction in the number of components. In this scenario, the introduction of RISC-V allowed for a fast and efficient improvement of space-oriented systems [7]. Its Instruction Set Architecture (ISA), characterized by an open-source and extendible nature, allowed

engineers and developers to implement different kinds of architecture, each one of them characterized by specific features depending on the field of applications. However, when soft-core processors are implemented on SRAM-based FPGA ensuring reliability is the major concern [8]. Indeed, SRAM-based FPGA configuration memory (CRAM) is susceptible to Single Event Upsets (SEU)[9], namely bitflip in the memory cells. Since CRAM content defines the circuit implementation on the FPGA device, any radiation-induced content alteration may provoke structural fault in the processor Datapath, altering its functionality. Hence, adopting mitigation techniques such as Triple Modular Redundancy (TMR) to improve the design reliability is a must [10].

In this paper, we propose a reliability assessment of a cutting-edge RISCV processor when deployed in a space mission. To address realistic scenarios and present an effective case study, we establish a correlation between space environment specifications and an SEU fault emulation campaign. Specifically, our focus is on a space mission with a geostationary orbit (GEO), encompassing a telecommunication satellite scenario. To characterize the radiation source and its effects, we utilize the OMERE tool [11] to extract high-energy particle fluxes affecting the mission environment. We then combine this information with ground radiation test data available for the target FPGA device to estimate the SEU rate per mission day. Then, we implement a TMR version of the NEORV32 RISC-V [12] processor and execute SEU emulations through a fault injection campaign in the device's CRAM. Finally, we correlate the SEU rate estimation with the fault injection results to assess the design mean time to failure. This outcome is crucial for designing mitigation strategies tailored to the specific processor and application scenario.

2 Background on Radiation Effects in the GEO Environment

The space environment is defined by the presence of high-energy ionizing particles originating from diverse sources. The primary contributors include energetic particles emitted by the Sun and galactic cosmic rays (GCRs)[13] originating from beyond our solar system. GCRs predominantly consist of high-energy protons (about 85% of the composition), alpha particles (approximately 14%), and other high-energy nuclei. In contrast, solar energetic particles primarily consist of protons accelerated to high energy levels by solar flares and coronal mass ejections. The contribution of these radiation sources is dynamic [14], influenced by solar activity and proximity to the Sun, with solar activity following approximately 11-year cycles alternating between maximum and minimum phases, as illustrated in Figure 1. During a solar maximum, solar activity is intense enough to shield GCRs originating from outside the solar system, resulting in a higher contribution from solar protons. Conversely, during solar minimum phases, the contribution from GCRs tends to be more significant. Additionally, the magnetic field of celestial bodies acts as a shield against radiation sources [15], so the interplanetary environment is different from the space environment close to Earth. The close Earth radiation environment is characterized by the Van Allen radiation belts[16], which are a zone of energetic charged particles, most of which originate from the solar wind, that are captured by Earth's magnetic field.

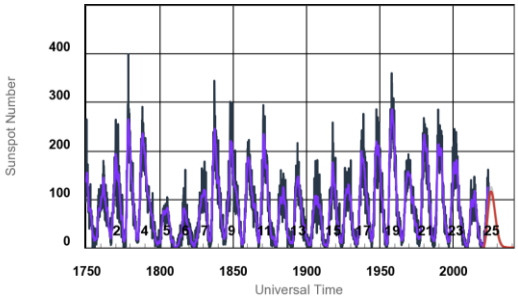

Figure 1. Solar cycle data trends extracted from the National Oceanic and Atmospheric Administration [18].

When considering satellite orbits, the environment surrounding Earth is divided into three regions[17]. Low Earth Orbit (LEO) extending from 160 km to 1000 km, Geostationary Earth Orbit GEO) at an altitude of 35,786 km, and Medium Earth Orbit (MEO), comprising all the satellites orbiting between LEO and GEO. GEO environment poses distinct challenges since it is almost fully exposed to GCRs[19], where the energy distribution of cosmic rays peaks at 300 mega electronvolts [MeV], with observations of ultra-high-energy particles up to GeV. In GEO, the trapped particle fluxes are low, mainly consisting of energetic electrons, while the trapped protons are below the energy levels that initiate nuclear events in materials. From an electronic device perspective, GCRs contribute to Single-Event Effects (SEEs)[20], while trapped electrons induce TID[21]. SEEs refer to transient malfunctions or changes in the behavior of electronic devices caused by a single energetic particle strike. Despite satellite shielding with aluminum, these particles can penetrate and potentially lead to mission failure. Different device types exhibit varying SEEs, emphasizing the critical role of the device function in the analysis, e.g. memories exhibit different effects than power converters for the same energetic particle. Therefore, a comprehensive radiation analysis requires merging of radiation environment characterization with the satellite payload and onboard electronics, to effectively anticipate and mitigate any radiation-induced effect. In the following, we are going to assume a radiation environment in GEO, evaluating variations induced by solar maximum and solar minimum conditions, and employing the environment characterization to estimate the SEU sensitivity of a satellite onboard processor.

3 Case of Study: The NEORV32

Soft-processor cores integrated into FPGAs are renowned for their efficiency in addressing the needs of space applications. The introduction of the RISC-V ISA-based architecture has notably enhanced the positive aspects brought by this solution. Its open-source and modular nature lead to the development of various architectures, each one of them with specific characteristics to perfectly fit the device's application field. Indeed, RISC-V-based architectures are reshaping the space market, especially in the European community where an effort is underway to effectively integrate RISC-V processors into space missions[7]. This has led the scientific community to create custom RISC-V architectures. However, determining the practicality of using a RISC-V core is not straightforward. Different architectures have varying

sensitivities, and the radiation environment related to each space mission affects processors differently. Among the available RISCV architectures, the NEORV32[12] provides a tiny, highly customizable RISC-based solution. It supports multiple ISA extensions and numerous optional modules to expand its computational capabilities and enhance performance.

Given this, we propose an evaluation that focuses on the minimal still performant processor configuration. This includes enabling the implementation of a UART interface module, serving as the primary serial communication method with the Host PC. In terms of computational resources, we implemented the Floating-Point Unit (FPU) using the ZFINX ISA extension. Additionally, we have also enabled the Mul/Div unit, further extending the ISA with the M instruction extension. Finally, the processor architecture has been equipped with the BOOTDLROM, and internal ROM memory to execute the bootloader during the processor setup phase. When COT components are used in space applications redundancy-based mitigation methodologies are adopted. Therefore, to cover a realistic case of use in a radiation-prone environment, we hardened by design the processor by adopting the TMR)mitigation strategy. This involved triplicating the main core and adding a majority voter at the processor output. The overall system implementation schematic is shown in Figure 2. Additional components have been integrated into the system alongside the three NEORV32 cores to facilitate the fault emulation process as we are going to explain in the following section.

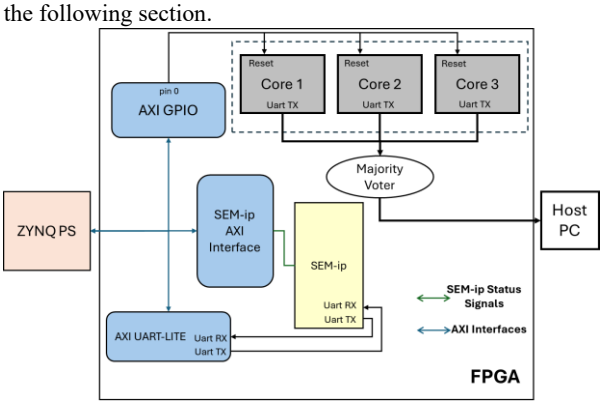

Figure 2. Schematic view of the NEORV32 in TMR.

4 Radiation Environment Characterization

A crucial aspect of studying the feasibility of a space mission is the characterization of the radiation environment. Indeed, this environment has a significant impact on the selection of onboard electronics, since a component that is suitable for LEO applications, for example, may not meet the radiation tolerance limits specified for interplanetary missions. For this reason, radiation experts focus on characterizing the environment in terms of radiation sources and effects, assisting in component selection. To achieve this, various characterization tools exist, unified by physical models of particles and their impact on matter (especially Silicon). The initial step is the mission parameters definition. Specifically, the orbit types such as geosynchronous, LEO, interplanetary, etc. The orbit details, in terms of distances from the Sun in the case of interplanetary missions, apogee, perigee, inclination, etc. in other cases. Mission duration (days, months, or years) and launch date. All these parameters, placing the spacecraft in space and time (in terms of solar activity), define the radiation sources. Once the mission overview is defined, the tools generate an estimation of the high-energy particle fluxes that the satellite may encounter. Specifically, GCRs, Solar protons, and trapped particles (for missions near planets). With the obtained fluxes and available information on the satellite's geometry or component sensitivity (as we will explain in the next sections), it is possible to quantify the effects induced by this particle and thus evaluate what may happen during the mission. Typically, the evaluated effects include the estimation of SEUs and absorbed radiation dose. In our work, we propose a flow to evaluate the SEU's effect by combining the environmental characterization, proton radiation test data, and fault injection campaign.

5 Reliability Analysis Platform

Various methodologies are available to emulate the space environment and evaluate the behavior of devices when exposed to its effects. Among these, radiation tests stand out as the most accurate ones[22][23], being able to replicate both the source of the faults and their effects on the devices. It consists of exposing the device to an accelerated particle beam. However, this methodology is extremely expensive and, given the limited number of facilities providing this service, is also characterized by long waiting lists which make it not accessible for everyone.

To overcome this limitation, fault emulation is typically adopted consisting of emulating directly the fault effect rather than the source. Faul emulation can be applied at different abstraction levels, targeting either the hardware or the software [24].

When designs are implemented on SRAM-based FPGA, radiation-induced effects typically relate to the device CRAM[10]. Indeed, the content of this memory is used to configure the programmable logic and the interconnection resources to implement the target circuit. Therefore, if a charged particle strikes a memory cell provoking a change in its status, namely an upset, it may induce an alternation in the implemented circuit, which will not behave as expected.

This radiation-induced effect can be easily emulated by corrupting the bitstream file to be loaded in the CRAM[25]. Indeed, given the criticality that an upset poses to the design, FPGA developers themselves have designed modules that can be integrated into the design to emulate this failure scenario. This is the case of the SEM-IP[26] module from AMD/Xilinx, which was implemented in our design alongside the NEORV32 architecture to perform fault emulation. The SEM-IP module enables configuration memory corruption through bit-flips, while also performing single or multiple error correction. Being instantiated inside the FPGA, it offers direct interaction with the CRAM at runtime, speeding up the experimental evaluation. The AXI GPIO, shown in Figure 2, is used to drive the reset signal of each soft processor after each fault injection. Moreover, two additional AXI interfaces are required. The AXI UARTLITE and a dedicated AXI interface for the SEM-IP. The former one allowed the ZYNQ PS to gather information from the SEM-IP and display it without requiring an additional external device. The latter one is an interface designed specifically for the SEM-IP, granting access and control to its internal registers.

The entire injection procedure is automatized through a Python script whose purpose is to communicate with the FPGA, send injection and error correction commands, and reset the NEORV32 through the AXI components. The proposed platform can perform single or multiple fault injections, depending on the goal of the experiment. Moreover, it can be easily adapted for different designs. While radiation tests and fault emulation differ, it's essential to recognize that these procedures can be both conducted and mutually complement each other. As highlighted in the following section, result analysis and consideration derived from each methodology individually can be integrated to perform a radiation sensitivity assessment of the design under evaluation.

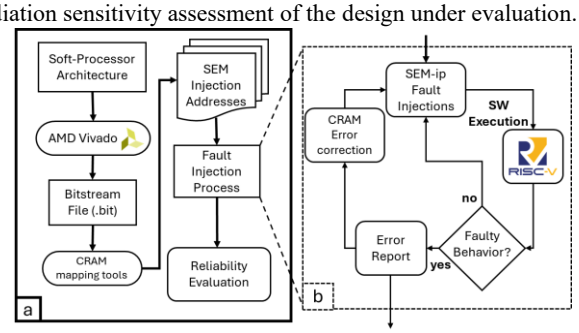

Figure 3. Flow chart of the implemented SEU emulation platform.

6 Experimental Analysis

To characterize the NEORV32 soft-core processor in the context of its application in a GEO environment, a multi-step approach has been adopted:

- Mission Definition: using the OMERE radiation environment tool, the space mission and its environment are defined to extract radiation sources and their effects on the target FPGA device. This analysis is independent of the implemented circuit.
- SEU emulation: this step involves fault injection with accumulation to assess the implemented circuit's robustness, specifically the TMR NEORV32, concerning SEUs. The objective is to gather statistics on the number of SEUs that the system can tolerate before failure.
- NEORV32 Radiation Sensitivity Estimation: the outcomes from steps (1) and (2) are combined to characterize the NEORV32 concerning the specific space mission under analysis. This combination is crucial for estimating the mean time to failure in terms of mission days, providing insights into the processor's reliability and performance in the GEO environment.

The NEORV32 has been implemented in TMR fashion in the Zynq XC7Z020 SoC. The SoC contains dual ARM® Cortex®-A9 MPCore ™ with CoreSight ™ and 28 nm high-k metal gate CMOS programmable Xilinx Artix7 FPGA family logic, with 85k logic cells. Implementation details in terms of resource usage and frequency are provided in Table 1.

6.1 Mission Definition

Analyzing radiation sensitivity involves defining key space mission parameters, such as satellite trajectory, launch details, and mission duration. These factors delineate the satellite's operational

Table 1. NEORV32 implementation details.

	FPGA Resource Utilization [%]				Power [W]
	LUTs	FFs	BRAMs	DSPs	
NEORV32 TMR	88.13	81.32	96.43	100.00	0.098

environment throughout its mission. Various tools are available for such characterizations, and one notable option is OMERE, a freeware specifically designed for assessing space environment and radiation effects on electronic devices. The tool supports numerous environment models, including the standard ECSS-10-04 models, compliant for effective space mission characterization. Considering the target GEO environment, we adopted as a case study the orbit data related to EUTELSAT-10B[27], one of the latest European telecommunication satellites launched on November 23, 2022, currently operative. Orbits parameters are reported in Table 2. As for mission length, we target 1 year duration. Given the same mission parameters, we considered two different radiation environments, related to solar activity, by selecting two different launch windows. Specifically, we considered a launch in 2024, covering solar maximum, and then a launch date in 2029, hence covering 1-year mission in solar minimum. The energetic particle fluxes for the two scenarios are reported in Table 3. Once the particle fluxes are obtained, we can use the data to estimate the SEU rate. Since this aspect is strongly technology-dependent, we need to provide the tool with the target FPGA CRAM SEU cross-section per bit. The CRAM cross-section has been obtained from a proton radiation test previously conducted on the Zynq7020 SoC at the PIF facility in Switzerland[28]. Combining the device sensitivity with the expected mission fluxes, the tool provides the SEU rate per bit per day affecting the CRAM. Since the cross-section data relates to a proton radiation test, the SEE estimation refers to the proton's contribution, considering protons from solar events, trapped protons of the outer Van Allen Belt, and the protons included in the GCRs.

Table 2. EUTELSAT 10 satellite trajectory parameters

	Perigee [km]	Apogee [km]	Inclination [°]	Semi.-major axis [km]	Period [m]
EUTELSAT	35,777.9	35,811.1	0.052	42,165	1,436.1

Table 3 GCRs proton fluxes related to EUTELSAT orbit.

Energy [MeV]	Cosmic Rays Proton Differential flux [cm-2.s-1.MeV-1]	
	Sun Maximum	Sun Minimum
1.0	2.18e-07	1.95e-06
10.0	1.83e-05	1.26e-04
100.0	4.06e-04	1.66e-03
150.0	5.71e-04	2.08e-03
200.0	6.98e-04	2.34e-03
1000.0	8.72e-04	1.55e-03
10000.0	2.69e-05	2.97e-05

Table 4. SEE rate per bit per mission day for different solar activity.

SEE rate [bit/day]	Sun Maximum	Sun Minimum
Trapped Proton	0.00e+00	0.00e+00
Solar Proton	3.31e-08	1.38e-08
Cosmic Rays (Protons)	8.13e-10	1.39e-09
Total	3.39e-08	1.52e-08

As explained in Section 2, GCRs are composed of 85% of protons. Hence, we are covering the effects induced by the most prevalent

radiation source in space. For the SEE estimation, the magnetic cut-off induced by Earth has been enabled since emulating the environment faced by a GEO satellite. The SEE rate for solar maximum and solar minimum are reported in Table 4.

Once we have the SEU estimation per single bit per day, we need to quantify the effective number of upsets potentially affecting the NEORV32 during one day of the mission. This is achieved by multiplying the single bit rate, by the number of CRAM bits effectively used to implement the design. Specifically, 7,065,292 bits are programmed in the CRAM for implementing the NEORV32 in TMR fashion, corresponding to 21% of CRAM bits. The outcome of this multiplication provides an estimation of 0.24 SEU/design/day when the satellite operates during the maximum solar activity and 0.107 SEU/design/day during the solar minimum period. If we multiply the SEU/bit/day by the overall number of bits composing the CRAM, we will obtain the estimated SEU rate per device. However, those upsets are not affecting any memory cell used by the NEORV32, hence not provoking any effect in the implemented design. The SEU/device/day estimation will be used in the following section to assess the sensitivity of the NEORV32 concerning the target radiation environment.

6.2 Fault Injection with Accumulation

Our proposed work aims to assess the NEORV32's robustness in a space mission environment by simulating radiation-induced faults. Typically, fault injection campaigns with accumulation are utilized to estimate the design's mean time to failure (MTTF). In contrast to single-fault injection campaigns, where only one SEU is emulated in the CRAM per run, and the system's impact is assessed, accumulation involves emulating consecutive SEUs in the CRAM until the TMR failure occurs. This methodology allows us to estimate the number of SEUs the design can tolerate before compromising its integrity, providing valuable insights for fine-tuning the memory scrubbing frequency.

Different benchmarks can be chosen depending on the processor's application scenario, spanning from those that stress the control unit or the ALU to those that thoroughly assess memory access. In our analysis, we selected four distinct benchmarks. *Whetstone,* a performance benchmark executing arithmetic, floating-point, and logic operations. The *Linpack* consists of linear equations with large matrices of floating-point numbers. The *Dhrystone* is a performance benchmark based on integer arithmetic, string operations, and memory accesses. *Matmul,* performing matrix multiplication between large matrices of integers.

The overall experimental analysis consists of 1000 runs. For each run, multiple SEUs were injected consecutively until a failure in the NEORV32 was observed. To focus on the effect of SEUs on the design, the CRAM injection area has been constrained to the area related to the implemented design. This has been achieved in two separate steps. First, during the FPGA design flow, we acted on the floor planning before the final place&route phase. This consisted of defining pBlock regions in the FPGA area onto which confining the design's modules. In this way, we can control both resource assignment and module locations, which facilitates the SEUs injection process. Since SEM-IP requires CRAM memory addresses to inject upsets, we need to extract such information for each of the pBlock regions defined. This can be accomplished by employing specific CRAM mapping tools, such as the PyXEL[25] toolkit that starting from the bitstream file can identify the bits related to each pBlocks region and convert them into memory addresses, ultimately passed to the SEM-IP during the fault injection process. The outcomes of the injection campaign are highlighted in Figure 4, showcasing the cumulative number of SEUs for each run. As can be seen, in most of the cases, the TMR processor was able to tolerate more than 40 SEUs before failing. These results validate the effectiveness of the TMR mitigation techniques, increasing the processor fault tolerance. Indeed, as mentioned before we have exclusively targeted CRAM bits used to implement the processor, hence effectively impacting its Datapath. Still, the TMR approach is capable of masking such an effect, guaranteeing system-correct behavior. Another important aspect of the accumulated injection result is the nature of the SEU-induced errors. Specifically, the observed errors have been classified in *HALT*, when the SEUs caused the processor to hang. *SDC*, when one or more characters in the logfile are non-numeric, and *Wrong Value* when the computed result is different from the expected one. The occurrence of the errors is provided in Table 5. The *HALT* type is the most common one. This means that when SEUs are affecting any kind of logic apart from the control system, the TMR efficiently masks the fault effects. Additionally, from Figure 4, it can be noticed that benchmark applications share a similar failure trend. Specifically, there's a common failure pattern in *Whetstone* and *Linpack*, as well as in *Dhrystone* and *Matmul*. The first pair's similarity is easy to understand since both benchmarks involve floating-point operations. In contrast, *Matmul* and *Dhrystone* show similarity because matrix multiplications require spatial and temporal related memory access for loading input data, handling intermediate results, and storing final results. So, even if stressing memory access isn't *Matmul*'s main goal like it is for *Dhrystone*, it's still the main reason for their shared behavior.

In evaluating the MTTF, we focus on the average failure rate linked to the *HALT* failure type. This type not only constitutes 99% of

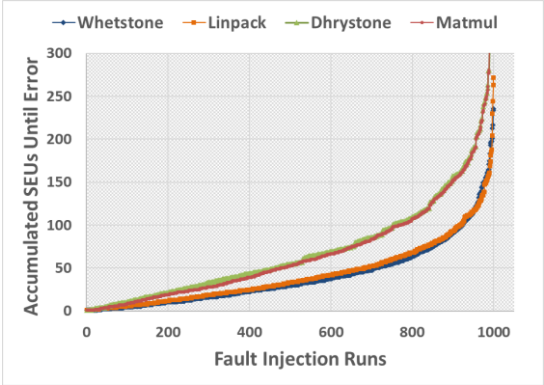

Figure 4. Accumulated fault injection campaign results for 1000 runs.

Table 5. System faulty behavior classification.

Fault Type	Whetstone	Linpack	Dhrystone	Matmul
Halt [%]	956	956	990	923
SDC [%]	12	2	6	61
Wrong Value [%]	32	42	4	16

failures but also stands out as the most severe, requiring a processor reset and thereby reducing the system's overall availability. For the two pairs of application benchmarks, the average accumulated SEUs inducing a system halt are 41 SEUs for the floating-point (FP)-based benchmarks, while the system can tolerate up to 70 SEUs when executing memory-intensive benchmarks.

The MTTF is obtained by dividing the accumulated SEUs before failure by the mission SEU/design/day estimation obtained in Section 6.1. The evaluation has been performed by covering the two different solar activity conditions, for the two types of benchmark applications. MTTF estimation results are reported in Table 6. As can be noticed, the processor MTTF strongly depends on the executed workload. Considering for example the worst-case scenario of operating in solar maximum. Given the same SEUs rate affecting the processor Datapath, when executing FP-based programs the processor requires a reboot almost twice per year, while surviving for almost 0.8y in the other case. Moreover, the reported cases relate to conservative estimation, since we assumed no periodic memory scrubbing operation that could increase the MTTF and considered the device fully exposed to the environment, while satellite geometry, material, and additional shielding layer attenuate the exposure factor, increasing the MTTF.

Given this, the TMR system in NEORV32 demonstrates strong tolerance capabilities, making it a viable and effective solution for integrating RISC-V-based architecture into satellite applications.

Table 6. MTTF estimation for different benchmark and solar conditions.

	FP-based benchmarks		Memory-intensive benchmarks	
SEUs before Failures	40		70	
	Sun max	Sun min	Sun max	Sun min
SEUs/design/day	0.24	0.107	0.24	0.107
MTTF (days)	166.66	373.83	291.66	654.20
MMTF(years)	0.45	1.02	0.80	1.80

7 Conclusions

In this study, we presented a multi-step approach to assess the viability of RISC-V-based architecture for satellite applications. Beginning with defining the radiation environment for GEO applications, we analyzed radiation sources and effects on the FPGA device housing the NEORV32 processor. Combining proton radiation test data with environmental characteristics, we calculated the SEU/device/day. Subsequently, we emulated SEU effects through CRAM fault injection to determine the design's tolerance to SEUs before failure. Integrating these metrics, we evaluated the system's mean time to failure in the GEO environment. Our findings, encompassing worst-case scenarios, suggest that RISC-V-based architectures prove to be robust and flexible solutions for effective space mission deployments.

REFERENCES

[1] S. Dagras et al., "Evaluation of spacecraft materials behavior to JUICE environment (Synergistic effect of radiations and cryogenic temperature)," 17th European Conference on Radiation and Its Effects on Components and Systems (RADECS), 2017, pp. 1-6, doi: 10.1109/RADECS.2017.8696170

[2] Steven A. Walker et al., "Radiation Exposure Analyses Supporting the Development of Solar Particle Event Shielding Technologies", 43rd International Conference on Environmental Systems, 2013.

[3] C. H. Le et al., "Challenges in FPGA Design for Complex, High-Performance Space Applications," 2023 IEEE Space Computing Conference (SCC), Pasadena, CA, USA, 2023, pp. 45-50, doi: 10.1109/SCC57168.2023.00016.

[4] E. Vacca et al., "Analyzing the SEU-induced Error Propagation in Systolic Array on SRAM-based FPGA", in IEEE European Conference on Radiation and its Effects on Components and Systems (RADECS), Toulouse, France, 2023.

[5] P. Yiannacouras et al., "Exploration and Customization of FPGA-Based Soft Processors," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 26, no. 2, pp. 266-277, Feb. 2007.

[6] D. L. Bekker et al., "Performance Analysis of Standalone and In-Fpga LEON3 Processors for Use in Deep Space Missions," 2019 IEEE Aerospace Conference, Big Sky, MT, USA, 2019, pp. 1-17, doi: 10.1109/AERO.2019.8742194.

[7] G. Furano et al., "A European Roadmap to Leverage RISC-V in Space Applications," *2022 IEEE Aerospace Conference (AERO)*, Big Sky, MT, USA, 2022, pp. 1-7, doi: 10.1109/AERO53065.2022.9843361.

[8] T. Li, H. Yang, H. Zhao, N. Wang, Y. Wei and Y. Jia, "Investigation into SEU Effects and Hardening Strategies in SRAM Based FPGA," *2017 17th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Geneva, Switzerland, 2017, pp. 1-5.

[9] P. Maillard et al.,"Single Event Latchup (SEL) and Single Event Upset (SEU) Evaluation of Xilinx 7nm Versal™ ACAP programmable logic (PL)," IEEE Radiation Effects Data Workshop (REDW), 2021, pp. 1-6.

[10] E. Vacca et al., "Failure rate analysis of radiation tolerant design techniques on SRAM-based FPGAs", Microelectronics Reliability, Volume 138, 2022, 114778, ISSN 0026-2714, DOI: 10.1016/j.microrel.2022.114778.

[11] N. Sukhaseum et al., "Statistical estimation of uncertainty for single event effect rate in OMERE,"12th European Conference on Radiation and Its Effects on Components and Systems, 2011, pp. 401-407.

[12] S. Nolting and Contributors, "The NEORV32 RISC-V Processor." Zenodo, Aug. 18, 2023. doi: 10.5281/zenodo.8260609

[13] Simpson, J.A. "Introduction to the Galactic Cosmic Radiation", Composition and Origin of Cosmic Rays. NATO ASI Series, vol 107. Springer, Dordrecht.

[14] Barth, J.L., "Space and Atmospheric Environments: From Low Earth Orbits to Deep Space". Protection of Materials and Structures from Space Environment, Space Technology Proceedings, vol 5. Springer, Dordrecht.

[15] Jiawei Gao et al., "Geomagnetic field shielding over the last one hundred thousand years", J. Space Weather Space Clim., Volume 12, 2022.

[16] K. Kirby et al., "Successes and challenges of operating the Van Allen Probes mission in the radiation belts," IEEE Aerospace Conference, 2015, pp. 1-18.

[17] F. Vatalaro et al."Analysis of LEO, MEO, and GEO global mobile satellite systems in the presence of interference and fading," in IEEE Journal on Selected Areas in Communications, vol. 13, no. 2, pp. 291-300, Feb. 1995.

[18] https://www.noaa.gov/

[19] Francis F. Badavi, "Exposure estimates for repair satellites at geosynchronous orbit", doi: 10.1016/j.actaastro.2012.09.021.

[20] D. Kobayashi, "Scaling Trends of Digital Single-Event Effects: A Survey of SEU and SET Parameters and Comparison With Transistor Performance," in IEEE Transactions on Nuclear Science, vol. 68, no. 2, pp. 124-148, Feb. 2021.

[21] H. J. Barnaby, "Total-Ionizing-Dose Effects in Modern CMOS Technologies," IEEE Transactions on Nuclear Science, vol. 53, no. 6, pp. 3103-3121.

[22] K. Böhmer *et al.*, "Neutron Radiation Tests of the NEORV32 RISC-V SoC on Flash-Based FPGAs," *2023 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, Juan-Les-Pins, France, 2023, pp. 1-6, doi: 10.1109/DFT59622.2023.10313556.

[23] E. Vacca et al., "Layout-oriented radiation effects mitigation in RISC-V soft processor". 2022, In Proceedings of the 19th ACM International Conference on Computing Frontiers (CF '22). Association for Computing Machinery, New York, NY, USA, 215–220. https://doi.org/10.1145/3528416.3530984.

[24] P. Kenterlis et al.,"A low-cost SEU fault emulation platform for SRAM-based FPGAs," 12th IEEE International On-Line Testing Symposium (IOLTS'06), Lake Como, Italy, 2006, pp. 7 pp.-, doi: 10.1109/IOLTS.2006.5.

[25] C. De Sio et al., "PyXEL: Exploring Bitstream Analysis to Assess and Enhance the Robustness of Designs on FPGAs," in 2023 19th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Jul. 2023, pp. 1–4.

[26] AMD, Soft Error Mitigation Controller v4.1, (PG036), 2018

[27] https://www.eutelsat.com/files/PDF/brochures/EUTELSAT_SATELLITE_E10B.pdf

[28] S. Azimi et al., "A comparative radiation analysis of reconfigurable memory technology: FinFET versus bulk CMOS", Microelectronics Reliability, Volume 138, 2022, doi: /10.1016/j.microrel.2022.114733.