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Validation of the 65 nm TPSCo CMOS imaging technology for the ALICE ITS3

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Abstract: During the next Long Shutdown (LS3) of the LHC, planned for 2026, the innermost three layers of the ALICE Inner Tracking System will be replaced by a new vertex detector composed of curved ultra-thin monolithic silicon sensors. The R&D initiative on monolithic sensors of the CERN Experimental Physics Department, in cooperation with the ALICE ITS3 upgrade project, prepared the first submission of chip designs in the TPSCo 65 nm technology, called MLR1 (Multi Layer Reticle). It contains four different test structures with different process splits and pixel designs. These proceedings illustrate the first validation of the technology in terms of pixel performance and radiation hardness.

Keywords: Particle tracking detectors; Radiation-hard detectors; Timing detectors; Front-end electronics for detector readout

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Contents

1 Introduction

The ALICE Inner Tracking System upgrade (ITS3), planned for the LHC Long Shutdown 3 (2026–2028), will feature the substitution of the three inner layers of the current Inner Tracker (ITS2) in favour of three truly cylindrical sensors. The technology identified as a leading candidate to meet the requirements of the ITS3 is the TPSCo 65 nm process [1]. The reasons behind this choice are the fact that the ITS3 detector design foresees wafer-scale O (10 cm × 30 cm) sensors and the necessary wafer size is available in this technology node, giving access to large stitched sensors [2]. Furthermore, the sensors can be thinned down to < 50 µm and bent to 19, 25.2 and 31.5 mm curvature radius. In this technology, sensor optimization plays a crucial role, as already applied in the 180 nm CMOS imaging technology [3, 4].

The main sensor features are the presence of an octagonal-shaped *n*-well collection electrode with 1.14 µm diameter and of a high-resistivity *p*-type epitaxial layer with a thickness ~10 µm, grown on top of a low-resistivity *p*-doped substrate. Full CMOS circuitry is located on devoted *n*-wells and *p*-wells, shielded by a deep *p*-well. Three different implant geometries were designed: standard, modified, and modified-with-gap, illustrated in figure 1. Because of the spherical shape of the *pn* junction, in the standard process it is very difficult to deplete the epitaxial layer over its full width, while in the modified one, by means of an additional low dose *n*-type implant, the *pn* junction from which the depletion starts is shifted more in depth in the sensor, allowing to reach a uniform and complete sensor depletion. The application of a higher reverse bias increases the depletion volume, keeping at the same time the collection electrode small, preserving a low capacitance. In the modified-with-gap process, a gap in the additional *n*-layer has been introduced near the pixel edge, in order to speed up the charge collection process thanks to an increased lateral electric field.

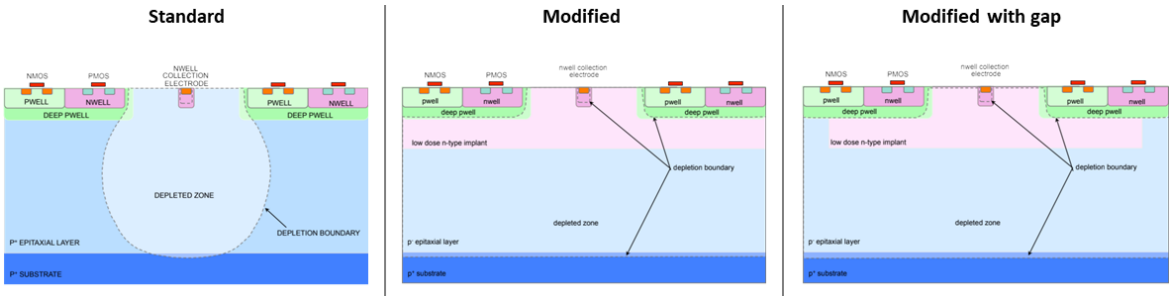

Figure 1. Three process variants implemented in the MLR1 chips.

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2 First submission in 65 nm CMOS IS technology

The Multi-Layer-Reticle (MLR1), shown in figure 2 (left), was the first submission in the 65 nm TPSCo CMOS technology, in a joint proposal between the CERN Experimental Physics Department and the ALICE ITS3 project. It was produced in summer 2021 with the aim of evaluating the charge collection performance of the targeted process that, up to that time, was mainly addressed to light detection applications. It contains transistor test structures for radiation hardness evaluations, together with diode matrices for charge-collection studies.

The four prototype chips, illustrated in figure 2 and all measuring $1.5 \times 1.5\ \mathrm{mm}^2$, are the following: Analogue Pixel Test Structure with a source-follower based readout chain (APTS-SF), Analogue Pixel Test Structure with operational amplifier as output stage (APTS-OA), Digital Pixel Test Structure (DPTS) and Circuit Exploratoire 65 (CE-65).

The first two share an identical front end, the only difference being the possibility, for the OA version, to achieve a better timing performance thanks to the operational amplifier contribution. For both of them the chip is a matrix of 6×6 pixels with direct analogue readout of the central 4×4 submatrix with the aim of testing the pixel cell and comparing process modifications.

The DPTS is a matrix of 32×32 pixels with 15 µm pitch in the modified-with-gap flavour. Each pixel is equipped with an amplifier and a discriminator, providing a time encoded digital readout with the purpose of testing the pixel front-end. Finally, the CE65 contains a pixel matrix with analog readout in a rolling shutter configuration.

In order to validate the technology for HEP applications, extensive and challenging characterization campaigns were carried out both in laboratory and at test beam facilities. In the following sections the most important results are summarised.

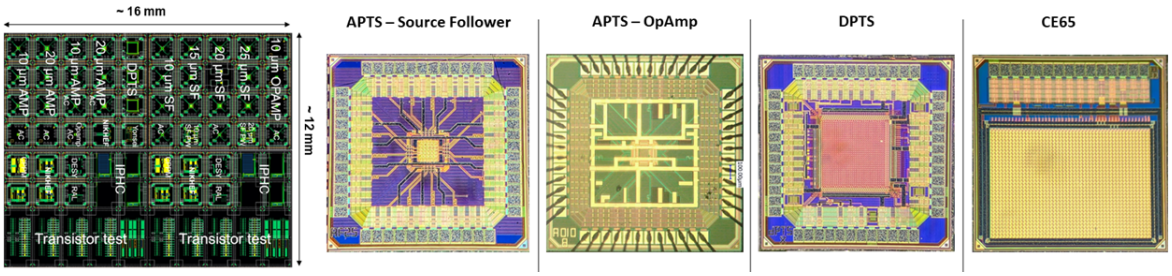

Figure 2. MLR1 submission (left). Chips belonging to the MLR1 submission (right): in order APTS (Source-Follower and OpAmp version), DPTS and CE65.

3 Laboratory tests with X-rays

The first part of the characterization has involved the use of a ^{55}Fe source to perform the signal calibration, to study the charge collection process and to compare different process modifications. A significant impact on the charge collection is determined by the implant geometry, which has been studied on APTS chips. By looking at the seed pixel signal spectrum (i.e. the charge collected by the pixel with the highest amount of collected charge in a cluster), reported in figure 3 (left), one can notice that for the standard process, the charge sharing contribution is dominant, shown by the population located to small seed pixel signals, which is strongly suppressed for the modified and

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modified-with-gap processes. In these process modifications, the charge is mainly collected by a single pixel, as it clearly appears from the Mn-K$_\alpha$ peak located ~1640 e.

The effect of different applied reverse bias voltages can be observed in figure 3 (right), showing spectra for the modified-with-gap process. As a consequence of the increased reverse bias, the amplitude progressively increases as well, as can be noticed from the shift of the Mn-K_α peak, translating into a reduction of the input capacitance.

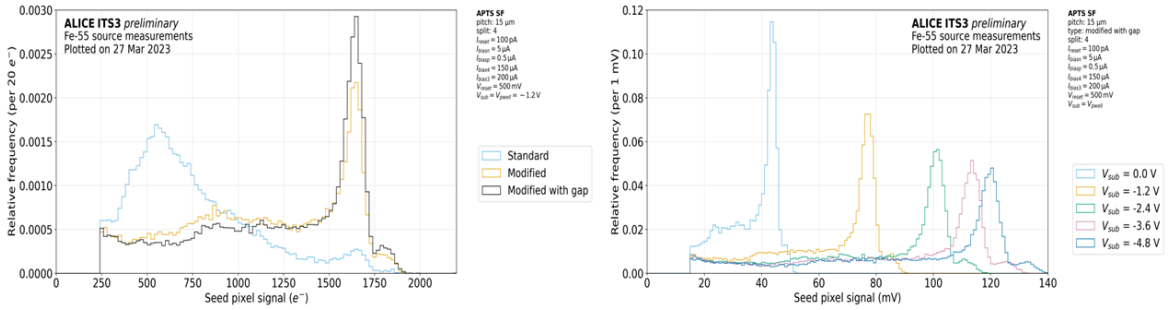

Figure 3. Distribution of collected charge for the standard, modified and modified-with-gap implant geometry (left) and collected charge distributions for the modified-with-gap process at different reverse biases (right).

4 In-beam measurements

The second part of the characterization was performed at test beam facilities with minimum ionizing particles. The analysis is based on a reconstruction software [5] that fits General Broken Lines to clusters on the reference planes and, subsequently, by interpolating the tracks to the DUT,[1] associates or discards the tracks. Plenty of test beam campaigns have been completed starting from 2021 with the goal of measuring the detection efficiency and the fake-hit-rate[2] (FHR). Furthermore, also the sensor spatial and temporal resolutions were measured.

In-beam measurements conducted on the DPTS prototypes allowed the detection efficiency measurement for both non-irradiated and irradiated chips. In particular, figure 4 (left) shows the detection efficiency of a non-irradiated chip at different thresholds and considering a set of different reverse biases. Only for the lowest reverse bias of 0.6 V, a FHR above the measurement sensitivity limit is observed for a low threshold. This result ensures a wide operational range of the sensor featuring a detection efficiency above 99%.

By considering the detection efficiency of the chip irradiated to a combination of an ionizing dose of 10 kGy (TID) and a non-ionizing dose of 1×10^{13} 1 MeV n_{eq} cm^{-2} (NIEL) on figure 4 (right), it is possible to observe that by increasing the reverse bias, the onset of the measured FHR is offset to lower thresholds. This results in the preference of larger reverse bias voltages when operating the sensor at lower thresholds, with a wide operational margin at about 99% detection efficiency [6]. The aforementioned irradiation levels are of particular interest since they represent the posed requirements of the ALICE ITS3 project.

[1] Device under test.

[2] Number of hits per pixel and second in absence of external stimuli.

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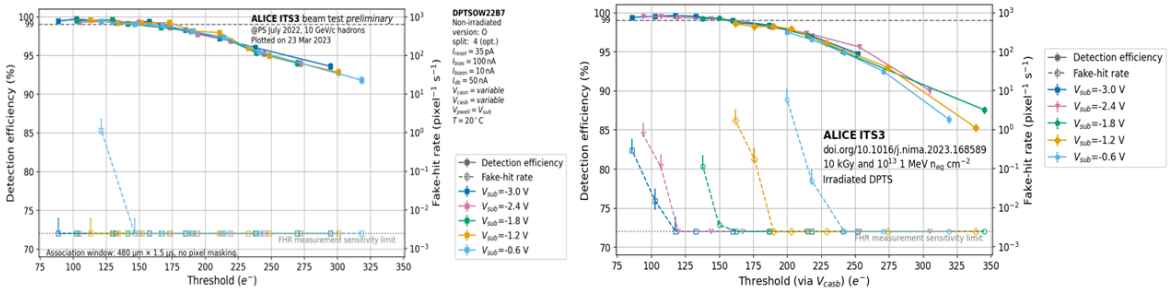

Figure 4. Detection efficiency and fake hit rate for a non irradiated DPTS chip (left) and for an irradiated DPTS at 10 kGy (TID) and 1×10^{13} 1 MeV n_{eq} cm^{-2} (NIEL) (right) as a function of the threshold. Different colors refer to different reverse bias voltages (V_{sub}).

A relevant study carried out on the DPTS chip is related to the chip performance at different power consumption regimes. Figure 5 shows the DPTS detection efficiency with different I_{bias} currents and, as a consequence, with a different power consumption, being the I_{bias} current the main biasing current of the front-end [7]. Except for the I_{bias} = 10 nA case, the efficiency reaches 99% or more for all the I_{bias} values and the power consumption estimation remains better than the target for the ALICE ITS3 (power consumption ~15 mW cm^{-2} with I_{bias} = 30 nA).

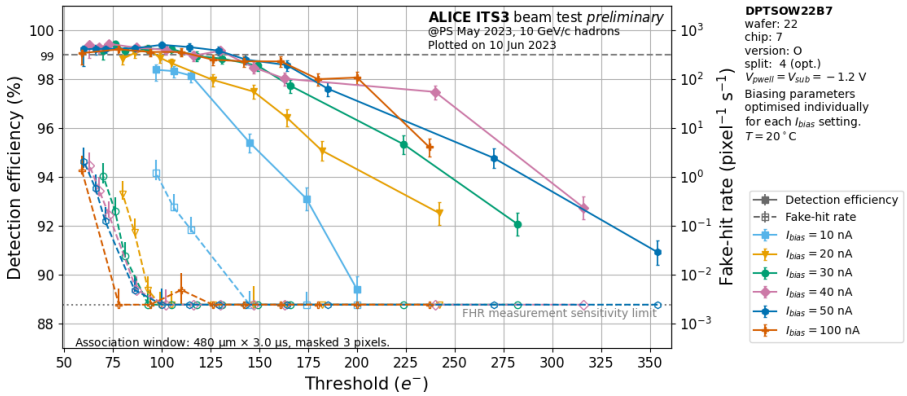

Figure 5. DPTS detection efficiency as a function of the threshold with different I_{bias} currents in the front-end circuit.

A comparison of three different prototypes belonging to the MLR1, tested with in-beam measurements is shown in figure 6. It illustrates the seed pixel signal distribution, in electrons, for APTS, CE65 and DPTS, all of them with a pixel pitch of 15 µm and for the modified-with-gap process. One can observe that all the spectra are in agreement. In order to evaluate their compatibility, the difference among each test structure and their mean has been computed. The differences, divided by the uncertainty, provide a quantitative comparison (figure 6 bottom panels), leading to the conclusion of sensors compatibility within 2 sigma for APTS and DPTS and within 4 sigma for CE65 at high seed pixel signal.

The timing performance of the APTS-OA test structure was evaluated with in-beam measurements of two APTS-OA. Figure 7 shows the time residual distribution of the two sensors by applying a CFD technique with 10% threshold.

From the sigma of the gaussian fit, a timing resolution of (77 ± 5) ps was determined.

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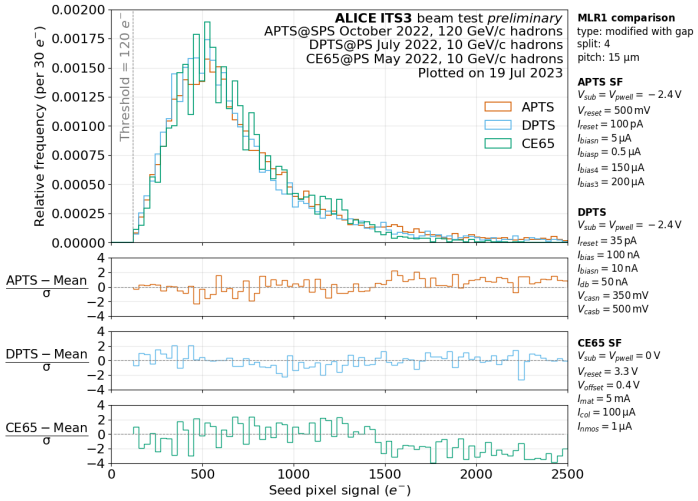

Figure 6. Distributions of collected charge deposited by charge particles during in-beam measurements for APTS (red), DPTS (blue) and CE65 (green). Bottom plots show the difference between each DUT and the mean of the three, in units of sigma.

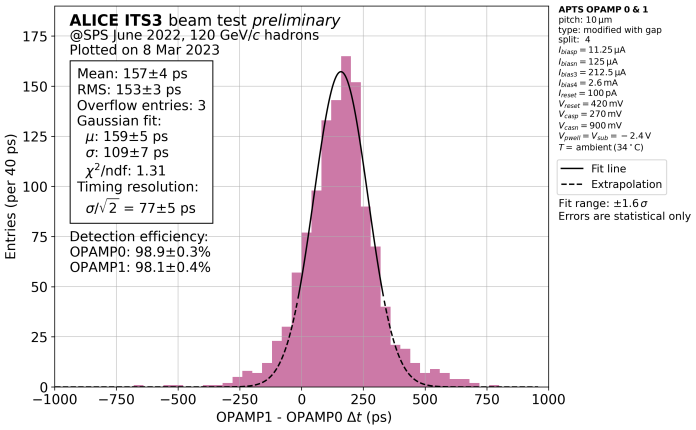

Figure 7. Time residual distribution of two APTS-OA with a sumperimposed gaussian fit to extract the timing resolution.

5 Conclusions

The TPSCo 65 nm technology has been validated for particle detection in terms of charge collection efficiency, detection efficiency, and radiation hardness. Extensive test campaigns were carried out with a ^{55}Fe source on different prototypes and demonstrated a better charge collection performance for the modified-with-gap process, which suppresses charge sharing. Multiple in-beam measurements showed a detection efficiency above 99% for a wide range of working points and a radiation hardness within the requirements of the ALICE ITS3. Finally, a timing resolution ~77 ps was measured for the APTS-OA sensor.

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Acknowledgments

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