TCAD-Assisted Progress on the Cisco Platform Toward Low-Bias 200 Gbit/s vertical-pin Ge- on-Si Waveguide Photodetectors

TCAD-Assisted Progress on the Cisco Platform Toward Low-Bias 200 Gbit/s vertical-*pin* Ge-on-Si Waveguide Photodetectors

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***Abstract*—We discuss the characterization and numerical simulation of vertical Ge-on-Si waveguide photodetectors (VPIN WPDs) of the Cisco platform for data communications in the O-band ($1.31\ \mu$m), with the goal of optimizing their frequency response while integrating them into low-power systems. In a large set of WPDs belonging to 6 different structural variants, at a standard bias voltage of -2 V the best specimens exhibit an intrinsic electro-optic bandwidth of more than 40 GHz, which is reduced to about 10 GHz at zero bias. A comprehensive 3D multiphysics model, validated through the characterization campaign, provides design guidelines towards intrinsic bandwidths not only wider than 60 GHz at -2 V, directly suitable for application in 200 Gbit/s systems, but also wider than 40 GHz at zero bias, not including the possible recourse to extrinsic parameter engineering.**

***Index Terms*—FDTD, multiphysics simulation, silicon photonics, waveguide photodetectors, VPIN.**

I. Introduction

THE present drive of silicon photonics (SiPh) platforms [1], [2], [3], [4], [5] towards 200 Gbit/s operation [6], [7], [8] is made more challenging by the constraint of limiting the power consumption of the data communication systems [9], [10]. Ge-on-Si waveguide photodetectors (WPDs) are essential components of SiPh platforms, and it is urgent to assess the potential of competing WPD solutions in terms of their performance under low-bias operation. Comprehensive reviews of the state of the art of WPDs are provided, e.g., in [3], [8], [11], [12], [13]; the main figures of merit of a representative set of devices are reported in Table I.

TABLE I
Responsivity and Cutoff Frequency of Representative VPIN and LPIN Devices

Reference	Structure	Band	$\mathcal{R}$, A/W	f_{cutoff}, GHz
[29]	VPIN	C-band	1.09	42.5
[36]	VPIN	C-band	0.80	49.5
[26]	VPIN	C-band	0.95	103
this work, experiments	VPIN	O-band	0.9	39.8
this work, optimized	VPIN	O-band	0.76	64
[15]	LPIN	C-band	0.6	30
[20]	LPIN	C-band	0.3	265
[37]	LPIN	C-band	0.63–0.74	51

Ge-on-Si *pin* WPDs are based on either vertical (VPIN) or lateral (LPIN) heterojunctions. In the LPIN configuration, the Ge absorption region is located between two highly doped Si regions, *n*- and *p*-type, respectively [14], [15], [16], [17], [18], [19]; in the innovative approach presented in [20], thin FinFET-like LPIN WPDs have been shown to allow bandwidths f_{cutoff} in excess of 200 GHz, though at the expense of the responsivity $\mathcal{R}$.

For the more immediate future, however, it is important to fully exploit the potential of the widely used VPIN configuration, presently adopted also in the Cisco SiPh platform (see Fig. 1 for an example). VPIN WPDs having bandwidths larger than 50 GHz in the C-band have been already reported [21], [22], [23], [24], [25], [26], where this performance has been achieved mostly thanks to extrinsic parameter engineering, i.e., inductive gain peaking [27], [28], that may enhance the intrinsic frequency response of the WPD by 40% or more.

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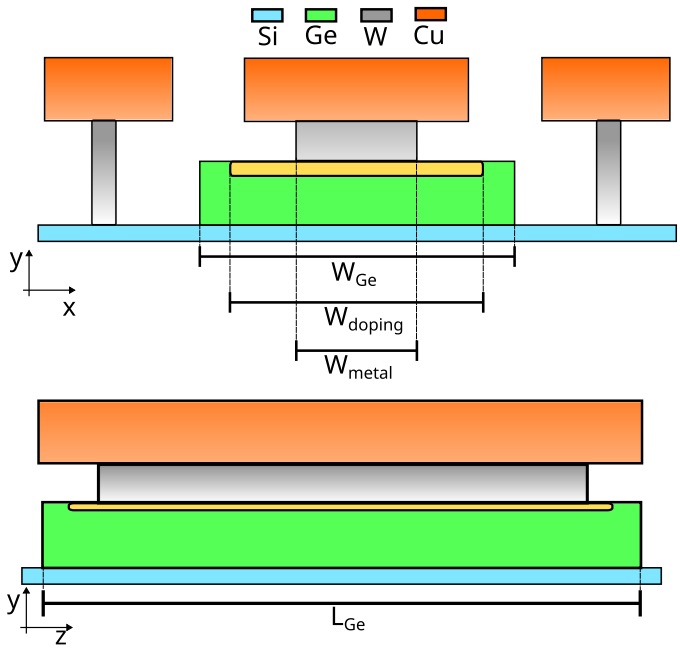


Fig. 1. Transverse (xy, top) and longitudinal (yz, bottom) cross sections of the VPIN WPD structure under study with its most significant geometrical parameters. The Ge absorber is grown on top of the Si substrate; top and lateral metallic contacts are placed on the absorber and on the substrate, respectively. Ge is considered to be intrinsic (green), with the exception of a n^+ layer resulting from ion implantation below the Ge–metal contact (yellow), while Si is heavily p-doped (blue). A 40 μm-long tapered waveguide (not shown) injects light into the substrate.

The present study is focused on the O-band, where Ge exhibits higher absorption with respect to the C-band. This results in a larger O-band responsivity, but also makes more challenging to achieve high-speed operation there, chiefly because of the stronger electric field screening caused by photogenerated carriers. Accurately describing this kind of three-dimensional (3D) multiphysics interaction requires a fully coupled analysis of electromagnetic and carrier transport phenomena. To our best knowledge, the intricacy and computational demands of such integrated 3D models have been addressed by only a few research groups so far [29], [30].

Extensive multiphysics simulations combined with experimental characterization of selected WPD variants can offer a deep understanding of the underlying physical processes, critical to develop guidelines for the design and optimization of integrated optical trasceivers that fulfill the demand of wide bandwidth and high power efficiency. Building upon our previous work [31], [32], [33], [34], [35], we demonstrate here that a multiphysics simulation framework is able to accurately describe the experimental dynamic behavior of the VPIN WPDs of the Cisco platform over a wide range of reverse voltage down to zero bias, and we use this numerical tool towards two goals: first, we propose an optimized design for a VPIN WPD that could be a promising candidate for a 200 Gbit/s receiver at a standard bias voltage of $-2\,\mathrm{V}$ even without gain peaking; second, always focusing on the intrinsic electro-optic frequency response, we explore the device performance under low power consumption.

The paper is structured as follows. In Section II we discuss the nominal geometry of the WPD used as a reference structure, the experimental characterization techniques, and the multiphysics modeling approach. Considering the intrinsic electro-optic frequency response as the main figure of merit, the model is validated against experimental data in Section III, and is used in Section IV to identify design guidelines in order to achieve optimal performance. Last, Section V outlines future work and possible developments.

II. VPIN WPD Geometry, Characterisation and Modeling

We describe first the VPIN geometry taken as reference (Section II-A) and a set of its variants (Section II-B) whose properties will be studied in Section III. Then, we present our experimental setup and characterization techniques (Section II-C). Finally, we introduce the multiphysics CAD environment (Section II-D) whose validation and results will be discussed in next two Sections.

A. Nominal Geometry and Technology

All the VPIN WPDs considered in the present work consist of a Si substrate on which a Ge absorber having length L_{Ge}, width W_{Ge} and thickness H_{Ge} is grown at low temperature [38]. Fig. 1 provides transverse (xy) and longitudinal (yz) cross sections of the device, where the input optical signal propagates along z, highlighting the key dimensions and materials. Given the mismatch between the lattice constants of Ge and Si, the growth technique results in a thin defective layer at the Si–Ge interface. Above this layer, Ge can be considered as bulk. Since the defective layer thickness is small with respect to the total Ge thickness, the non-ideal Si–Ge interface can be treated according to [32]. On top of and next to the absorber are metal contacts that reach Ge and Si, respectively. High dopant concentrations are present both in the substrate and at the metal–Ge contact, but most of the Ge absorber remains intrinsic. The n^+ layer in Ge is the result of an ion implantation process, determining a donor density $1 \times 10^{19}\,\mathrm{cm}^{-3}$ in a region about $50\,\mathrm{nm}$ thick. The acceptor density in silicon decreases from $1 \times 10^{20}\,\mathrm{cm}^{-3}$ at the metal contacts to $1 \times 10^{19}\,\mathrm{cm}^{-3}$ under the Ge layer. This vertical configuration allows for a large contact area between Si and Ge. The absorber thickness H_{Ge} plays a critical role in determining the transit time of the photogenerated carriers in the absorber [39], and therefore the frequency response of the detector. Compared to the lateral configuration, this arrangement makes the device speed generally less sensitive to other figures of merit such as the responsivity,[1] so that vertical WPDs are ideal case studies for electro-optic bandwidth optimization (see also the discussion in Section IV).

For the structure taken here as reference, the Ge layer dimensions are $L_{\mathrm{Ge}} = 15\,\mu\mathrm{m}$, $W_{\mathrm{Ge}} = 4\,\mu\mathrm{m}$, and $H_{\mathrm{Ge}} = 0.8\,\mu\mathrm{m}$,

[1]Reducing the transit time in a LPIN WPD involves reducing W_{Ge}, and the resulting "narrow" absorbers may provide a less efficient coupling with the waveguide than the "wide" absorbers preferred for VPIN WPDs, even if the cross-section area is the same: representative values of $\mathcal{R}$ in LPIN e VPIN WPDs may be compared in Table I.

TABLE II
GEOMETRICAL PARAMETERS OF THE DEVICES UNDER STUDY (SEE FIG. 1). DEVICE 2 CORRESPONDS TO THE NOMINAL GEOMETRY (REFERENCE). FOR ALL DEVICES, $L_{\mathrm{GE}} = 15\,\mu\mathrm{m}$ AND $H_{\mathrm{GE}} = 0.8\,\mu\mathrm{m}$, EXCEPT FOR DEVICE 6 WHERE $L_{\mathrm{GE}} = 18.5\,\mu\mathrm{m}$. THE LAST COLUMN REPORTS THE SIMULATED RESPONSIVITY AT A BIAS VOLTAGE OF $-3\,\mathrm{V}$ AND INPUT OPTICAL POWER $200\,\mu\mathrm{W}$

Device	W_{Ge}	W_{doping}	W_{metal}	W_{taper}	$\mathcal{R}$
1	4.0 µm	3.5 µm	1.5 µm	3.0 µm	0.84 A/W
2	4.0 µm	3.0 µm	1.5 µm	2.0 µm	0.89 A/W
3	3.0 µm	2.5 µm	2.0 µm	3.0 µm	0.76 A/W
4	3.0 µm	2.0 µm	1.5 µm	2.0 µm	0.79 A/W
5	1.5 µm	1.3 µm	1.0 µm	1.5 µm	0.79 A/W
6	1.0 µm	0.8 µm	0.5 µm	0.8 µm	0.81 A/W

whereas $W_{\mathrm{doping}} = 3\,\mu\mathrm{m}$ is the lateral extension of the n^+ Ge implantation area. The Si layers, Ge implantation region, and metals are centered with respect to the Ge absorber. The cladding material is SiO_2, and light is injected into the Si substrate through a $40\,\mu\mathrm{m}$-long tapered waveguide. The resulting evanescent coupling between Si and Ge distributes light in the absorber more evenly than direct (butt) coupling, reducing the screening effects in the front section of germanium and enhancing the performance at high input optical power, albeit at the cost of a more complex electromagnetic design.

B. Variants

In addition to the reference structure, we analyzed different variants obtained by changing the absorber and doping implantation widths (W_{Ge} and W_{doping}, respectively) while keeping constant all the other parameters. Both reference and variants are referred to as Device n, where the reference is Device 2. In total, we characterized 28 devices belonging to 6 different design variants, thus comparing several nominally identical devices for each variant. A summary of all parameter combinations considered can be found in Table II, where the devices are sorted by W_{Ge} and then by W_{doping}.

Let us examine Table II. From Device 1 to Device 6, the Ge layer width W_{Ge} varies from $4\,\mu\mathrm{m}$ to $1\,\mu\mathrm{m}$. Device 1 and Device 2 (reference) have the same W_{Ge} but a different lateral extent of the highly doped Ge region, W_{doping}, and the same can be said for Device 3 and Device 4. Considering Device 5 and Device 6, they have comparable $W_{\mathrm{doping}}/W_{\mathrm{Ge}}$ ratios but the latter has narrower W_{Ge} and W_{doping}. For all configurations, the width of the top metallic contact W_{metal} and the maximum (final) width of the optical taper W_{taper} are also reported.

C. Characterization

Static current-voltage characteristics $I(V)$ were measured on all devices under study, to determine the current both in dark (I_{d}) and under the same illumination conditions used in the ensuing radio-frequency (RF) characterization (I_{p}). As a representative example, Fig. 2 reports the static $I_{\mathrm{d}}(V)$ and $I_{\mathrm{p}}(V)$ curves for Device 2 (reference); in general, the dark current will not be a concern affecting our investigation of the design guidelines meant to optimize the frequency response.

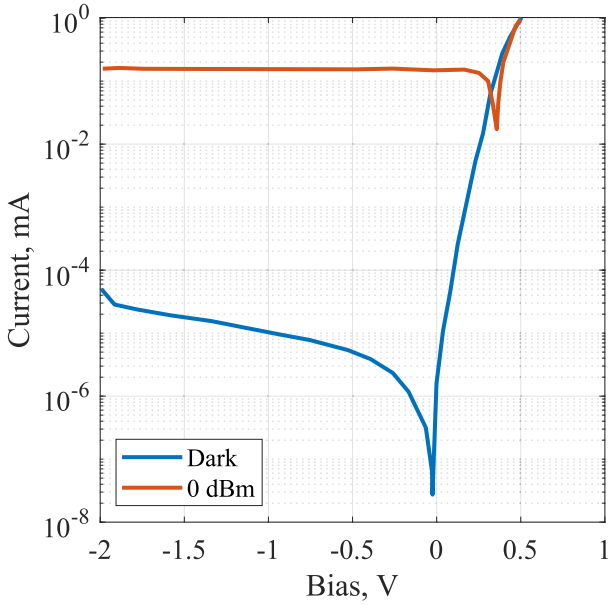


Fig. 2. Experimental $I(V)$ characteristics of a sample of Device 2 (reference) in dark (blue line) and under 0 dBm illumination (orange line).

A 50 GHz Keysight Lightwave Component Analyzer (LCA) and a Keysight network analyzer [40] were used for the small-signal RF device characterization, that began with measurements of the S-parameters in dark using the SOL method [41]. This allowed to de-embed the contributions from the measurement pads, shifting the reference plane of the measurement from the pads to the metal contacts of the WPD. After this step, the characterization exploited the LCA to obtain the optical measurements of the S-parameters under monochromatic illumination with wavelength $\lambda = 1310$ nm. The performance of the waveguide in our system is described by its coupling losses and intrinsic waveguide losses. Coupling losses, indicating the efficiency at which light is transferred from the source to the waveguide, have been estimated between $-2.7\,\mathrm{dB}$ and $-2.2\,\mathrm{dB}$. Waveguide losses, representing the attenuation of light as it propagates through the waveguide, range from $-0.23\,\mathrm{dB}$ to $-0.09\,\mathrm{dB}$.

For each device geometry, measurements were made on four (or in some variants, five) nominally identical samples taken from different regions of the wafer under test, to explore unintentional deviations in the manufacturing process. Measured S-parameter data were normalized with respect to their low-frequency value after Savitzky-Golay filtering [42].[2] Fig. 3 is an example of the electro-optic response on Device 2 (reference). The black curves are the unfiltered experimental values for each of five nominally identical devices at a bias voltage of $-3\,\mathrm{V}$, while the dashed blue curve is the result of the multiphysics simulation under the same conditions. A circuit with a resistive load of $50\,\Omega$ is considered in both simulation and measurements, and the electro-optic cutoff frequency f_{cutoff} is defined as the frequency where the amplitude of the transfer function is reduced

[2]The data in dB were calculated as $20\log_{10}(H/H_{\mathrm{LF}})$, where H is the amplitude of the electro-optic frequency response and H_{LF} is its low frequency value.

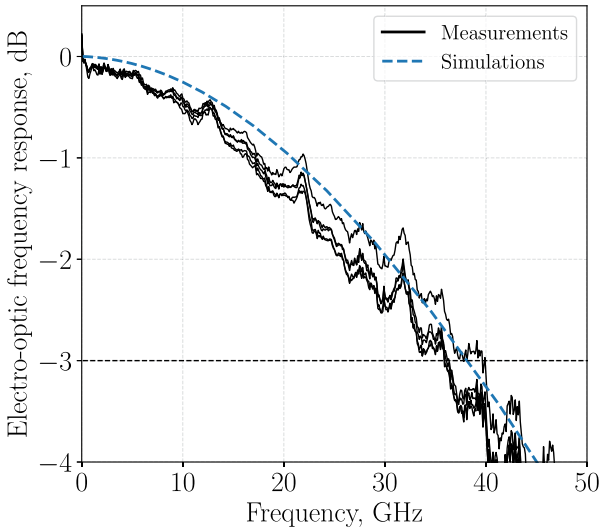


Fig. 3. Simulation (dashed blue curve) and measurements (black curves) of five nominally identical samples of Device 2 (reference), for a bias voltage of $-3\,\mathrm{V}$.

by 3 dB vs. the low-frequency value. The measured curves are well reproduced by the simulation, whose f_{cutoff} falls midway between the measured curves. A similar agreement is observed for all the device variants reported in Table II.

D. Multiphysics Modeling

The three-dimensional (3D) multiphysics model adopted in this investigation [34], [35], [43] is based on two coupled simulation codes: first, the electromagnetic problem is solved with a finite-difference time-domain (FDTD) approach, as implemented in Synopsys RSoft FullWAVE [44]; second, a drift-diffusion model (Synopsys TCAD Sentaurus, [45]) is used to describe the electrical transport problem.

As the input waveguide mode propagates along a tapered waveguide and enters the photodetector, where the Ge absorber converts the light into electron-hole pairs, FDTD allows to compute the spatial distribution of the optical generation rate $G_{\mathrm{opt}}(x, y, z)$ from the time-averaged divergence of the Poynting vector. As an example, Fig. 4 reports G_{opt} in the Ge absorber of Device 2 (reference) for an input optical power $200\,\mu\mathrm{W}$. Due to the multimode nature of the absorber, G_{opt} displays an intricate interference pattern that results in pronounced local variations. It is evident that these 3D features cannot be captured by approximate propagation models, as they are not adequately represented by a simple exponential decay of the generation term along the absorber length.

G_{opt} enters as a source term in the continuity equations of electrons and holes, which are solved self-consistently with the Poisson equation taking into account Fermi-Dirac statistics and incomplete dopant ionization. The gradual saturation of electron and hole velocities v_n, v_p for increasing electric field is described according to the Canali model [46], with a saturation velocity in Ge $v_{\mathrm{sat}} \approx 0.75 \times 10^7$ cm/s. As an example, the velocity of electrons (mostly photogenerated, under an input optical power $200\,\mu\mathrm{W}$) is mapped in Fig. 5 for two values of the bias voltage. As expected, the average velocity rises with increasing reverse bias. However, it's worth noting that, even in this scenario, the velocity displays a complex distribution that can be accurately captured only by a comprehensive 3D model. With the adopted approach, both the steady-state solution of the transport problem at equilibrium and under reverse bias, in dark and under illumination, as well as the small-signal electro-optic frequency response may be determined.

III. Validation of the Design Environment

Voltage scaling is mandatory to reduce both the static and dynamic power consumption in low-power applications. However, reducing the supply voltage may lead to a deterioration of the device performance. As a preliminary critical step towards addressing this issue with the help of multiphysics modeling, an extensive validation of the model against experimental data has been performed.

After calibrating the input optical power P_{tot} as described in [47], we plotted the experimental f_{cutoff} as a function of the bias voltage for all variants (Device 1...6) with $P_{\mathrm{tot}} = 200\,\mu\mathrm{W}$. As discussed in [47], this optical power level does not induce significant screening effects, that in general could affect the frequency response by reducing the velocity of photogenerated carriers.

We used then the multiphysics model to obtain the corresponding simulated f_{cutoff} for all geometries and operating conditions. The results, collected in Fig. 6, show the accuracy of the description provided by the model. Each of the six boxes corresponds to a different Device as described in Table II and reports several experimental curves corresponding to nominally identical devices. In all six cases, the experimental value of f_{cutoff} increases monotonically with reverse voltage, reaching an electro-optic cutoff frequency of about $40\,\mathrm{GHz}$ or higher. The same behavior is reproduced by simulations, that always follow within $2\,\mathrm{GHz}$ one of the experimental curves of the considered group.

By reducing the bias voltage from $-1.5\,\mathrm{V}$ to $-0.8\,\mathrm{V}$, a decrease of f_{cutoff} between $5\,\mathrm{GHz}$ and $10\,\mathrm{GHz}$ is observed depending on the geometry, but f_{cutoff} never becomes lower than $30\,\mathrm{GHz}$. When the bias voltage is set to zero, f_{cutoff} drops more significantly, but even at zero bias all devices have a cutoff frequency close to $10\,\mathrm{GHz}$. Our multiphysics approach is able to reproduce with very good accuracy the behavior of the frequency response for decreasing bias, difficult to predict with approximate models not based on a detailed 3D description of the device.

IV. Design Guidelines

From the results of our simulation campaign, we summarize in this Section some design guidelines that can lead to the development of Ge-on-Si VPIN WPDs compatible with 200 Gbit/s communication systems, i.e., with a bandwidth in excess of 60 GHz, even without recourse to extrinsic parameter engineering.

The first guideline regards the width of the doping implantation region at the metal–Ge contact. From Fig. 6 one may

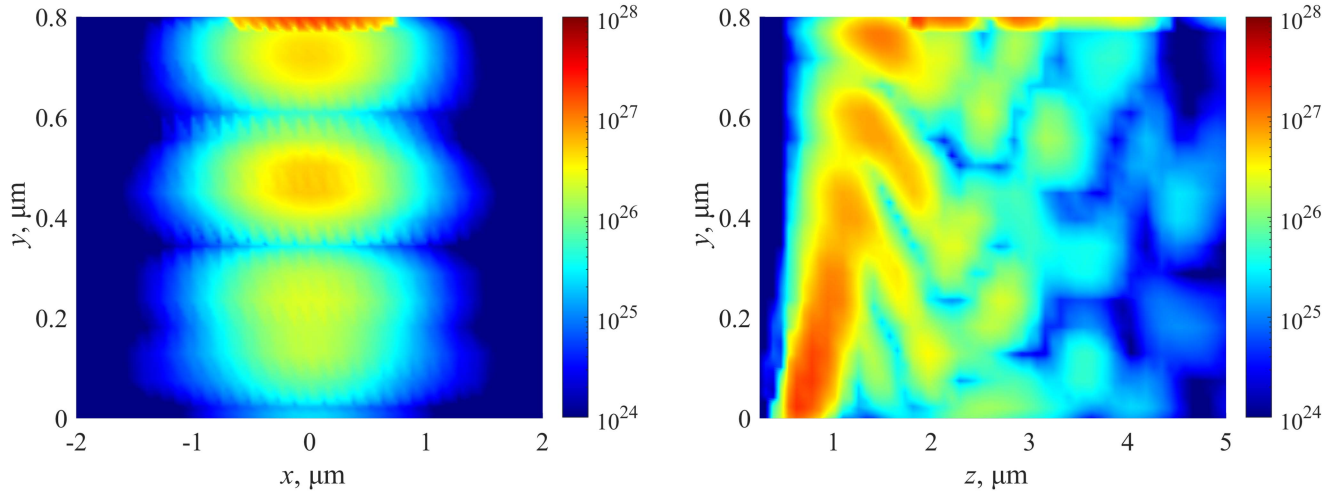


Fig. 4. Optical generation rate $G_{\text{opt}}(x, y, z)$ ($\text{cm}^{-3}\text{s}^{-1}$) in the Ge absorber of Device 2 for an input optical power 200 μW. (Left) Transverse (xy) cross section for $z = 1.8\,\mu\text{m}$, where z is measured from the beginning of the absorber. (Right) Longitudinal (yz) cross section for $x = 0$ (corresponding to the device center) and $z \in [0,\ 5]\ \mu\text{m}$.

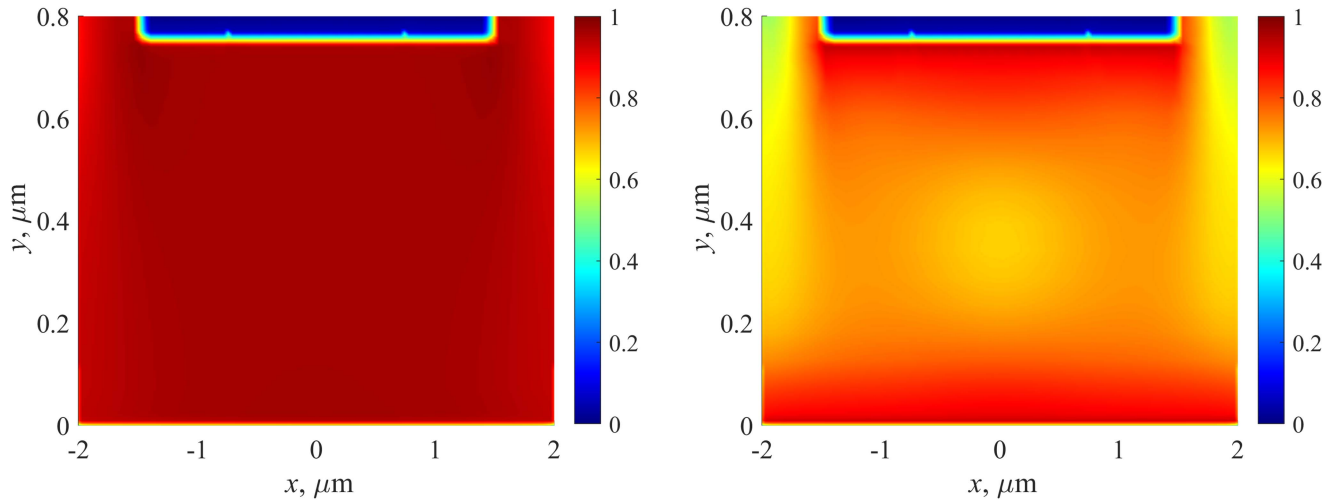


Fig. 5. Magnitude of the electron drift velocity normalized with respect to the saturation velocity, $|v_n(x, y, z)|/v_{\text{sat}}$, in the transverse (xy) cross section of the Ge absorber of Device 2 at $z = 1.8\,\mu\text{m}$ for an input optical power 200 μW. (Left) -2 V bias voltage. (Right) Zero bias voltage.

observe that Device 1 has a wider bandwidth than Device 2, and the same can be said for Device 3 with respect to Device 4. Each pair has the same W_{Ge} but a different W_{doping}, as reported in Table II, and a better performance is observed when the ratio $W_{\text{doping}}/W_{\text{Ge}}$ is closer to 1. In general, one should aim at a dopant implantation area which extends as much as possible to the whole upper surface of the absorber, since in the ideal case $W_{\text{doping}} \approx W_{\text{Ge}}$ one would observe an almost vertical electric field everywhere in Ge, favorably impacting the carrier velocity distribution.

Additional recommendations come from a set of simulations focused on the effects of W_{Ge} and H_{Ge} on f_{cutoff} and $\mathcal{R}$, for different values of the bias voltage in the interval $[-2,\ 0]$ V.

Fig. 7(a) shows the variation of f_{cutoff} for $W_{\text{Ge}} \in [1,\ 6]\ \mu\text{m}$, while all other dimensions are given the values of Device 2 with the exception of W_{doping}, which is changed in order to keep the ratio $W_{\text{doping}}/W_{\text{Ge}}$ constant. The bandwidth dependence on W_{Ge} observed in Fig. 7(a) is weakly non-monotonic, and f_{cutoff} reaches a maximum for $W_{\text{Ge}} \approx 3\,\mu\text{m}$.

The effect of H_{Ge} is more significant, as shown in Fig. 7(b), where f_{cutoff} is reported for $H_{\text{Ge}} \in [0.2,\ 1.2]\ \mu\text{m}$, while keeping all other dimensions as in Device 2. Fig. 7(b) suggests that reducing H_{Ge} should prove convenient, since an electro-optic cutoff frequency above 60 GHz is obtained for $H_{\text{Ge}} = 0.3\,\mu\text{m}$ at a bias voltage of -2 V.

The behavior of f_{cutoff} as a function of W_{Ge} and H_{Ge} in Fig. 7 is qualitatively consistent with the closed-form study in [39], where the transit time and the parasitic RC product are presented as the two main elements that limit the bandwidth. For the device under study, when H_{Ge} is decreased from $1.2\,\mu\text{m}$ to $0.3\,\mu\text{m}$, the

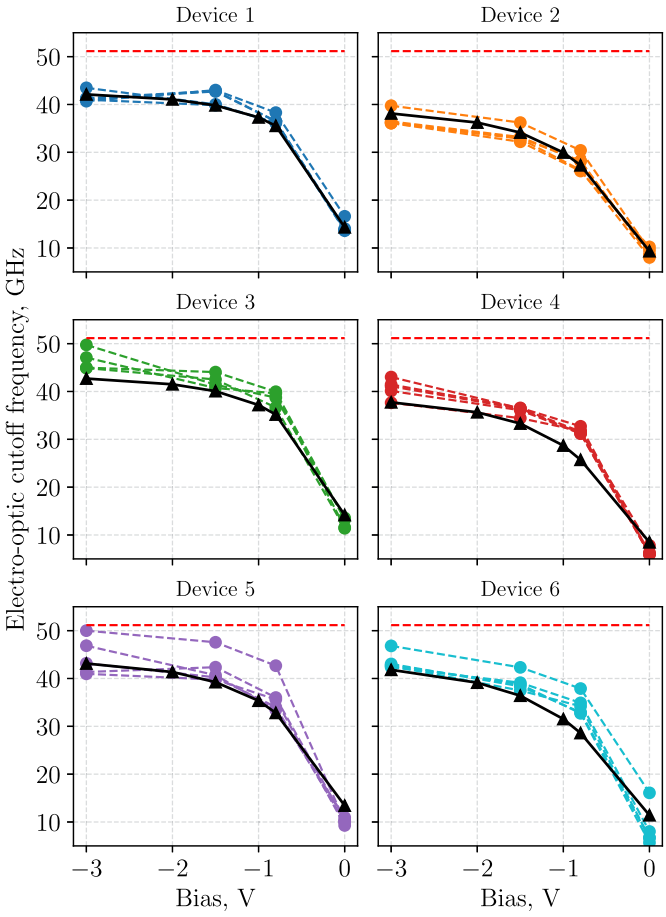


Fig. 6. Experimental values of f_{cutoff} as a function of the bias voltage for the six device variants whose geometry is reported in Table II (dashed lines), compared with the corresponding simulated curves obtained with calibrated P_{tot} (black solid lines). The horizontal red dashed lines correspond to the (bias-independent) transit-time limit according to the closed-form model of [39, Sec. 4.10.1].

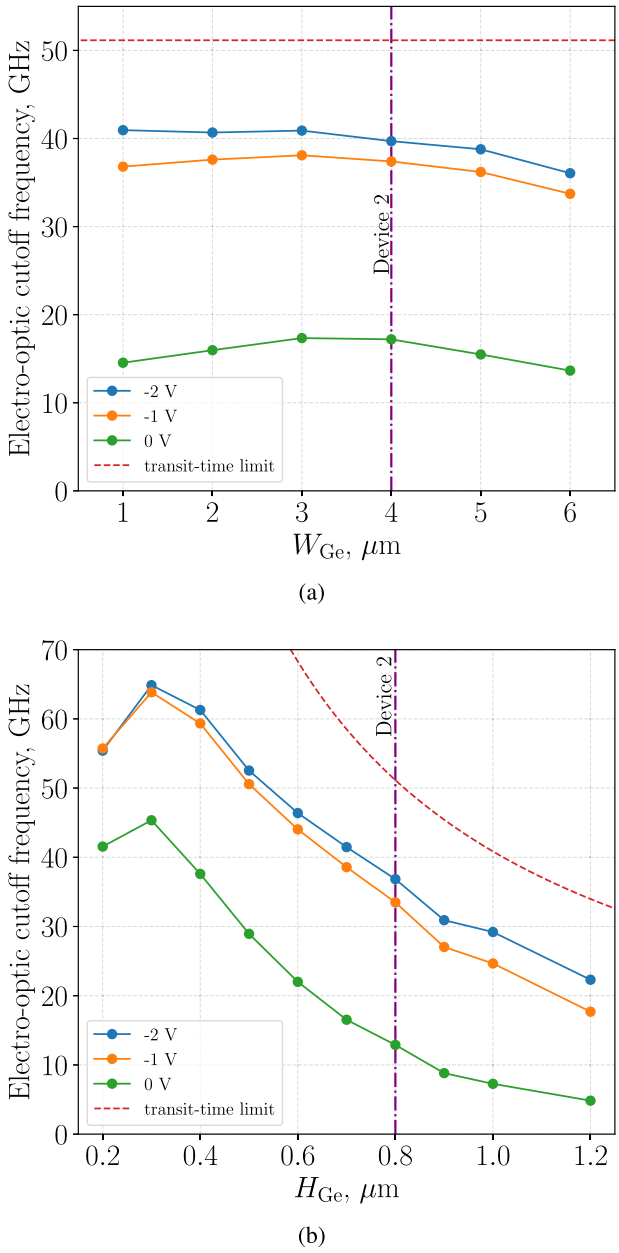
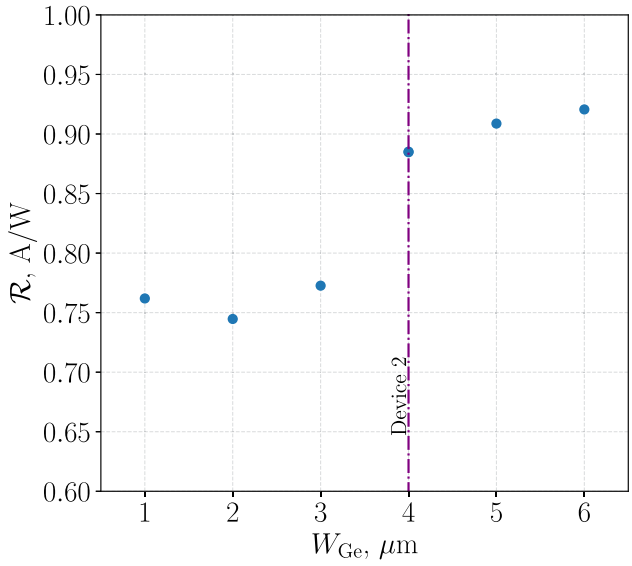


Fig. 7. Dependence of f_{cutoff} on (a) W_{Ge} and (b) H_{Ge}, starting from Device 2 (vertical dashed-dotted line), for input optical power 200 μW and bias voltage $[-2, -1, 0]$ V. The upper bound provided by the transit-time limit [39, Sec. 4.10.1] is reported as a reference (red dashed line).

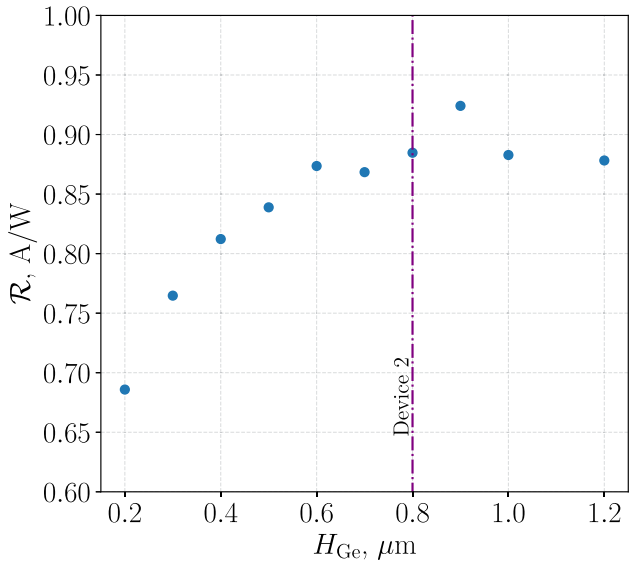
bandwidth becomes wider according to $f_{\text{cutoff}} \propto v_{\text{sat}}/H_{\text{Ge}}$ as a result of a reduction of the transit time, which is the limiting factor in this region of the parameter space [39, Sec. 4.9.3]. Conversely, when H_{Ge} is further decreased below $0.3\,\mu$m, the observed bandwidth reduction can be attributed to the RC product, since $f_{\text{cutoff}} \propto H_{\text{Ge}}/S$ [39, Sec. 4.9.4], where S is the Ge detector area in the xy plane.

The detector geometry corresponding to the maximum value of f_{cutoff} is determined by the interplay between transit time and RC limits. However, when aiming at an overall device optimization, a careful balance is required to achieve high-speed operation while preserving light detection efficiency, a critical requirement for limiting the power consumption of SOI platforms. For this purpose, Fig. 8 allows to assess the impact of W_{Ge} and H_{Ge} on the detector responsivity.[3] From Fig. 8(a) one may observe that the nominal H_{Ge} of Device 2 is near-optimal, since the marginal increase in f_{cutoff} that could be achieved by reducing the absorber width would be accompanied by a 12–15% decrease of $\mathcal{R}$. Conversely, Fig. 8(b) shows that halving the absorber thickness from $0.8\,\mu$m to $0.4\,\mu$m would provide an increase of about 25 GHz to f_{cutoff} at the cost of a 9% penalty on $\mathcal{R}$. Remarkably, a device with $W_{\text{Ge}} \approx 4\,\mu$m and $H_{\text{Ge}} \approx 0.4\,\mu$m should have an intrinsic bandwidth larger than 40GHz even at very low or zero bias, which promises the possibility for an optimized device to operate at high speed with very low power consumption.

[3]The responsivity is closely related to another important figure of merit, the energy consumption per bit e_c [48]. In the devices considered here, since the measured current exhibits a low sensitivity to the applied bias, e_c is proportional to $\mathcal{R}$. As a reference, the energy consumption per bit for a 10 Gbits modulation on Device 2 under an applied reverse bias of 2 V is of the order of $e_c = 35$ fJ/bit, comparable with the values reported in [48, Sec. III-D].



(a)



(b)

Fig. 8. Dependence of $\mathcal{R}$ on (a) W_{Ge} and (b) H_{Ge}, starting from Device 2 (vertical dashed-dotted line), for input optical power 200 μW and bias voltage -2 V. On the present plot, the values of $\mathcal{R}$ at lower bias (-1 V and 0 V) would be superimposed to the reported data points.

V. Conclusion

We have discussed the characterization and modeling of Ge-on-Si VPIN WPDs for data communications with the aim of maximizing their intrinsic frequency response in the O-band. Six device variants were manufactured, and their characterization showed that, with two exceptions, all variants achieved an electro-optic bandwidth of 40 GHz or more at $\lambda = 1310$ nm for a reverse bias of -2 V.

The experimental results were used to validate a numerical model combining 3D electromagnetic and electrical transport simulations. Since the multiphysics model was able to reproduce the experimental behavior with good accuracy, an extensive simulation campaign was carried our to identify design guidelines leading to maximum bandwidth with minimum power consumption. This campaign enabled the determination of values for W_{Ge}, W_{doping}, H_{Ge} that should provide the best performance from a trade-off between transit time and capacitive effects. The model predicts, at zero bias, a maximum intrinsic bandwidth close to the remarkable value of 45 GHz, allowing to employ Ge-on-Si VPIN WPDs in SOI platforms with reduced power consumption. Using a higher but moderate bias voltage (e.g., -2 V), a cutoff frequency larger than 60 GHz is expected, and the 4-level Pulse Amplitude Modulation (PAM-4) coding scheme should enable data transmission in excess of 200 Gbit/s.

The validated model will be employed to extend the investigation of the detailed behavior of microscopic quantities, such as the velocities of photogenerated carriers, and will support further performance improvements also by including a microscopic description of carrier transport through direct full-band Monte Carlo simulation [49].

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