Guest Editorial: Digitalbased and digitalintensive analog integrated circuits and systems

(Article begins on next page)

02 May 2024

Guest Editorial: Digital-based and digital-intensive analog integrated circuits and systems

Paolo S. Crovetti[1], ✉ [ID] and Yong Chen[2] [ID]

[1] Department of Electronics and Telecommunications (DET), Politecnico di Torino, Torino, Italy

[2] State-Key Laboratory of Analog and Mixed-Signal VLSI and IME/ECE-FST, University of Macau, Macao, China

✉ E-mail: paolo.crovetti@polito.it

Since traditional analogue and mixed-mode integrated circuits do not take advantage of scaling and are more and more often the bottleneck in terms of cost and performance of present-day integrated systems in nanoscale technologies [1], digital techniques are more and more often adopted in order to improve the performance of analogue and mixed-signal blocks [2, 3] or even to replace analogue functions with digital-based equivalents [4, 5]. This is particularly needed in order to meet the stringent requirements in terms of reconfigurability, area, power consumption and cost of emerging Internet of Things (IoT) applications [6] and biosensors [7]. In this context, the design of digital-assisted and digital-based integrated circuits is nowadays emerging as a very active area of research and this Special Issue aims at providing a vivid picture of some among the most recent advances in digital-based and digital-assisted integrated circuit design techniques across technologies and application domains. In particular, the contributions in this special issue covers the research areas of digital intensive techniques in power management integrated circuits (ICs9), high-speed data conversion and digital-assisted calibration.

Digital-based techniques in power management integrated circuits: The need for increased flexibility and reconfigurability is one of the main drivers leading to the introduction of digital-based and digital inten-sive solutions in power management ICs [8]. In this context, the Let-ter "Automatic power-stage partitioning method for reconfigurable SC DC–DC converters with reduced power-cell redundancy" by Xuchu Mu et al. [9] deals with fully integrated, digitally reconfigurable switched capacitor DC–DC converters and presents an automatic power-stage im-plementation methodology which enables reconfigurable, fine-grained voltage conversion ratios with efficient capacitance (and hence area) uti-lization and low complexity. In detail, the authors propose an algorithm which, starting from a given set of voltage conversion ratios and hard-ware constraints, generates a specific power-stage partitioning which attains a significant reduction in the number of sub-cells required for a fine-grained control of the voltage conversion ratio. The proposed methodology is applicable to both linear and binary SC converters. On the other hand, real-time reconfigurability and digital-based assis-tance can be valuable to tackle the limitations of specific DC–DC con-verter topologies. This clearly emerges from the Letter "Line-transient enhancement techniques for multi-path hybrid DC–DC converter with <1% output overshoot/undershoot" by Huihua Li et al. [10], which presents two transient enhancement techniques for multi-path switched-capacitor-inductor (MP-SCI) hybrid DC–DC converters intended to mit-igate the line-transient-induced voltage coupling to the converter out-put, that is a specific limit of this topology. In essence, the proposed solutions prevent the direct line coupling through topology reconfigura-tion and power switch modulation. The proposed controller also features adaptive line transition detection and automatic flying-capacitor voltage balancing. From simulations, the output variation reduction during line transients can be more than 94% when compared with the existing solu-tions.

High-speed data conversion: Digital-based and digital-intensive tech-niques in radio-frequency (RF) integrated systems play a pivotal role towards the virtualization of critical RF subsystem, as demanded in ver-satile, multi-standard radio transceivers leveraging the software-defined radio (SDR) paradigm [11]. The applicability of such digital-centred paradigm is however closely related to the performance of high speed of data converters which operate at multi GS/s data rates leveraging time interleaving. In such converters the input buffer is very critical and can be easily a bottleneck in terms of power and performance. This impor-tant aspect is tackled in the paper "A 10GHz bandwidth 45.5dB SNDR buffer with local feedback in 45 nm CMOS" by Jie Wu et al. [12], which proposes a high-speed buffer with bandwidth expansion and slew-rate enhancement, targeting the requirements of time interleaved data con-verters operating at 20 GS/s. The new buffer is fabricated in 45 nm COMS process, and achieves 7.2 bit ENOB at 10GHz input frequency with consuming 20.4 mW.

Digital-assisted calibration: Even before the last developments of radi-cal digital-in-concept analogue IC design approaches, digital techniques have been and are still a valuable asset to improve the performance of more traditional analogue and mixed-signal circuits [13]. In this frame-work the Letter "Digital calibration technique-based AC injection for continuous time sigma-delta converters" by Shengling Zhu et al. [14], presents an innovative digital calibration method based on AC signal in-jection for continuous-time sigma-delta analogue-to-digital converters. Compared to calibration techniques proposed in previous art, the new method does not require complex timing logic, processing or additional capacitors and does not adversely impact the dynamic performance of the converter. Furthermore, it is suitable to integration in nanoscale CMOS technologies.

Conclusion: The papers selected for this special issue present an inter-esting, although not exhaustive, picture of the present-day research on digital-based and digital intensive analogue and mixed signal techniques in power management ICs, high-speed data converters and digital-assisted calibration. In the next years, further developments related to the more and more pervasive development of the IoT and of next-gen biosensors are expected. Moreover, the development of new digital-based analogue processing approaches taking advantage of artificial in-telligence (AI) and machine learning is expected. Last but not least, digital-based and digital intensive solutions is likely to provide answers to the open challenges related to the development of analogue and sens-ing functionalities in future CMOS technology nodes and non-CMOS emerging technologies (flexible semiconductors, spintronics, quantum computing).

Author contributions: **Paolo S. Crovetti**: Writing. **Yong Chen**: Revi-sion.

Data availability statement: N/A

References

1 Kinget, P.R.: Scaling analog circuits into deep nanoscale CMOS: Ob-stacles and ways to overcome them. In: 2015 IEEE Custom Integrated Circuits Conference (CICC). San Jose, CA, pp. 1–8 (2015). https://doi.org/10.1109/CICC.2015.7338394

2 Toledo, P., et al.: Re-thinking analog integrated circuits in digital terms: A new design concept for the IoT era. *IEEE Trans. Circuits Syst. II Express Briefs* **68**(3), 816–822 (2021). https://doi.org/10.1109/TCSII.2021.3049680

3 Crovetti, P.S., et al.: Breaking the boundaries between analogue and dig-ital. *Electron. Lett.* **55**, 672–673 (2019). https://doi.org/10.1049/el.2019.1622

4 Crovetti, P.S.: A digital-based virtual voltage reference. *IEEE Trans. Circuits Syst. I Regul. Pap.* **62**(5), 1315–1324 (2015). https://doi.org/10.1109/TCSI.2015.2402991

5 Crovetti, P.S.: A digital-based analog differential circuit. *IEEE Trans. Circuits Syst. I Regul. Pap.* **60**(12), 3107–3116 (2013). https://doi.org/10.1109/TCSI.2013.2255671

6 Alioto, M.: *Enabling the Internet of Things—From Integrated Circuits to Integrated Systems*. Springer, Cham, Switzerland (2017)

7 Carrara, S.: Body dust: Well beyond wearable and implantable sensors. *IEEE Sens. J.* **21**(11), 12398–12406 (2021). https://doi.org/10.1109/JSEN.2020.3029432

8 Okuma, Y., et al.: 0.5-V input digital LDO with 98.7% current efficiency and 2.7-μA quiescent current in 65 nm CMOS. In: IEEE Custom Integrated Circuits Conference 2010. San Jose, CA, pp. 1–4 (2010). https://doi.org/10.1109/CICC.2010.5617586

9 Mu, X., Li, H., Jiang, Y., Law, M.-K., Mak, P.-I., Martins, R.P.: Automatic power-stage partitioning method for reconfigurable SC DC–DC converters with reduced power-cell redundancy. *Electron. Lett.* **58**, 957–962 (2022). https://doi.org/10.1049/ell2.12646

10 Li, H., Ma, Q., Jiang, Y., Law, M.-K., Mak, P.-I., Martins, R.P.: Line-transient enhancement techniques for multi-path hybrid DC–DC converter with <1% output overshoot/undershoot. *Electron. Lett.* **58**, 952–956 (2022). https://doi.org/10.1049/ell2.12634

11 Staszewski, R.B., et al.: All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS. *IEEE J. Solid-State Circuits* **39**(12), 2278-2291 (2004)

12 Wu, J., Meng, Q., Li, F., Huang, Y.: A 10-GHz bandwidth 45.5-dB SNDR buffer with local feedback in 45-nm CMOS. *Electron. Lett.* **59**, e12710 (2023). https://doi.org/10.1049/ell2.12710

13 Murmann, B.: Digitally assisted analog circuits; Fifth IEEE Dallas Circuits and Systems Workshop. In: 2006 IEEE Dallas/CAS Workshop on Design, Applications, Integration and Software. Richardson, TX, pp. 23–30 (2006). https://doi.org/10.1109/DCAS.2006.321026

14 Zhu, S., Chen, L., Su, J.: Digital calibration technique based AC injection for continuous-time sigma-delta converters. *Electron. Lett.* **59**, e12960 (2023). https://doi.org/10.1049/ell2.12960

Paolo S. Crovetti was born in Turin, Italy, in 1976. He received the Laurea (summa cum laude) and Ph.D. degrees in electronic engineering from the Politecnico di Turin, Turin, Italy, in 2000 and 2003, respectively. He is currently an Associate Professor with the Department of Electronics and Telecommunications (DET), Politecnico di Torino, Turin where he leads a research group in Analog, Mixed-Signal and Power microelectronics with several international collaborations and teaches courses on basic and automotive electronics. He has co-authored more than 100 papers appearing in journals and international conference proceedings. In 2009 and in 2019 he was co-recipient of the excellent paper award of the EMC'09 Kyoto Symposium and of the Best Student Paper Award of the International Symposium of Circuits and Systems ICECS 2019. His main research interests are in the fields of ultra-low power integrated circuit design and electromagnetic compatibility. His recent research activities are focused on non-conventional digital-based information processing techniques and ultra-low-voltage, ultra-low-power IC design for the Internet of Things. Prof. Crovetti is the Editor-in-Chief of IET Electronics Letters and is an Associate Editor of the IEEE Transactions on Circuits and Systems and of the IEEE Transactions on Very Large Scale of Integration Systems.

Yong Chen received the B.Eng. degree in electronic and information engineering, Communication University of China (CUC), Beijing, China, in 2005, and the Ph.D. in Engineering degree in microelectronics and solid-state electronics, Institute of Microelectronics of Chinese Academy of Sciences (IMECAS), Beijing, China, in 2010. From 2010 to 2013, he worked as Post-Doctoral Researcher in Institute of Microelectronics, Tsinghua University, Beijing, China. From 2013 to 2016, he was Research Fellow in VIRTUS/EEE, Nanyang Technological University, Singapore. In 2016, He joined the State Key Laboratory of Analog and Mixed-Signal VLSI (AMSV) of University of Macau, Macao, China, where he is now an Associate Professor. His research interests include integrated circuit designs involving analog/mixed-signal/RF/mm-wave/sub-THz/wireline.

Dr. Chen was the recipient of the "Haixi" (three places across the Straits) postgraduate integrated circuit design competition (Second Prize) in 2009, the co-recipient of the Best Paper Award at the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS) in 2019, the Best Student Paper Award (Third Place) at the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium in 2021, the Macao Science and Technology Invention Award (First Prize) in 2020, and the Macao Science and Technology Invention Award (Second Prize) in 2022, Gold Leaf Prize (Top 10% Papers) at the 18th International Conference on PhD Research in Microelectronics and Electronics (PRIME) in 2023. Dr. Chen was recognized as the top five Associate Editors in 2020, the five highest-performing Associate Editors in 2021, one of the three best Associate Editors in 2022, and one of the three best Reviewers in 2022, of IEEE TVLSI Systems.

Dr. Chen serves as an associate editor of IEEE Transaction on Very Large Scale Integration (TVLSI) Systems since 2019, a Subject Editor ('22-) for Circuits and Systems of IET Electronics Letters (EL) and an associate editor (2020-) of IET EL, an editor of International Journal of Circuit Theory and Applications (IJCTA) since 2020, Guest Editor (2022-2023) of IEEE Transactions on Circuits and Systems I: Regular Papers in 2022, guest editor (2021–2022) of IEEE Transactions on Circuits and Systems II: Express Briefs and an Associate Editor of IEEE Access (2019–2021). He serves as a vice-chair (2019–2021) and Chair (2021–2023) of IEEE Macau CAS Chapter, a Tutorial Chair of ICCS (2020), a Special Session Co-Chairs of APCCAS (2022), a conference local organization committee of A-SSCC (2019), a member of IEEE Circuits and Systems Society, Circuits and Systems for Communications (CASCOM) Technical Committee (2020–), a member of Technical Program Committee (TPC) of A-SSCC (2021–), APCCAS (2019–2022), ICTA (2020–), NorCAS (2020–), MWSCAS (2022), ICECS (2021) and ICSICT (2020, 2022), a Review Committee Member of ISCAS (2021–), and a TPC Co-Chair of ICCS (2021–2022).