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SPICE-compliant load flow analysis of power distribution networks with behavioral loads

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Abstract

This paper discusses an alternative and Simulation Program with Integrated Circuit Emphasis (SPICE)-compatible solution for the steady-state simulation of power distribution networks. It introduces two alternative auxiliary subcircuits that allow to efficiently simulate the network in any simulation tool for circuit analysis. This feature introduces remarkable benefits in terms of simplicity and generality, since it avoids the need for any iterative method, thus bridging the gap between classical industry-standard and general-purpose simulators based on circuital equations, such as SPICE, and dedicated tools for the load flow analysis of power systems. The approach is first demonstrated based on a simple illustrative example, for which the performance in terms of accuracy and efficiency is discussed and then applied to the standard IEEE 33-node power distribution benchmark.

KEYWORDS

circuit simulation, load flow analysis, power distribution networks, SPICE, steady-state analysis

1 | INTRODUCTION

Nowadays, the load flow method[1] has been consolidated as a standard tool for the operational, planning, and reliability assessments of power distribution networks.[2–4] A large number of papers are available in the literature, either with a theoretical nature that focuses on the generalization and improvement of the numerical method or with a strong application-oriented nature.[5–9]

Load flow analysis allows computing the sinusoidal steady-state response of a power network by suitably recasting the constitutive relations of the different involved elements, like transmission lines and loads, in the phasor domain, yielding a set of nonlinear algebraic equations that can be solved by an iterative algorithm. It usually relies on a simple and effective behavioral approach in which possibly complex blocks that are widespread in a modern power distribution network, including solar panels, electric vehicles charging hubs, and storage units, are defined in terms of complex absorbed or supplied power.[10] Typical examples are provided by the active and reactive powers absorbed by the users in a residential building or supplied by a photovoltaic panel.

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The second aspect, related to the description of circuit blocks in terms of complex power, makes the power flow analysis to differentiate from the classical circuit simulation carried out by means of tools such as the Simulation Program with Integrated Circuit Emphasis (SPICE) or its commercial versions that are massively used in the industry as a standard simulation engine for the design of electrical and electronic circuits.[11] In SPICE, a block is preferably described in terms of current-voltage relations based on basic circuit elements. Also, a sharp barrier exists between transient (.TRAN) and sinusoidal steady-state (.AC) analyses, the latter being unsuitable when loads are defined in terms of complex power, which depends on node voltages or branch currents thereby leading to a problem which is inherently nonlinear in the phasor domain. Because of this, load flow analysis naturally led to the development of alternate and by now mature tools that are available in a many open source or commercial solvers for power system analysis.[12–14]

In recent years, alternative approaches that use a more classical circuital interpretation of the network have been investigated for both power transmission and distribution systems.[15,16] They rely on the application of traditional methods for circuit analysis inspired by the modified nodal analysis (MNA), thus offering a flexible and general solution. These methods use MNA equations just like SPICE, but a custom implementation of the algorithm in a different simulation engine (e.g., MATLAB) is still required.

Based on the above picture, this paper is aimed at bridging the gap between the two abovementioned simulation worlds by providing an approach for load flow analysis that can be fully integrated into SPICE, thereby extending its analysis scope. Indeed, the novel contribution of this research work is to present a method for simulating the steady-state response of a power distribution network with loads described by their absorbed active and reactive power. It relies on the SPICE engine only, without the need for external tools or custom modifications of the solver.

The method is applied to the SPICE simulation of two test cases: a simple circuit aimed at illustrating the validity and strength of the proposed approach, as well as highlighting the different performances of the two subcircuits for detecting the root-mean-square (RMS) voltages, and a more realistic test case consisting of the IEEE 33-node single-phase benchmark power network.

2 | BEHAVIORAL LOAD DESCRIPTION

In power flow analysis, loads are typically described in terms of complex (active and reactive) power, rather than by their physical resistance-inductance (RL) description. In AC analysis, the complex power is computed using phasor voltages and currents as

$$S = P + jQ = \frac{1}{2}\hat{V}_{\text{peak}}\hat{I}^*_{\text{peak}} = \hat{V}_{\text{rms}}\hat{I}^*_{\text{rms}}, \tag{1}$$

depending on weather the amplitude or RMS value is used for the phasor magnitude.

By describing the load in terms of admittance $Y = G + jB$ and combining (1) with Ohm's law in the phasor domain, the active and reactive power are expressed as

$$P = GV^2_{\text{rms}}, \quad Q = -BV^2_{\text{rms}}, \tag{2}$$

where $V_{\text{rms}} = |\hat{V}_{\text{rms}}|$ denotes the RMS value of the node voltage. Therefore, the equivalent load conductance and susceptance are computed as

$$G = \frac{P}{V^2_{\text{rms}}}, \quad B = -\frac{Q}{V^2_{\text{rms}}}. \tag{3}$$

Recall that the conductance is simply the reciprocal of the resistance and that the susceptance of an inductance is $B = -1/(\omega_0 L)$, with $\omega_0 = 2\pi f_0$, where f_0 is the operating frequency. Then, the load can be interpreted as the parallel connection of a resistive and an inductive load with

$$R = \frac{1}{G} = \frac{V^2_{\text{rms}}}{P}, \quad L = -\frac{1}{\omega_0 B} = \frac{V^2_{\text{rms}}}{\omega_0 Q}. \tag{4}$$

Therefore, for the time-domain simulation, we can define the equivalent, behavioral load illustrated in Figure 1. Note that we emphasized the fact that the RMS values, as well as the active and reactive power values, are in general a function of time, since the circuit should be able to track variations in the load configuration over time. However, once the circuit has reached the steady-state, their values become constant.

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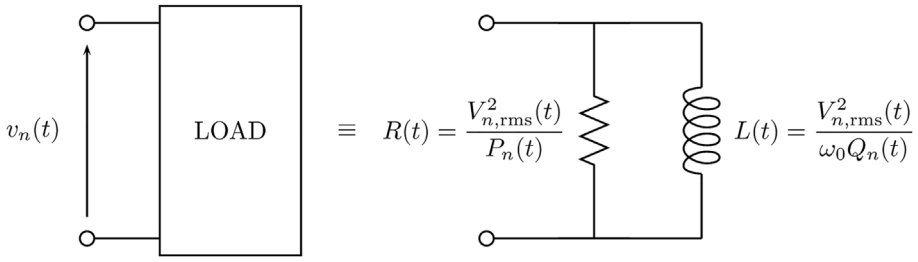

FIGURE 1 Behavioral load description in terms of time-varying resistance and inductance as a function of the RMS node voltage and active and reactive power consumption.

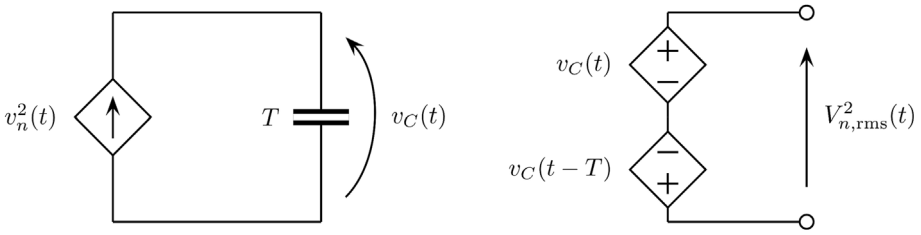

FIGURE 2 First implementation of the RMS detector circuit. The output produces the integral of $v^2(t)$ over one full period, corresponding to the square of the RMS input voltage.

At this point, we need a companion circuit capable to detect and track (the square of) the node RMS voltages. Two alternative implementations are discussed next. The first alternative is based on a nonstandard interpretation that yields a very fast convergence of the RMS detection when a transient simulation is carried out. The second implementation relies instead on a more classical interpretation of the RMS value.

2.1 | RMS detector #1: Capacitor with delay

Let us recall the definition of the RMS value of a periodic signal $x(t) = x(t+T)$, which reads

$$X_{\mathrm{rms}} = \sqrt{\frac{1}{T}\int_0^T x^2(t)dt}, \tag{5}$$

that is, the integral over one period of the squared signal, normalized by the period itself. For a sinusoidal signal, this leads to the well-known relationship $X_{\mathrm{rms}} = X_{\mathrm{peak}}/\sqrt{2}$. Let us also recall the governing equation of a capacitor, whose integral form yields the voltage across the capacitor as

$$v_C(t) = \frac{1}{C}\int_{-\infty}^{t} i_C(t)dt. \tag{6}$$

Therefore, if we let a current $i_C(t) = v^2(t)$ flow through a capacitance that is numerically equal to the period ($C = T$), we get that

$$v_C(t) - v_C(t-T) = \frac{1}{T}\int_{t-T}^{t} v^2(t)dt = V^2_{\mathrm{rms}}(t). \tag{7}$$

Hence, the squared RMS value of voltage $v(t)$, computed over the last period, is obtained as the difference between the capacitor voltage and its value delayed by T.

We can therefore put forward the first implementation of the RMS tracking circuit, illustrated in Figure 2. It should be noted that some SPICE simulators, such as HSPICE, can directly embed a delay in controlled sources. In the general

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case, an ideal matched transmission line with delay $T_D = T$ can be used to obtain the necessary delayed version of $v_C(t)$.

The main advantage of this circuit is its fast tracking time. Indeed, once the steady state is reached, it takes only one full period to track the current RMS value. The main drawback is that the capacitor voltage keeps growing indefinitely, since it integrates an always-positive current. Hence, the overall circuit has no actual steady-state solution. However, this is not critical since the steady-state solution of the main network is achieved in a few cycles of the sinusoidal excitation.

2.2 | RMS detector #2: Low-pass filter

To derive the second RMS detection circuit, we start by computing the square of a sinusoidal signal $x(t) = X_{\text{peak}} \cos(\omega_0 t + \varphi)$:

$$\begin{aligned} x^2(t) &= X_{\text{peak}}^2 \cos^2(\omega_0 t + \varphi) \\ &= 2X_{\text{rms}}^2 \left(\frac{1}{2} + \frac{1}{2} \cos(2\omega_0 t + 2\varphi) \right) \\ &= X_{\text{rms}}^2 + X_{\text{rms}}^2 \cos(2\omega_0 t + 2\varphi), \end{aligned} \tag{8}$$

where the well-known formula for the square of the cosine was used. Hence, the squared RMS value can be interpreted as the DC component of $x^2(t)$. The DC component can be extracted by means of a low-pass filter, for example, a simple first-order RC circuit, leading to the alternative detector circuit illustrated in Figure 3.

It should be noted that, in this case, there is a trade-off between the tracking speed and the rejection of the sinusoidal component at $2\omega_0$, which may cause the detected RMS voltage to (slightly) oscillate around the correct value. For example, the transfer function of a first-order low-pass RC filter reads

$$H(j\omega) = \frac{\omega_c}{\omega_c + j\omega} \tag{9}$$

where $\omega_c = 1/(RC) = 1/\tau$. Based on that, we can determine the time constant τ for which the sinusoidal component is attenuated by a predefined level A. The condition is

$$\omega_c : |H(j2\omega_0)| = \frac{\omega_c}{\sqrt{\omega_c^2 + 16\pi^2 f_0^2}} = A \tag{10}$$

Larger values of τ (smaller values of ω_c) would yield higher attenuation of the sinusoidal component. On the other hand, they also lead to longer tracking times. Indeed, recall that it takes roughly 5τ for a first-order circuit to reach the steady-state. Overall, the tracking time may be higher than that, since the whole circuit must reach the steady-state.

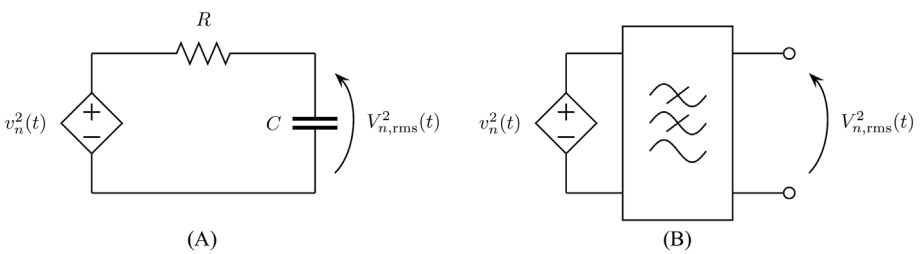

FIGURE 3 Alternative implementation of the RMS detector circuit. A low-pass filter is used to isolate the DC component of $v^2(t)$, corresponding to the square of the RMS input voltage. The filter can be either a simple RC circuit (A) or a generic higher-order filter (B)

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It was found that setting an attenuation of 40 dB, corresponding to $\tau = 0.159$ s for $f_0 = 50$ Hz, provides satisfactory accuracy and that it is safe to assume 10τ as a margin for the circuit to reach the steady-state. Hence, the tracking time is roughly $1.6\text{s} = 80 \cdot T$. If necessary, a better tracking performance can be achieved by means of a higher-order filter, as will be shown in the next section.

3 | DISCUSSION AND NUMERICAL RESULTS

It is important to point out that the behavioral load of Figure 1 as well as the RMS tracking circuits of Figures 2 and 3 are readily implemented in any standard SPICE implementation. Despite more advanced behavioral descriptions coupled be used based, for example, on Verilog-A language, for wider compatibility, we propose a model relying exclusively on a circuital description and standard components. In particular, the model requires the definition of behavioral resistors and inductors, with resistance and inductance values that depend on the output of the corresponding RMS tracking circuit. For "static" simulations, the active and reactive power values for each load are defined as fixed simulation parameters. When the loading configuration varies over time instead, the power values are stepped by means of controlling piece-wise linear (PWL) sources.

The behavioral circuit outlined in Section 2, together with the two alternative RMS detector circuits, has been implemented in HSPICE. In this section, we apply the proposed approach to two test cases. The first one is a synthetic, illustrative example introduced for a preliminary assessment of the feasibility of the proposed solution and to highlight the different performances of the two RMS detector circuits. The second test case is a realistic 33-node bus from the IEEE benchmarks instead.

3.1 | Synthetic example

Let us consider the illustrative example shown in Figure 4. The circuit emulates a two-node power network with inductive loads. To mimic a load change, we assume that the switches disconnect part of the loads after 2 s. The source is a sinusoidal generator with a peak voltage normalized to 1 V and a frequency of 50 Hz ($T = 20$ ms).

First, a forward AC simulation is run in the two loading conditions to obtain the steady-state node voltages and the active and reactive power absorbed by the loads. The results are summarized in Table 1. Then, a transient simulation is run for the same sinusoidal source by replacing the two loads with the behavioral circuit of Figure 1 in conjunction with one implementation of the RMS detectors outlined in Section 2. The template netlist of the equivalent circuits replacing the physical loads is provided in the dashed box on the right, using as an example the detector circuit of Figure 2. Varying values of P and Q are specified as PWL voltage sources controlling the resistance and inductance values.

The top panel of Figure 5 shows the value of $V^2_{1,\text{rms}}$ and $V^2_{2,\text{rms}}$ detected using the RMS detector of Figure 2. The values are consistent with the fourth column of Table 1. The precision and stability of the detected RMS value can be appreciated, together with tracking speed. For this example, less then 0.2 s is needed for the circuit to reach the steady-state, which corresponds to 10 cycles of a sinusoidal signal at 50 Hz. This number of cycles is comparable to the number of iterations required by classical numerical methods for load flow analysis (see, e.g., the comparative analysis in Memon et al.[17]). The bottom panel shows the RMS values detected using the circuit of Figure 3A instead. As expected,

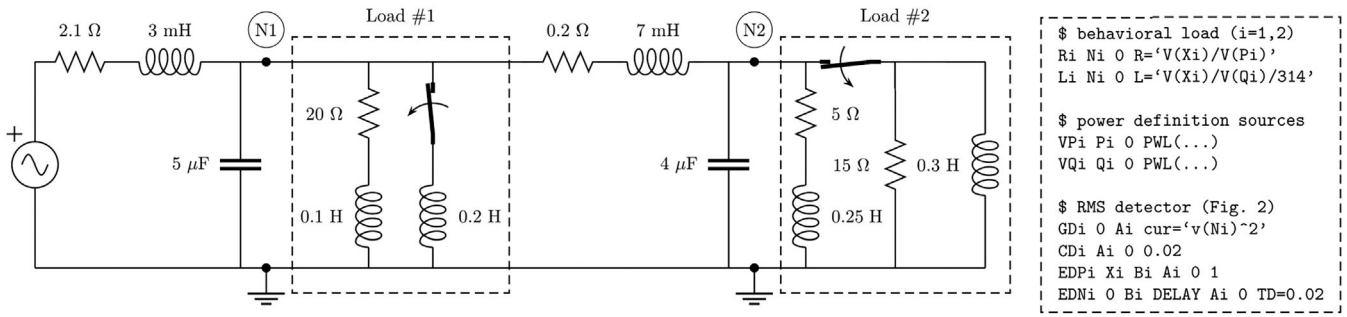

FIGURE 4 Circuit schematic for the illustrative example. An HSPICE netlist of the behavioral model replacing the physical loads is provided on the right.

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TABLE 1 Node voltages and active and reactive power (expressed in milliwatts and millivolt-amperes reactive, respectively) absorbed by the loads in the circuit of Figure 4.

Time t (s)	Node # n	$V_{n,\text{peak}}$ (V)	$V^2_{n,\text{rms}}$ (V^2)	P (mW)	Q (mvar)
$0 < t < 2$	1	0.8200	0.3362	4.8	13.0
	2	0.7652	0.2928	19.8	6.8
$t > 2$	1	0.9402	0.4419	6.4	10.0
	2	0.9170	0.4204	0.3	5.3

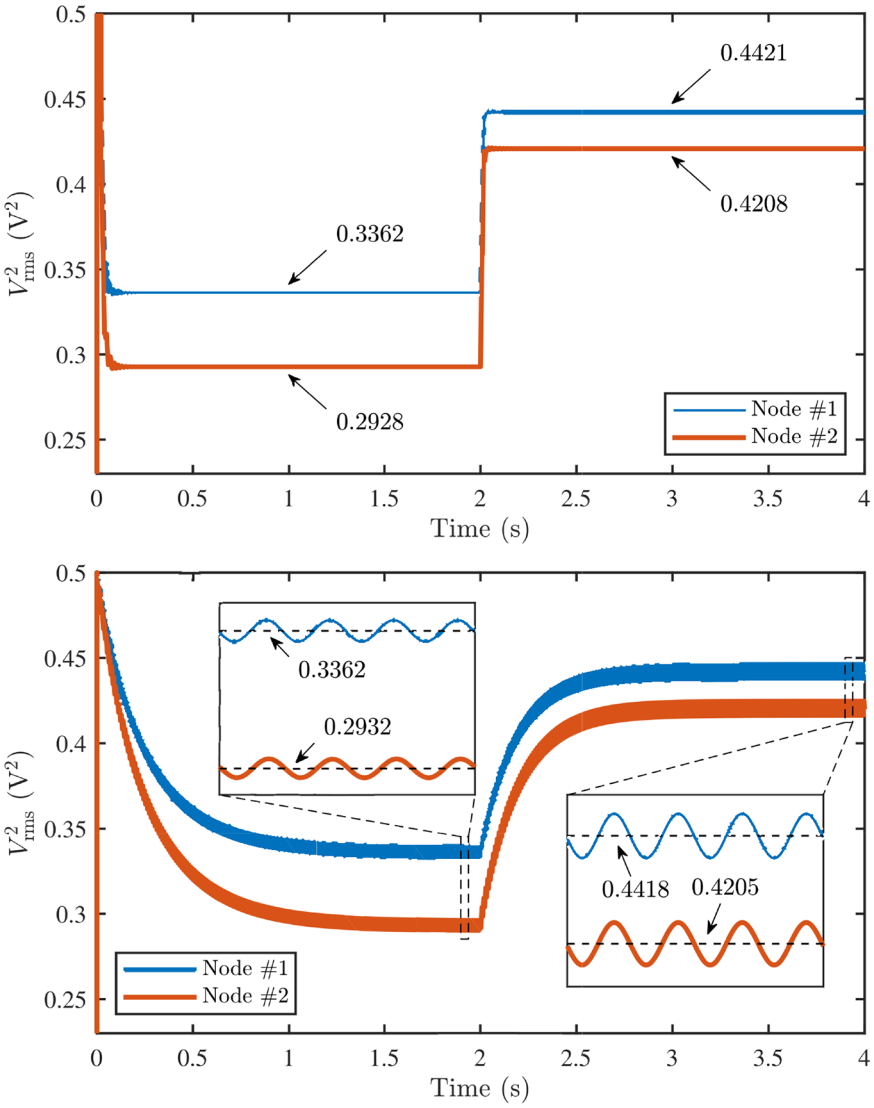

FIGURE 5 Top panel: Squared RMS node voltage detected using the circuit of Figure 2. The circuit is able to track the RMS value in just one period. Bottom panel: Squared RMS node voltage detected using the circuit of Figure 3. The output oscillates around the correct RMS value.

the tracking time is slower and the RMS value exhibits a ripple around the correct value, as is better appreciated from the insets. The ripple is 1% of the DC value, since the cut-off frequency was designed to yield an attenuation of 40 dB at $2f_0$. Despite the reduced efficiency of this alternative RMS detector circuit, the tracking time is still within the reasonable rate of variation that can be expected in a realistic scenario.

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To assess the impact of the filter order on the detection performance, the analysis is repeated by replacing the simple RC filter with a fifth-order Butterworth filter. The filter is designed to have a cut-off frequency of 10 Hz, again as a trade-off between the tracking speed and the rejection of the 100 Hz component. Indeed, this choice yields an attenuation of 100 dB at 100 Hz, while resulting in a step response that reaches the steady-state in about 0.5 s. Figure 6 compares the results for the two RMS values obtained by using the RC filter (solid blue and red lines, already shown in Figure 5) and the Butterworth filter (dashed and dotted black lines). Despite a richer dynamical behavior in the first transient, the detector with the Butterworth filter reaches a steady RMS value quicker than the one using the RC filter, while not exhibiting any visible ripple. Moreover, as indicated in the insets, the achieved RMS value is closer to the one obtained with the detector of Figure 2 (cfr. the top panel of Figure 5).

Finally, Figure 7 provides the behavior of the node voltages for the entire transient simulation obtained using the RMS detector of Figure 3A. The load switching occurring at $t = 2$ s is clearly visible in the behavior of the node voltages. The inset provides a close-up of the steady-state solutions in the first loading condition. The results obtained using the RMS detector of Figure 2 (dashed black lines) and of Figure 3B using the fifth-order Butterworth filter (magenta markers) are also included in the inset, showing no appreciable difference. The voltage amplitudes are consistent with the magnitude of the phasor solution obtained from the AC simulation and reported in Table 1. This comparison shows that the various implementations of the RMS detector yield similar accuracy on the steady-state node voltages.

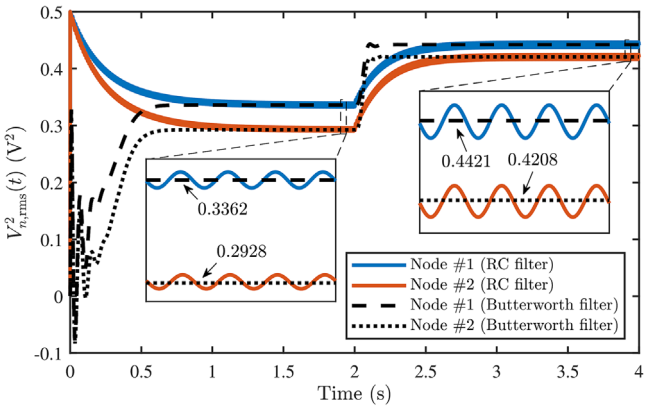

FIGURE 6 Comparison between the squared RMS node voltage detected via the circuit of Figure 3 using the RC filter (solid blue and red lines) and a fifth-order Butterworth filter (dashed and dotted black lines).

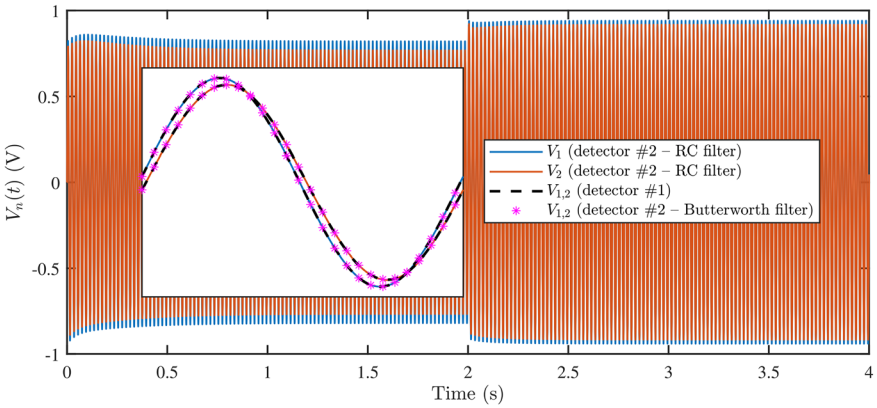

FIGURE 7 Transient node voltages obtained using the behavioral load models of Figure 1 in conjunction with the RMS detector of Figure 3. Inset: close-up of the steady-state solution obtained using the RMS detector of Figure 3A (solid colored lines), of Figure 2 (dashed black lines), and of Figure 3B with the fifth-order Butterworth filter (magenta markers).

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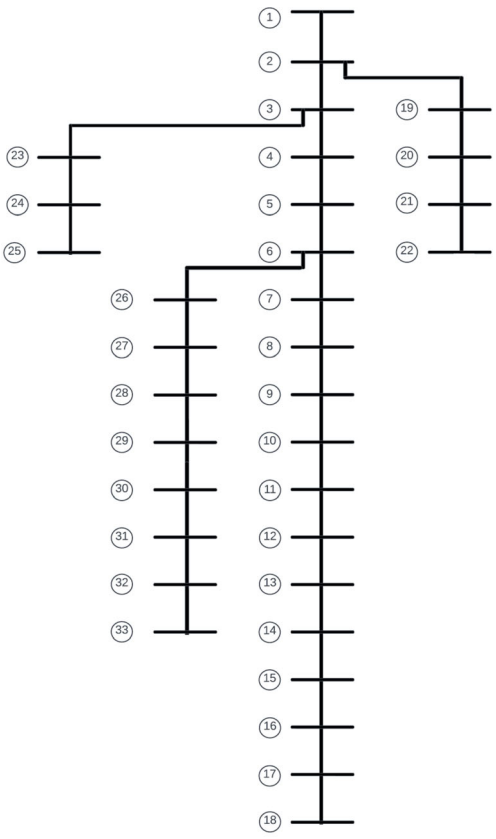
3.2 | 33-node IEEE benchmark

As a second and more realistic test case, the 33-node power distribution network from the IEEE benchmarks, illustrated in Figure 8, is considered.[18–21] It is a representative 10 MW single-phase power distribution network with radial topology, having 33 nodes and 32 branch connections. The base voltage is 12.66 kV, while the total load connected is 3.7 MW. This network has been considered by many authors, serving as a viable example providing the initial validation of alternate power analysis techniques.



Load absorbed power $P + jQ$

Bus	P [kW]	Q [kvar]
1	0	0
2	100	60
3	90	40
4	120	80
5	60	30
6	60	20
7	200	100
8	200	100
9	60	20
10	60	20
11	45	30
12	60	35
13	60	35
14	120	80
15	60	10
16	60	20
17	60	20
18	90	40
19	90	40
20	90	40
21	90	40
22	90	40
23	90	50
24	420	200
25	420	200
26	60	25
27	60	25
28	60	20
29	120	70
30	200	600
31	150	70
32	210	100
33	60	40

Branch impedance $R + jX$

Bus i	Bus j	R [Ohm]	X [Ohm]
1	2	0,0922	0,0477
2	3	0,4930	0,2511
3	4	0,3660	0,1864
4	5	0,3811	0,1941
5	6	0,8190	0,7070
6	7	0,1872	0,6188
7	8	1,7114	1,2351
8	9	1,0300	0,7400
9	10	1,0400	0,7400
10	11	0,1966	0,0650
11	12	0,3744	0,1238
12	13	1,4680	1,1550
13	14	0,5416	0,7129
14	15	0,5910	0,5260
15	16	0,7463	0,5450
16	17	1,2890	1,7210
17	18	0,7320	0,5740
2	19	0,1640	0,1565
19	20	1,5042	1,3554
20	21	0,4095	0,4784
21	22	0,7089	0,9373
3	23	0,4512	0,3083
23	24	0,8980	0,7091
24	25	0,8960	0,7011
6	26	0,2030	0,1034
26	27	0,2842	0,1447
27	28	1,0590	0,9337
28	29	0,8042	0,7006
29	30	0,5075	0,2585
30	31	0,9744	0,9630
31	32	0,3105	0,3619
32	33	0,3410	0,5302

FIGURE 8 Schematic of the IEEE 33-node power distribution benchmark with information about the lumped impedance of the transmission line branches along with the absorbed power at the different nodes/buses.

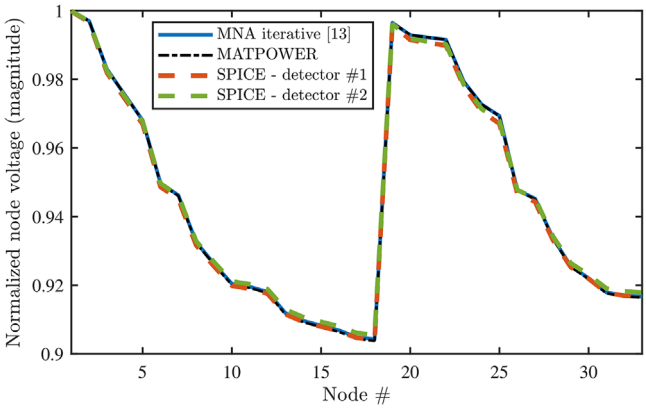


FIGURE 9 Voltage profile of the 33-node IEEE benchmark. Solid blue and dash-dotted black lines: reference results obtained with the iterative method in Memon et al. [17] and MATPOWER, respectively; dashed red and green lines: results obtained with the proposed SPICE simulation using the RMS detector circuits of Figure 2 and Figure 3A, respectively.

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Figure 9 shows the cross-comparison between the proposed approach using the two implementations of the RMS detector circuits (dashed red and green lines, the latter obtained using the RC filter) and two reference solutions computed, for the same test case, by means of the iterative MNA-based method in Memon et al,[17] implemented in MATLAB (solid blue line), and MATPOWER[13] (dash-dotted black line). The voltage profile in the figure corresponds to the amplitude of the steady-state nodal voltages, normalized to the base voltage. Both SPICE results compare well with the reference solutions, with maximum discrepancies below 2.5 milliunits. The goodness of the fit of the SPICE results in comparison with MATPOWER is further assessed statistically based on a parametric two-sample t-test and a nonparametric Wilcoxon rank sum test (also known as Mann–Whitney U-test). Both tests accept the null hypothesis with a confidence level of 5%, respectively, yielding p-values of 0.9441 and 0.8980 for the data obtained with the RMS detector #1 and of 0.9617 and 0.8777 for the data obtained with the RMS detector #2.

4 | SUMMARY AND CONCLUSIONS

This paper elaborated on the well-known and simple interpretation of a power distribution network in terms of a circuit in the phasor domain, in which the typical loads (either associated to end-users or distributed generators) are described in terms of the absorbed or supplied complex power. The latter feature led to some unconventional nonlinear components in the phasor domain which can be hardly processed by a classical AC analysis available in standard circuit simulators like SPICE.

With a suitable re-interpretation of the involved circuit components, this work introduced a novel simulation paradigm that bridges the gap between dedicated load flow analysis tools and general-purpose SPICE simulators. More specifically, thanks to the behavioral circuit of Figure 1 and two alternative implementations of the RMS detector circuit, a power distribution network with RL loads described in—possibly time-variant—active and reactive power are readily simulated in standard SPICE solvers. Compared with state-of-the-art approaches, which resort to dedicated solvers for load flow analysis, the proposed approach offers an alternative and flexible solution that can be made available within industry-standard SPICE solvers.

The RMS detector circuit of Figure 2 provides the advantage of a stable output voltage and rapid tracking speed. On the other hand, the RMS detector circuit of Figure 3 is "circuitally and physically sounder", although it exhibits longer tracking time and an oscillating output voltage. Nevertheless, a trade-off is established between the tracking speed and the voltage ripple. Furthermore, the oscillations can be reduced arbitrarily by suitably increasing the filter order. Both detector circuits are readily implemented in any SPICE solver, since they rely on basic elements and simple behavioral sources. While HSPICE does provide an advanced feature for embedding a delay in controlled sources (cfr. the RMS detector of Figure 2), such a delay can be readily achieved in any SPICE version using a standard ideal transmission line element. The behavioral load description of Figure 1, in which resistance and inductance values depend on node voltages, is also available in standard SPICE distributions (e.g., HSPICE, PSPICE, and LTspice).

The features of the proposed technique in terms of accuracy, efficiency, and convergence were discussed based on an illustrative example and a standard IEEE power distribution benchmark, highlighting excellent accuracy while offering enhanced simulation flexibility. In future works, to further improve the efficiency the proposed approach could be combined with periodic steady-state solvers, such as the harmonic balance or shooting methods,[22] in order to avoid any issue related to the settling time of the transient analysis (for time-invariant loads).

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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