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A Two-Way GaN Doherty Amplifier for 5G FR2 With Extended Back-Off Range

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***Abstract*— This article presents the design and experimental characterization of a two-way gallium nitride on silicon carbide (GaN-SiC) monolithic Doherty power amplifier (DPA) for deep back-off operation in the 5G FR2 band. The amplifier, including two driver stages ON-chip, achieves 35-dBm output power, 30% power-added efficiency, and 16-dB gain at saturation at 29 GHz. It favorably compares with the present state of the art, maintaining a power-added efficiency higher than 27%, 28%, and 22% at 6-, 9-, and 12-dB output power back-off, respectively.**

***Index Terms*— 5G FR2 bands, Doherty, gallium nitride, monolithic microwave integrated circuit (MMIC), power amplifier.**

I. Introduction

POWER amplifiers (PAs) are key components of modern wireless communication systems, where they serve as the workhorses responsible for amplifying signals to the required levels for transmission. One of the paramount challenges in current wireless technology is the balance between spectral and power efficiency, particularly with the advent of 5G and the emerging prospects of 6G networks on the horizon. Complex modulations are used, requiring the PA to operate in output power back-off (OBO) for a large portion of its operational time. Under such conditions, it becomes crucial to maximize the average efficiency.

The need to maximize average efficiency, particularly for OBO ranging from 9 to 12 dB [1], calls for the extension of the existing solutions, such as the 6-dB two-way Doherty power amplifier (DPA) [2], or the development of new topologies such as the load-modulated balanced amplifier (LMBA) [3], distributed efficient power amplifier (DEPA) [4], and N-way DPA [5]. Even if a few examples extend toward high frequency [6], [7], [8], the prototypes presented in the literature mainly operate in the sub-6-GHz frequency bands and are based on single-stage demonstrators, achieving gains of the overall amplifier of the order of 10 dB.

In fact, at higher frequencies, such as those in the 5G FR2, PA design becomes more complex, often necessitating multistage architectures to achieve the desired gain. Furthermore, examples that comprehensively address the extended OBO scenario in FR2 are scarce [7], [8], [9].

In this context, this article explores the development of a two-way monolithic microwave integrated circuit (MMIC) DPA developed on gallium nitride on silicon carbide (GaN-SiC) technology, tailored for deep OBO operation required by 5G applications in the FR2 bands. The fabricated amplifier favorably compares with the present state of the art, achieving at 29 GHz, 35-dBm output power, 30% PAE, and 16-dB gain at saturation, while maintaining the PAE above 27%, 28%, and 22% at 6-, 9-, and 12-dB OBO, respectively.

II. Design

The initial phase of the design involves selecting the most appropriate DPA architecture, considering both the stage composition and the corresponding active periphery. The design specifically targets the high peak-to-average power ratio (PAPR) of signals within the 5G FR2 bands. The primary objective is to enhance efficiency at deep OBO levels, ranging from 10 to 12 dB. Simultaneously, the design aims to achieve a minimum saturated output power of 35 dBm and a small signal gain of about 20 dB around 29 GHz.

The adopted MMIC technology is the 150-nm GaN-SiC high-electron-mobility transistor (HEMT) process of WIN Semiconductors, which features approximately 3 W/mm at 20 V of drain voltage.

In a DPA, the first efficiency peak corresponds to the voltage saturation of the carrier device, which occurs at a given OBO (in dB) from the saturated power of the overall DPA ($P_{\text{out,sat,DPA}}$). This can be expressed as

$$P_{\text{out,sat,DPA}} = \frac{1}{\alpha} \cdot P_{\text{out,sat},c} \tag{1}$$

where α is the OBO value in linear units and $P_{\text{out,sat},c}$ is the output power provided by the carrier at saturation. Indirectly, this implies that the larger the targeted OBO, the larger the ratio between the active peripheries of the peaking and carrier final stages. This is a crucial aspect that usually prevents achieving OBO values larger than 6 dB with a two-way DPA architecture. Indeed, if the same drain voltage is adopted [10], the peaking device (typically biased in class C) has to supply a higher fundamental output current than the carrier (biased in class AB) for OBO larger than 5 dB [11]. The ratio of the

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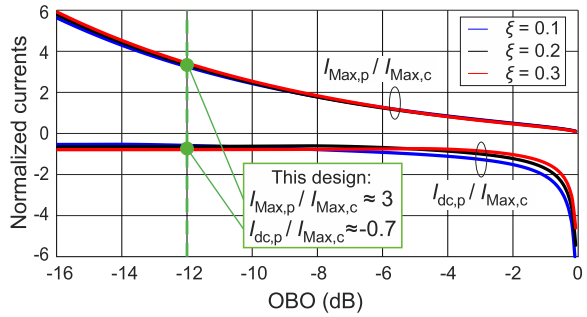


Fig. 1. Maximum current and virtual dc current [11] of the peaking device, normalized to the maximum current of the carrier, as a function of the OBO and parametrized by ξ. The OBO value is the distance in dB from $P_{\text{out,sat,DPA}}$, where the first efficiency peak of the DPA is placed.

fundamental drain currents can be expressed as

$$\alpha \cdot \left(1 + \frac{I_{1,\text{sat},p}}{I_{1,\text{sat},c}}\right) = 1 \tag{2}$$

where $I_{1,\text{sat},x}$ is the fundamental current component at saturation of peaking ($x = p$) or carrier ($x = c$) stage. Solving (2) for OBO = 12 dB, i.e., $\alpha = 0.251$, results in a ratio $I_{1,\text{sat},p}/I_{1,\text{sat},c}$ of about 3, which directly imposes that the gate periphery of the peaking stage must be at least three times larger than that of the carrier. In fact, the periphery ratio typically needs to be further increased to compensate for the lower conductive period of the class C peaking compared with the class AB carrier device [12].

This aspect is graphically shown in Fig. 1, where the ratio between the maximum currents $I_{\text{Max},p}/I_{\text{Max},c}$ is reported as a function of the OBO for different ξ values. The parameter $\xi = I_{\text{Max},c}/I_{\text{dc},c}$ estimates the class AB depth of the carrier device, i.e., $\xi = 0$ corresponds to class B, whereas $\xi = 0.5$ to class A operation. The maximum currents $I_{\text{Max},x}$ are related to the corresponding $I_{1,\text{sat},x}$ as detailed in [12]. At the same time, the deeper the OBO at which efficiency enhancement is sought, the sooner the peaking device should start conducting, and thus the shallower its class C bias point, as shown in Fig. 1, where the ratio between the "virtual" bias current of the peaking device ($I_{\text{dc},p}$) [11] and the maximum current of the carrier device is also reported.

Taking into account the power density of the selected technology and the performance targets, including a margin of 1 dB in the output power to account for the unavoidable losses of the output combiner, the minimum gate peripheries of carrier and peaking devices result in 335 μm and 1 mm, respectively. For the carrier, the active device with the closest size, for which the nonlinear foundry model is validated, is the 4 × 75 μm. For the peaking amplifier, the parallel combination of two 6 × 100 μm devices was preferred to a single device solution since it provides higher gain, reduces parasitics, and simplifies the synthesis of the output combiner. Furthermore, it permits the adoption of the nonlinear model for device peripheries fully validated by the foundry and requiring no data extrapolation. The drivers and predriver sizes are determined by the gain of the devices in the final stage. In particular, a 2 × 75 μm and a 4 × 75 μm devices were adopted to drive the final stages of the carrier and peaking, respectively, whereas a single 2 × 75 μm is used as predriver

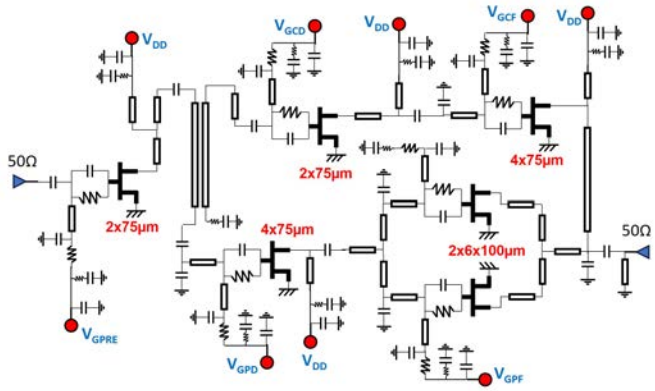


Fig. 2. Schematic of the implemented DPA.

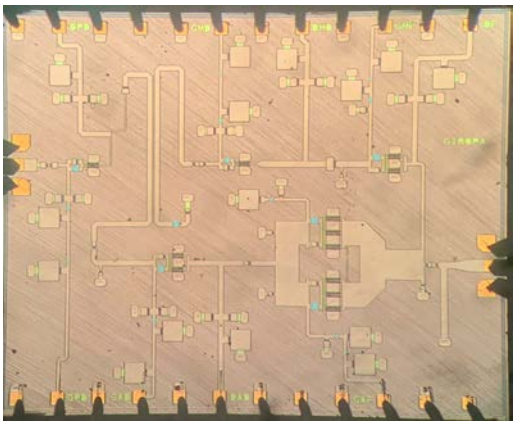


Fig. 3. Microscope photograph of the realized DPA.

in front of the splitter. The electric scheme of the overall DPA is shown in Fig. 2.

The output combiner was implemented following the scheme proposed in [13], in which the parasitic elements of the devices were embedded in the structure as in [9]. The transformation from the standard 50-Ω termination to the optimum impedance at the common node of the DPA (10 Ω) was carried out through a semi-distributed postmatching network realized by a C-L network. The matching networks between the final and driver stages were synthesized with the aim of maximizing the available gain while carefully achieving the optimal power driving both at saturation and in back-off. After amplification by the single predriver, the input power is split between the carrier and peaking branches through an unbalanced coupled-lines divider, delivering 60% of the power to the peaking and 40% to the carrier path. The coupled-line topology was selected because of its rather large bandwidth and good isolation between the branches, as well as the recovery of the 90° phase shift introduced by the output section. The photograph of the realized chip, whose area is 3.8 × 3.1 mm^2, is shown in Fig. 3.

III. Experimental Characterization

The manufactured two-way DPA has been characterized using continuous wave (CW) and modulated signals, at the nominal bias point: $V_{\text{DD}} = 20$ V for all the devices, $V_{\text{G}_{\text{PRE}}} = -1.4$ V, $V_{\text{G}_{C,D}} = V_{\text{G}_{C,F}} = -1.7$ V, $V_{\text{G}_{P,D}} = -2.6$ V, and $V_{\text{G}_{P,F}} = -2.1$ V, corresponding to an overall quiescent drain

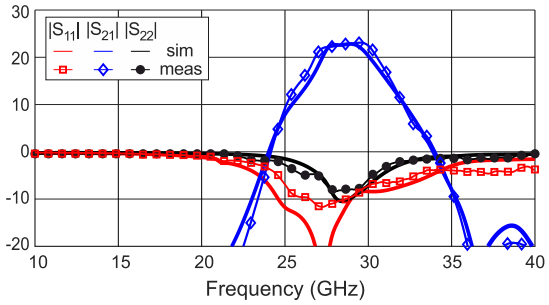


Fig. 4. Simulated (solid) and measured (symbols) scattering parameters.

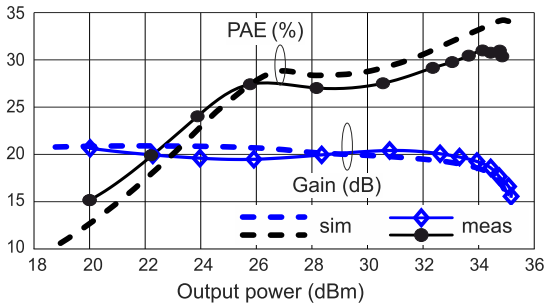


Fig. 5. Simulated (dashed) and measured (solid with symbols) CW gain and PAE versus output power at 29 GHz.

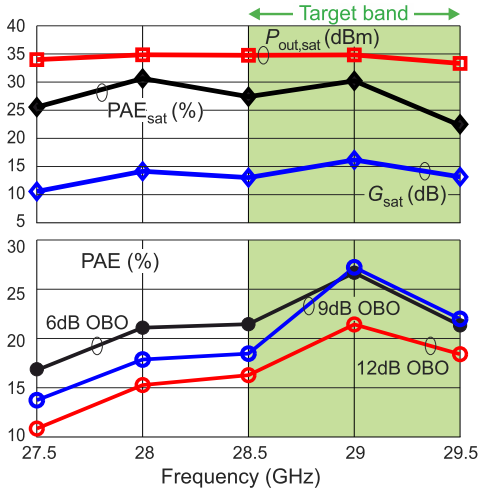


Fig. 6. Measured CW performance versus frequency: output power, gain, and PAE at saturation (top) and PAE at 6-, 9-, and 12-dB OBO (bottom).

current $I_{D,\text{tot}} = 17$ mA. Fig. 4 reports the good agreement between the simulated and measured scattering parameters in the 10–40-GHz range.

Fig. 5 shows a good agreement between the measured and simulated CW power sweep at 29 GHz. The saturated output power is 35 dBm, with associated PAE and gain in excess of 30% and 16 dB, respectively. Notably, the Doherty efficiency curve is very pronounced with two distinct peaks, showing PAE higher than 25% over 10 dB of the OBO dynamic.

Fig. 6 presents the CW performance versus frequency, demonstrating the effectiveness of the asymmetric Doherty architecture in improving the back-off efficiency performance.

Fig. 7 shows the performance at 29 GHz under a 5G FR2 64-quadrature amplitude modulation (QAM) standard signal excitation (10-dB PAPR, 50-MHz bandwidth), without the assistance of digital predistortion. The DPA shows good

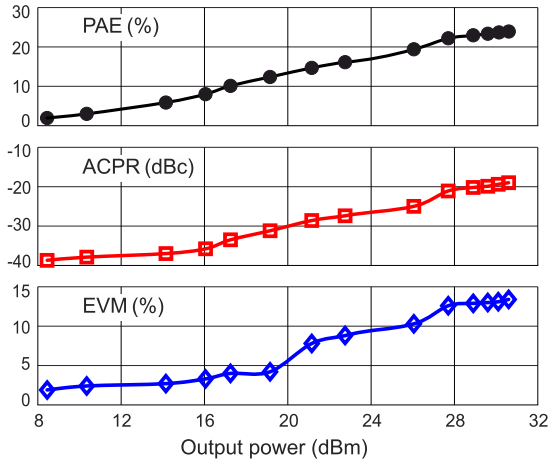


Fig. 7. Measured PAE, ACPR, and EVM versus average output power at 29 GHz (5G NR signal: 64-QAM, 50-MHz bandwidth, 10-dB PAPR).

TABLE I
STATE-OF-THE-ART *K*a-BAND DPAS

Tech.	Freq. (GHz)	$P_{out,sat}$ (dBm)	PAE sat (%)	PAE 6 dB (%)	PAE 12 dB (%)	G_{sat} (dB)	Ref.
CMOS	28	22.4	30*	28	15*	5*	[14]
CMOS	26	18.7	32*	15*	5*	12.5*	[15]
CMOS	27	18.8	30	22	10*	10*	[16]
GaAs	27.2–29.8	27	37	25	10*	14*	[17]
GaN	27–29	39	25	21	-	-	[18]
GaN	29	30	40	28*	20*	6	[19]
GaN	29	34	20	13	13	8	[9]
GaN	**28–29.5**	**34.6**	**24**	**21**	**15**	**13**	**T.W.**
	29	**35**	**30**	**27**	**22**	**16**	

* value inferred from graphs

inherent linearity in terms of adjacent channel power ratio (ACPR) and error vector magnitude (EVM), resulting in ACPR < -25 dBc and EVM $< 10\%$ up to an average output power of 26 dBm, and only degrades in strong compression.

The performance of the DPA is compared with the state-of-the-art in Table I. The realized chip demonstrates competitive saturated performance while achieving at 29 GHz the highest PAE at 12-dB OBO. The results prove to be competitive over a 1-GHz band, especially in terms of efficiency at deep back-off.

IV. Conclusion

In this letter, we have presented a GaN-SiC MMIC two-way DPA for deep back-off operation in the 5G FR2 band. The characterization of the realized amplifier demonstrates outstanding performance which challenges the current state of the art, with a saturated output power of 35 dBm, and the corresponding PAE and gain of 30% and 16 dB, respectively. Furthermore, the DPA shows excellent back-off PAE, higher than 27% up to 9 dB and higher than 22% at 12-dB OBO.

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