HIL Investigation of a Single-Phase Inverter for a Tokamak Non-Axisymmetric In-Vessel Coil Power Supply

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***Abstract*—This paper deals with a single-phase inverter topology evaluation for a non-axisymmetric in-vessel coil system in a tokamak. An IGBT-based power converter topology is investigated to supply the magnetic system composed of several independent coils. The dc-ac converter topology used for a single coil consists of a single-phase inverter with an interleaved leg and unfolding switching strategy. The converter operation and control investigation are carried out with a Hardware-in-the-Loop (HIL) approach. In the paper, the main control design requests and the issues of this application are explored. Then, the effectiveness of the proposed approach is validated by the HIL. Furthermore, the selection criteria for the power switches are discussed.**

***Index Terms*— Non-axisymmetric coil power supply, Divertor Tokamak Test (DTT), single-phase inverter, interleaved strategy, unfolder switch, IGBT**

I. INTRODUCTION

Nowadays, nuclear fusion energy is one of the greatest challenges in worldwide research [1]-[2]. Several international research projects, some developed also on an industrial scale [3], are involved in designing and operating a structure able to actually generate energy by nuclear fusion [1]-[2]. In the most promising ones, known as "tokamaks", a plasma is magnetically confined in a toroidal shape to achieve high rates of fusion reactions. However, many technological issues have to be solved to reach and maintain the requested operative conditions. For instance, the management of the large power flows produced by the plasma exhaust is still an open issue for the realization of DEMO, the reactor that according to the European Roadmap is expected to produce electricity from nuclear fusion around 2050 [2], [4], [5].

The Divertor Tokamak Test (DTT) project, under construction in the ENEA (Italian agency for new technologies, energy and the environment) Research Center in Frascati, Italy, aims to create an experimental facility to investigate and solve some of the most complex problems on the implementation path of nuclear fusion as an energy source [6]-[7]. Specifically, DTT was conceived as a "link" between the large international nuclear fusion projects ITER (International Thermonuclear Experimental Reactor) and DEMO (DEMOnstration Power Plant), to provide scientific and technological answers to major problems, such as the management of the plasma exhaust and the materials to be used [6]. In fact, the facility is named after the "divertor", which is part of a tokamak devoted to such management.

In order to investigate the previous problems in a relevant environment, DTT is designed to achieve a plasma current up to 5.5 MA with a magnetic field of 6 T and coupling to the plasma up to 45 MW of additional heating [6].

The DTT magnetic system includes several coils necessary to create and control the plasma current [8]-[9]. A dedicated power converter topology supplies every coil, feeding the high current requested at different voltage levels [8].

Most of the coils are symmetric with respect to the tokamak axis, but some "non-axisymmetric" (NAS) coils are necessary to address some tokamak non idealities and instabilities [10]-[15]. Such coils and their power supply system are characterized by specific requirements and problems [8]. In DTT, the NAS coils are installed inside the vacuum vessel after its assembly for better effectiveness, as sketched in Fig. 1. The system assembly was based on rows of 9 coil columns and moved from 2 rows, corresponding to 2×9=18 NAS coils, to 3 rows, corresponding to 3×9=27 NAS coils [12]. Each coil shall be independently supplied, as shown in the global block schematic of Fig. 2.

This paper discusses the power supply system for the DTT NAS coils. The topology solution is evaluated to optimize the current and voltage requests. In this paper, the following items are explored: the general problem, the full-bridge inverter topology selection for a single NAS coil, the feature request to the power switches. The power converter operation is validated through a Hardware-in-the-Loop (HIL) approach, enabling to test the digital implementation of the proposed modulation strategy.

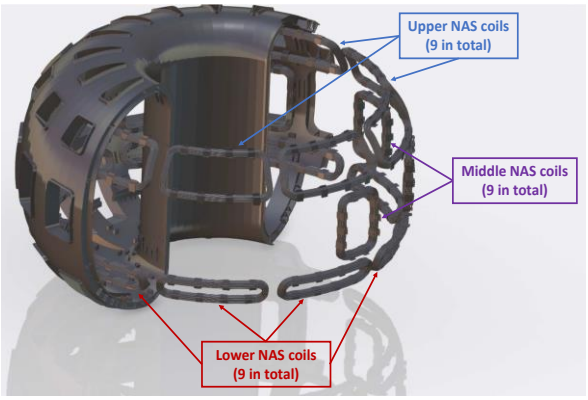

Fig. 1 Arrangement of the DTT NAS coils inside the vacuum vessel. The final configuration includes 3×9=27 NAS coils in total.

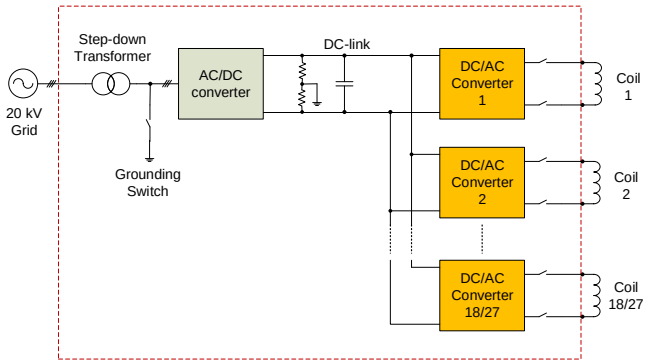

Fig. 2 Block schematic of the multi-converter power supply for the DTT NAS coils.

TABLE I
MAIN REQUIREMENTS OF THE DTT NAS POWER SUPPLY SYSTEM

Characteristic	Value
Number of independent output converters	18/27
Operations	4 quadrants
Load inductance	<1 mH
Load resistance	<20 mΩ
Maximum current	±1500 A
Maximum voltage on the load (dc bus)	±400 V
Sinusoidal current bandwidth at -1 dB	7 Hz
Maximum duration of a NAS operation	100 s
Time between two successive NAS operations	3600 s

II. NAS SYSTEM DESIGN ISSUES

A. NAS Coil Functions

The NAS coils are necessary to address two classes of phenomena:

1. The actual magnetic configuration produced by the tokamak structure and coils may differ from the theoretical predictions due to unavoidable uncertainties in a phase of construction or assembly. These uncertainties can be modelled as error fields (EFs) that must be corrected [11]-[12].
2. The stability of the plasma is a crucial matter to maintain the operative conditions. Particularly critical instabilities, known as edge-localized modes (ELMs), can occur in the edge area of the plasma [13]-[15]. These modes involve periodic bursts expelling particles and large heat energy that could damage the tokamak vessel and the divertor. The most successful method to mitigate or suppress ELMs consists in introducing NAS perturbations of the magnetic field. The intensity and the periodicity of such perturbations must be coherent with the undesired ELMs, otherwise, such ELMs may be even amplified.

The NAS coil power supply system must implement EF correction and ELM control at the same time. This is practically achievable because:

1. EFs are normally corrected by the dc component in the coil currents.
2. The desired action on ELMs is achieved by AC components in the coil currents.

These two actions must be independent and accurate. Excessive ripple or harmonic content can amplify oscillation and instabilities. A bad application of the NAS fields can produce detrimental effects on the plasma, even worse than the absence of NAS coils [15]. This is particularly critical for the NAS system, whereas for other tokamak coils the high inductance and the vessel effect can mitigate the ripple, the harmonics and some undesired oscillations [12].

Despite of being designed and procured as a single system, as the actions must be as local as possible, the current flowing in each of the NAS coils is independently fed by a specific power supply [12].

Due to the space constraints, the coils are not evenly distributed and have different shapes and consequently different inductances, resistances, and effects on the plasma. Moreover, the tokamak structure and the plasma configuration introduce an equivalent load that is not limited to the coil winding [12].

B. NAS Power Supply Requirements

The design requirements for every single NAS coil are provided in Table I. Given the high current demands (i.e., ±1500 A) and the relatively low output frequency (i.e., 7 Hz), cycloconverter topologies may be a suitable choice.

However, in preventing disruption currents [8], the dynamic response of cycloconverters can be slower compared to that of PWM inverters [16], while the available rated currents of PWM inverter components can require parallel connections of switches or inverter legs.

Therefore, the power supply system consists of two power conversion stages, as shown in Fig. 1:

1. An ac/dc controlled rectifier fed by step-down transformer.
2. The dc/ac converters (inverters) powering each NAS coil.

Powering each coil with a dedicated converter is a design requirement of the Tokamak system for optimal plasma management. To optimize the size of the ac/dc stage, its components are designed to support all the inverters simultaneously operating at half of the rated output current, corresponding to a power of 5.4 MW. The resulting design is rather standard and is not addressed in this paper for the sake of brevity, while the design of inverters is fully developed in the following.

The design constraints for every single inverter (called n) are summarized in Table I. The key design constraints of the switching pole (see Fig. 3) in an inverter standard topology using are:

- The correct selection of the switches for the switching legs.
- The loop inductance minimization in power switching legs and driver circuits to improve the overall system performance.

- The thermal management optimization.

The nominal DC bus voltage is 400 V, but this value can transiently increase up to 500-550 V, therefore a sufficient safety margin must be considered when selecting power switches.

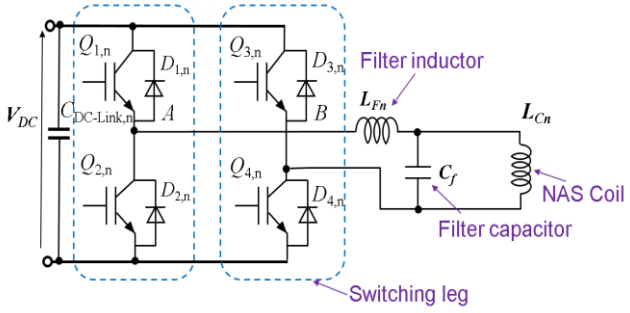

Fig. 3 Standard inverter topology with IGBTs for the DTT NAS coil power supply.

III. Full-Bridge Inverter Topology Selection

The high current requested by the NAS coils (±1500 A) requires the paralleling of switching legs. In Fig. 4, two different solutions of paralleling are shown.

For the first solution, shown in Fig. 4a, adopts synchronous commutation. The second solution, shown in Fig. 4b, uses interleaving [17]. The command signals of the switches generated by the modulation strategy are supplied to each switching leg with a phase shift (PS) with respect to the other legs as:

$$\mathrm{PS} = \frac{360}{N_C}\,(\text{degrees}) \qquad (1)$$

where N_C is the number of legs.

Besides the power sharing that allows the use of power modules with reduced rated current [18], [19], the interleaving has the advantage of providing a multilevel output voltage with an equivalent frequency that is N_C times higher than the switching frequency of the single leg.

The increase of the frequency of the output voltage is beneficial for an eventual output filter to yield nearly sinusoidal coil supply voltage. This is very important to reduce the electromagnetic interference (EMI) effects on the coil, especially because the coils need very long supply cables.

A. *Inverter topology with interleaving legs and unfolding leg*

The inverter using interleaving legs from Fig. 4b has the disadvantage of high switching losses due to the high number of switching legs. To reduce the switching losses, this paper proposes the solution reported in Fig. 5, consisting of an inverter with multiple legs operating in interleaving and an unfolding leg. The unfolding leg is working at the fundamental output frequency (7 Hz), so its switching losses are negligible.

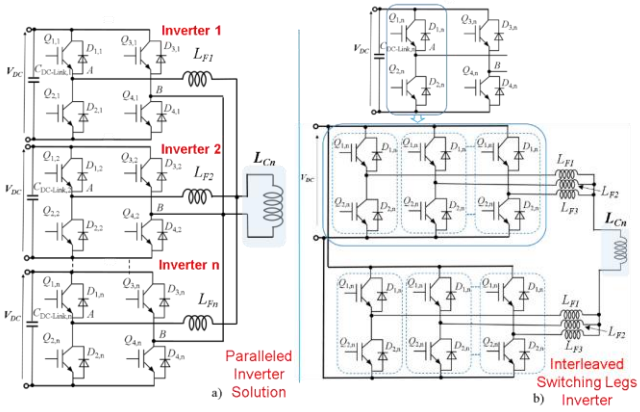

Fig. 4 (a) Parallel inverter topology (b) Interleaved switching leg inverter circuit.

Therefore, the unfolding leg can use a single switch with high-rated current or an equivalent switch that is obtained with multiple paralleled devices.

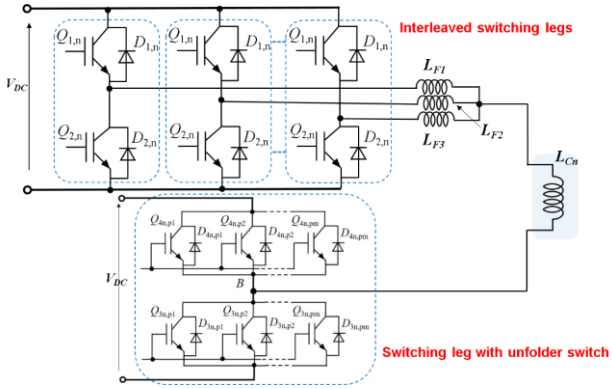

Fig. 5 Single-phase inverter topology with interleaved switching pole and unfolder switching leg.

The waveforms of the modulation strategy for both the interleaved switching legs and the unfolder switching leg are shown in Fig. 6.

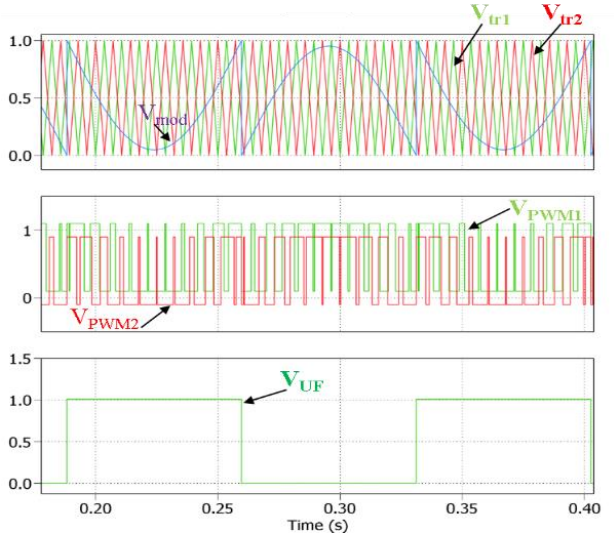

Fig. 6 Modulation strategy for two interleaved switching legs and the unfolder leg (PLECS® simulation).

For the sake of simplicity, two switching legs are considered in

the interleaved half-bridge and a low carrier frequency of 140 Hz (V_{tr1} and V_{tr2}) is used for the PWM. Thus, the PS according to (2) results in 180°. Fig. 6 reports the modulation voltage V_{mod} together with the triangular carrier signals and the resulting PWM signals (V_{PWM1} and V_{PWM2}) with the unfolder command signal. In the unfolder switching leg, there is a strong reduction of the switching losses while practically only the conduction losses remain for the entire working cycle. Thus, the choice of the devices that make up the switching legs of the inverter is crucial.

IV. Power Switches Selection Criteria

The dc/ac converter design constraints lead to selecting switching power devices considering the technology nowadays available. The chosen devices' breakdown voltage constraint must consider the voltage peak due to the stray inductances caused by the power loop layout arrangement and the contribution of the package parasitic inductances [20]. A maximum voltage with a safe margin of at least twice the dc bus voltage (maximum dc bus voltage can transiently rise up to 550 V) is considered. Thus, the power devices' breakdown voltage should be 1200 V. The interleaved switching legs share a current of 1500 A. Considering a safe margin S=1.5, the maximum shared current I_{Lmax} is higher than 2250 A. The number of switching legs to obtain the interleaved switching pole depends on the trade-off between the load inductive current ripple required and the maximum current for a single switching leg considered. A power module for the power devices arrangement is the correct choice for the application considered. Other design constraints regard the module architecture.

- A half-bridge arrangement is required for the compact construction of the modular power converter.
- Integrated temperature sensors for accessible temperature monitoring are preferrable.
- Viable thermal management should be taken into account.
- Reliability (i.e. technology maturity, short circuit withstand capability, and so on)
- Market availability (i.e. off the shelf solutions that are widely available on the market should be preferred)

The driving and protection circuits also play a crucial role in choosing usable power devices [21]. The interleaved switching pole strategy allows using a lower f_{sw} for each leg [22]. In the converter design evaluation, a f_{sw} of 4 kHz is considered. Two kinds of technology can be evaluated: silicon carbide (SiC) MOSFETs or silicon (Si) IGBTs [[23]. The SiC MOSFETs feature high f_{sw} and higher junction temperature than Si IGBTs. On the other hand, IGBTs modules, although slower in switching, show a higher current capability and a higher technological maturity. From the converter design constraints, the rated current of the power modules in the interleaved arrangement must be in the range of 400-800 A to maintain N_C to 4-6. Preference is given to power devices with a minimum breakdown voltage of 1200 V, even though this value surpasses the requirements of the dc bus. Devices with lower breakdown voltage (V_{BRD}=600-650 V), on the other hand, lack a sufficient safety margin during switching transients, particularly considering the peak dc bus voltage of 550 V, as outlined in Section II, Subsection B. A SiC MOSFET power module characteristics compared with two similar Si IGBTs power modules in a half-bridge configuration are investigated to select the application-oriented effective solution. The parameters are compared at the maximum temperature declared (150 °C for SiC MOSFET while 175 °C and 150 °C for the Si IGBT with I_{max}=800 A). From the inspection of Table II, the better dynamic performance and energy switching loss savings of SiC MOSFET are clear. However, the lower current I_{max} of SiC MOSFET increases the number of switching legs necessary (N_C=6), with the occupied volume and cost growth. Using 600 A Si IGBT is a viable trade-off among the number of switching legs necessary (N_C=4), costs, and quite satisfying switching performance. Both semiconductor technologies are well suited to the application, with SiC devices enabling the achievement of reduced switching losses. However, due to the low switching frequency requirements of the application (i.e., 4 kHz), the benefits introduced by using a wide bandgap solution are not noticeable. Whereas IGBT technology features a higher level of technology maturity, lower cost, and higher short-circuit withstand time (TSC) [24]. A second important benefit of SiC technology is the high efficiency at low loads due to the purely resistive behavior (i.e., no threshold conduction voltage). However, in this specific application, the converter must always work under nominal load conditions. Following this consideration, IGBT technology is selected. In Fig. 7, the arrangement of the interleaved switching pole with 4 Si IGBT power modules is shown.

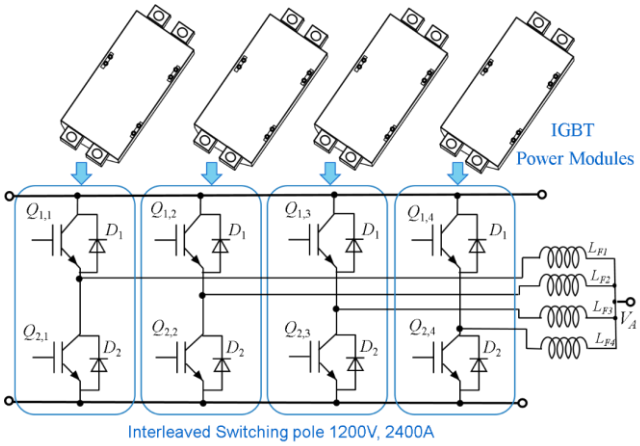

Fig. 7 Interleaved switching pole with 4 switching legs for the arrangement of the single-phase inverter.

TABLE II
MAIN POWER MODULES PARAMETERS

Parameter	Switching Leg V_{BRD}=1200 V		
	SiC MOSFET I_{nom}=541 A CAB530M12 BM3	**Si IGBT I_{nom}=600 A FF600R12ME7 _B11**	**Si IGBT I_{nom}=800 A CM800DX-24T1**
Nominal current	541 A @ T_{case}=90 °C	600 A @ T_{case}=85 °C	800 A @ T_{case}=90 °C

Parameter	Switching Leg V_{BRD}=1200 V		
	SiC MOSFET I_{nom}=541 A CAB530M12 BM3	**Si IGBT I_{nom}=600 A FF600R12ME7 _B11**	**Si IGBT I_{nom}=800 A CM800DX-24T1**
Pulse current	1060 A @ T_J=25 °C	1200 A @ tp=1 ms	1600 A @ T_J = 175 °C
$R_{DS,on}$/V_{CEsat}	2.67 mΩ @V_{GS} = 15 V @I_C=530 A @ T_J=150 °C	1.75 V @V_{GS}=15 V @I_C=600 A @T_J = 175 °C	2.05 V @V_{GS}=15V @I_C=800 A, @T_J=150 °C
Gate Charge Q_G	1.36 µC	9.6 µC	4.5 µC
E_{on}/E_{off}	16.1/14.9 mJ @ 150 °C	58/95.5 mJ @ 175 °C	80/ 84 mJ @ 175 °C
Diode: V_F	5 V @ 150 °C @ 530 A	1.60 V @ 175 °C @ 600 A	1.80 V @ 150 °C @ 800 A
Diode: Q_{rr}	8.5 µC	108 µC	80 µC
$R_{th,JC}$	0.065 K/W	0.0721 K/W	0.043 K/W
T_{SC} Short-Circuit time	5 µs	10 µs	10 µs
Package size	61 × 106 × 30 mm	152 × 62 × 20 mm	152 × 62 × 14 mm

TABLE III
MAIN PARAMETERS OF UNFOLDER SWITCH

Parameters	Si IGBT single switch power module V_{BRD}=1700 V FZ2400R17HP4_B29
Nominal current I_{Cn}	2400 A @ 100 °C
Pulse current I_{CRM}	4800 A t_p=1 ms
$V_{CE,sat}$	2.35 V @ 125 °C
Diode V_F	1.9 V

In the unfolder arrangement (Fig. 5), the switching leg operates at output frequency according to Fig. 6. The choice of Si IGBT is even more meaningful. In this case, the half-bridge operation is performed by a single unfolder switch module operating on the up and the low side of the switching leg [25]. The maximum coil current I_{Lmax} gives the total rated current requirement. The single switch selection in module arrangement is related to the market availability. The main parameters of the selected single-switch power module are reported in Table III.

V. SIMULATION RESULTS

The Full-Bridge topology with the interleaving solution and unfolder switching leg (Fig. 5) proposed for the NAS current supply is validated by arranging a single-phase inverter in the PLECS® tool [26]. PLECS® (Piecewise-Linear Electrical Circuit Simulation) is a software tool developed by Plexim for the simulation and analysis of electrical circuits. It is specifically designed for power electronics systems and is widely used in industries and academia for the design and testing of power electronic circuits and control systems. The global block schematic of the simulated circuit is reported in Fig. 8. The inverter topology simulation schematic is composed of the 4 legs of the interleaved switching pole and the unfolder switching leg, as described in the simulation schematic of Fig. 9. The IGBT model available in the PLECS® library is used with the parameters based on the selected actual power module devices to arrange the switching legs.

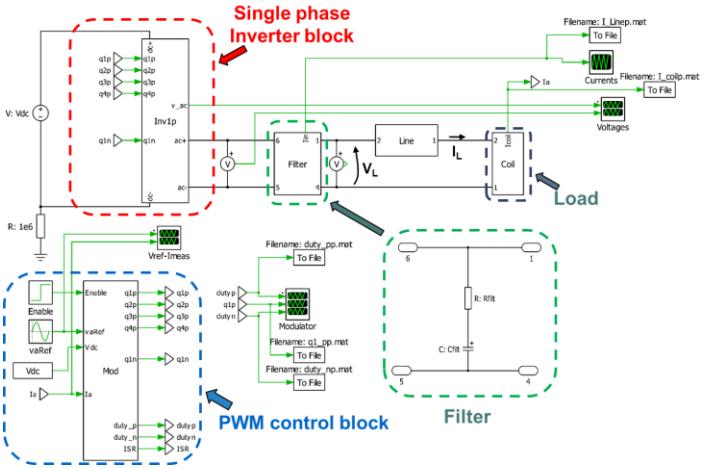

Fig. 8 Block schematic of the global supply system for the single NAS coil used in PLECS® simulation runs.

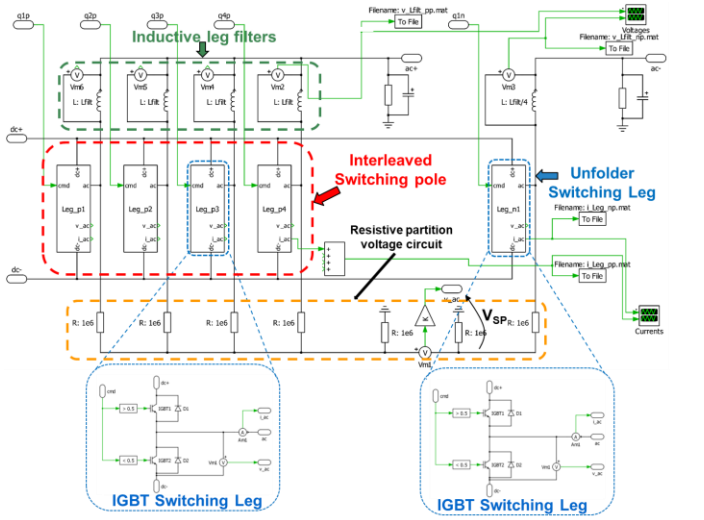

Fig. 9 Block schematic of the single-phase inverter topology with an interleaved switching pole and unfolder switching leg used in PLECS® simulation runs.

The voltage V_{SP} obtained with the 4 legs of the switching pole without the filter inductances (shown in Fig. 9, but replaced by short circuits) is shown in Fig. 10a. This voltage has the same waveform as that obtained using the resistive voltage partition network shown in Fig. 9 (named V_{SP}). As can be seen in Fig. 10a), there are 4 levels of positive voltage and 4 of negative voltage due to the chosen N_C and to the unfolder strategy (the modulation command is like the one shown in Fig. 6). The commutation of the unfolder switching leg determines the change of sign of the inverter output voltage. The actual output voltage with the inserted filter inductances is shown in Fig. 10b. The voltage V_L respects the design constraints (400 V output frequency of 7 Hz) with negligible voltage ripple due to the RC filter with a cutoff frequency of 530 Hz.

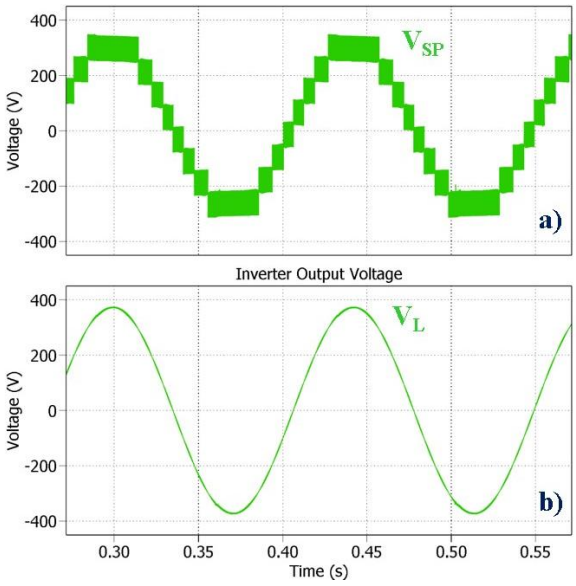

Fig. 10 Output voltage of the single-phase inverter without filter (a) and with the RC filter (b).

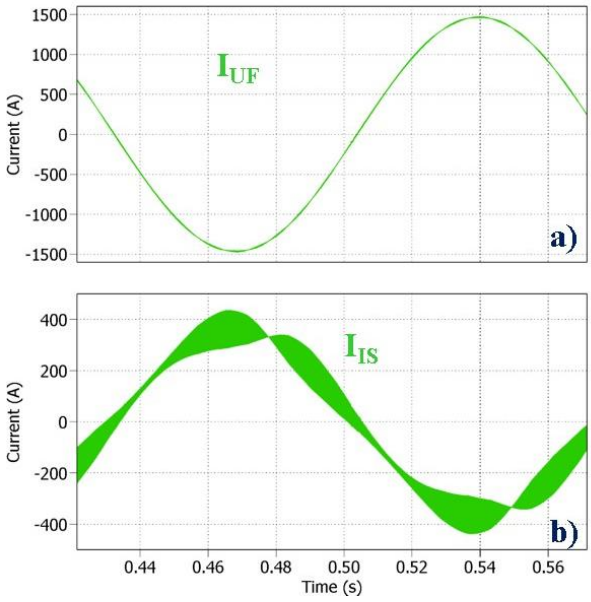

Fig. 11 Single phase inverter current. a) output current of the unfolder switching leg (I_{UF}). b) output current of a single switching leg of the interleaved switching pole (I_{IS}).

The current waveform output of the unfolder switching leg is reported in Fig. 11a. The current of a single leg of the interleaved switching pole is shown in Fig. 11b. As it can be seen in Fig. 11b the current is a quarter of the total load current I_L. The load current I_L is shown in Fig. 12a.

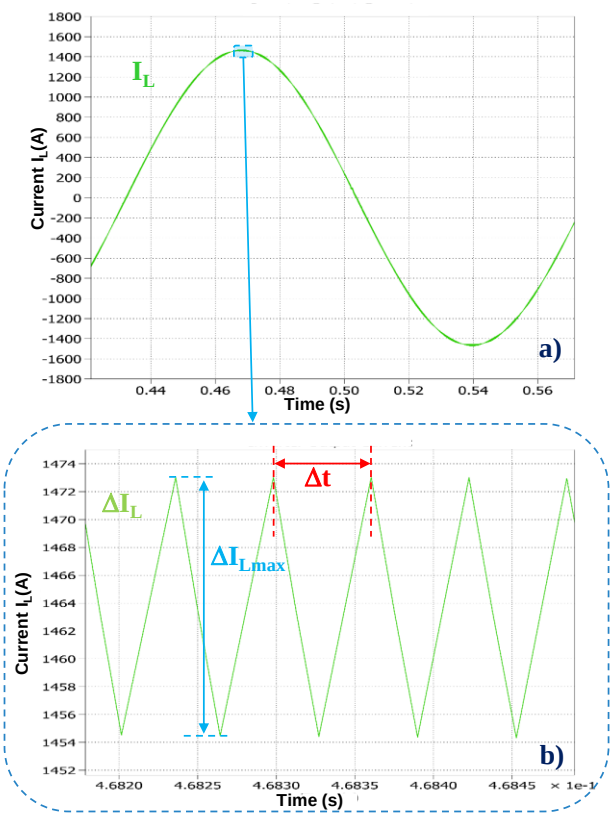

Fig. 12 a) Load current I_L simulation result. b) zoomed view of the ripple current behavior.

The inductive filters lead to the significant current ripple reduction as shown in Fig. 12b, showing a Δt=62 µs which means 16 kHz for the current ripple frequency (f_{ripple}) according to the interleaved strategy approach, corresponding to (1) with f_{sw}=4 kHz and N_c=4. The ΔI_L depends on the inductor leg filter: in the simulated case, a peak-to-peak current ΔI_{Lmax} of 20 A is evaluated (1.3% of the rated current I_L=1500 A). The simulation results have been obtained using an ideal dc voltage source (see Fig. 8).

To investigate the possible dc link voltage ripple with a real voltage supply, the electric charge of the dc link capacitor has been evaluated. The dc link current I_{dc} and its average $I_{dc,ave}$ over a switching period obtained in the simulation runs are shown in Fig. 13.

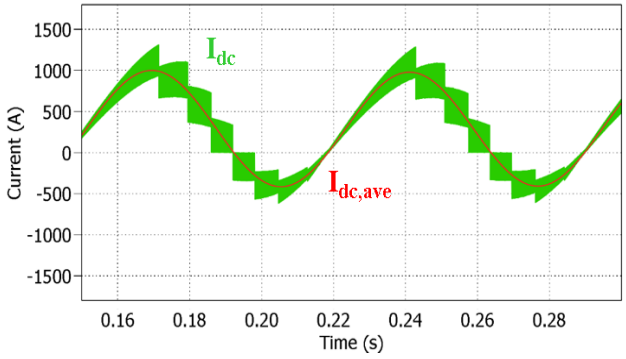

Fig. 13 dc link current I_{dc} and its average $I_{dc,ave}$ over a switching period.

A. *Optimal selection of leg number*

The optimal number of switching legs is a tradeoff between the maximum allowable current within a single switching leg, the current ripple in the NAS coil, and the complexity of the system. Numerical simulations were conducted to evaluate the optimal number of switching legs. Fig. 14 shows the current in one switching leg for various numbers of legs. For a single switching leg, this current matches the current of the NAS coil, while its value decreases almost linearly with the number of legs. In Fig. 15 the maximum current ripple in the NAS coil as a function of the number of switching legs is reported. A comparison of the two figures yields the following conclusions: 1) A low number of switching legs (i.e., fewer than 3-4 legs) results in a high current ripple in the NAS coil, furthermore the current in the single switching leg becomes excessive. 2) A high number of switching legs (i.e. more than 4 legs) enables achieving a marginal reduction of the NAS coil current ripple, but escalates the converter complexity and physical size, as every switching leg requires its own auxiliary systems (e.g. gate drivers, current sensors, auxiliary power supply, cooling, dc-link capacitors and so on). For this reason, a four-leg configuration has been selected.

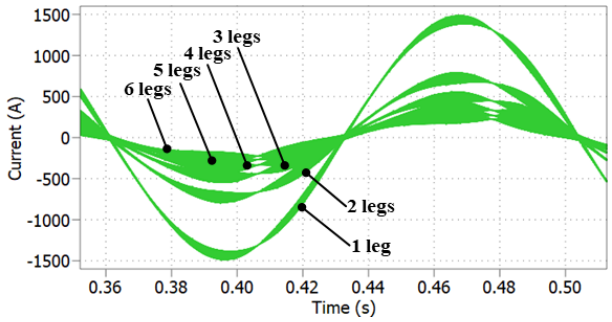

Fig. 14 Variation in the leg current of a single switching leg considering different numbers of switching legs.

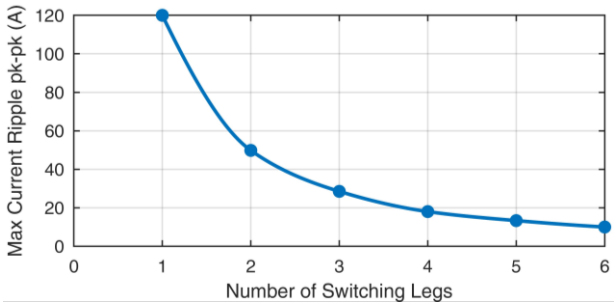

Fig. 15 Variation of maximum current ripple in the NAS coil considering different numbers of switching legs.

B. *Optimal selection of modulation strategy*

An interleaving modulation technique was employed for the four switching legs; however, this introduces a zero-sequence circulating current (ZSCC), leading to additional losses in the power semiconductors. Consequently, the proposed approach is compared with the case where the switching legs are commanded synchronously (i.e. no ZSCC). The results shown in Fig. 16 reveal that, without interleaving, the ripple current of the single leg is marginally reduced. However, the ripple current in the NAS coil significantly increases to a level that cannot be considered acceptable for the target application. As an alternative to mitigate ZSCC, an interleaved carrier phase shift (ICPS) PWM strategy can be employed [27]. Nevertheless, advanced modulation strategies are beyond the scope of this paper and will be explored for future work.

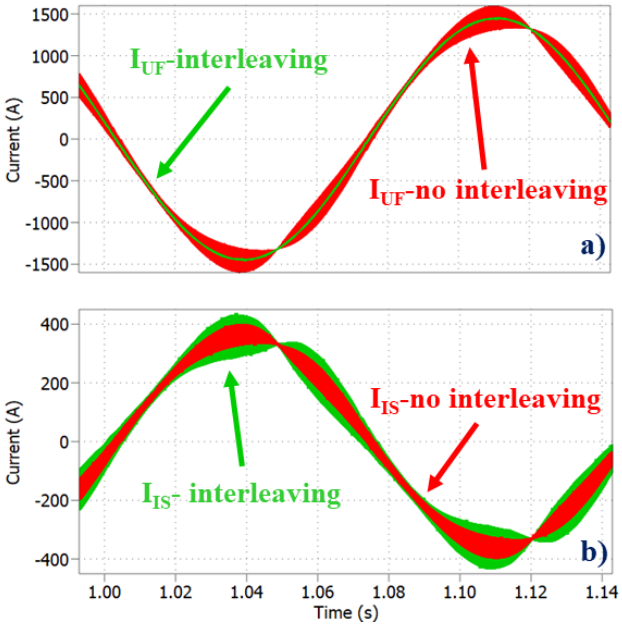

Fig. 16 Impact of the phase interleaving on the NAS coil current and phase switching leg current. a) current in the NAS coil with and without phase interleaving. b) current in one of the switching legs with and without phase interleaving.

VI. HIL Implementation

Validation via HIL is used for thoroughly testing the digital implementation of the modulation strategy previously simulated using time-continuous blocks.

The power elements of the converter are emulated using the PLECS RT Box 1, a real time simulator specifically designed for power electronics applications. This platform developed by PLECXIM can be easily programmed directly using PLECS (i.e., same software used during the simulation). The digital implementation of the control algorithm and PWM modulators is performed on the NUCLEO-STM32G474RE, a development board from STMicroelectronics based on the MCU STM32G4 targeting power conversion applications. The development board is interfaced to the RT Box 1 via a dedicated adapter board as shown in Fig. 17.

For the HIL implementation a converter with 4 switching legs and one unfolding leg is chosen. The control firmware previously implemented in PLECS is implemented on the MCU in C code using the STM32 CUBE IDE compiler. The PWM switching signals of the 5 legs (four switching legs and one unfolding leg) are generated using the HRTIM (High-Resolution Timer) unit of the MCU. This timer enables full flexibility in the modulation strategy having independent counters for each channel (each channel is used to generate the PWM signals of one converter leg). Furthermore, each channel

enables to generate two opposite PWM signals with the introduction of a dead time that in this specific case is set to 2 µs. A total of 10 PWM signals, one for each switch, are generated and utilized to drive the power switches emulated on the RT Box 1 as summarized in Fig. 18.

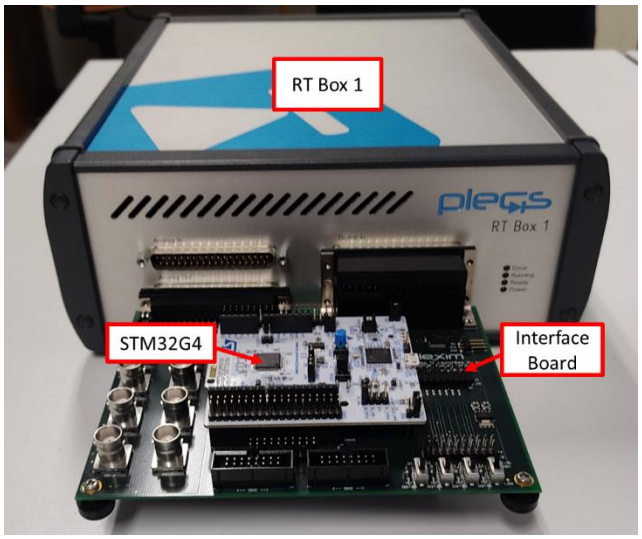

Fig. 17 HIL test rig consisting of the PLECS RT Box 1 and the NUCLEO-STM32G474RE.

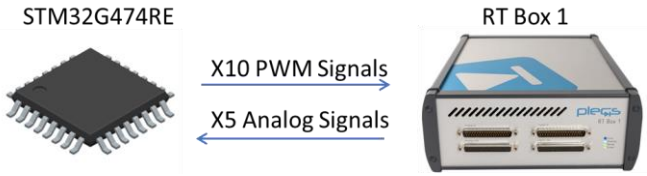

Fig. 18 Data exchanged between the STM32G474RE MCU and the RT Box 1.

The timer counters are configured in up-down counting mode so to emulate a triangular carrier. The input frequency to the TIMER counter is 170 MHz thus enabling to achieve high output resolution of the realized voltage. Considering the converter switching frequency of 4 kHz and the counter operating in Up-Down counting mode the PWM output signals are discretized on 21250 levels. Therefore, assuming a dc link voltage of 400 V the voltage discretization introduced by the timer is 19 mV. The triangular carriers with their reference duty cycles are shown in Fig. 19. The triangular carriers of the four switching legs are shifted between each other of a quarter of a period. In this way the equivalent switching frequency to the load is 16 kHz. Whereas the triangular carried of the unfolding leg is synchronized with the carrier of the first leg.

A further counter not shown in the figure called "master timer" supervises the correct phase alignment between the carriers. The main control interrupt service routine function is called in correspondence of the positive triangular vertex of leg1 indicated in Fig. 19 by the black arrows. The reference duty of the legs is updated on the positive vertex of their respective triangular carrier. For example, the duty cycle of leg2 is updated on the positive vertex of the triangular carrier of leg2. One special case is when the duty cycle of the unfolding leg goes from 0% to 100% or vice versa. In this case, the reference duty cycles of all the legs are updated immediately without waiting for the next positive triangle vertex. This avoids creating a voltage discontinuity on the load due to the commutation of the unfolding leg.

The power part of the converter consisting of the power source, power switches and reactive elements is emulated on the RT Box 1. The same model used for the PLECS simulation is executed on RT Box 1 in real-time. In this specific case, the model is executed every 5 µs. While the ideal scenario would involve executing the model as quickly as possible to closely reflect reality, the computational limitations of the chosen hardware, coupled with the model's complexity, prevent further reduction of the timestep. However, this timestep can be considered sufficient considering the adopted topology and the PWM switching frequency of 4 kHz (250 µs period).

Fig. 17 displays some of the results obtained from the HIL implementation, specifically showcasing the current profiles of the four switching legs. The obtained legs current well matched the currents obtained from the previous simulation, thus confirming the correct implementation of the digital control on the MCU. It is possible to note that the four currents are not perfectly overlapped, and this is due to the time discretization introduced by the HIL implementation. The same “digital” model implemented on the MCU was implemented in PLECS with the maximum time step set to (1 ns). The resulting phase currents are shown in Fig. 20, with the traces perfectly overlapping.

The results presented in this paper were obtained using an open-loop control approach, where the reference voltages were directly provided. Analyzing different control strategies is beyond the scope of this paper. However, in the implementation of the final converter, closed-loop current control is likely to be implemented. It is advisable to measure the output current of each switching leg rather than the total converter current flowing in this unfolding leg. This latter current is characterized by minimal ripple, as previously shown in Fig. 12. However, in the real application, a current imbalance between the switching legs is probable (e.g., due to unmatched impedances or switching times). Therefore, it is recommended to measure and control the current in each leg. Like in standard 2-level VSI converters, the optimal sampling point for the current is on the vertexes of the triangular carriers, thus enabling to sample of the average value of the current as summarized in Fig. 22.

VII. Conclusions

This paper investigates the dc/ac power converter operation supplying a single internal NAS coil to control EF and ELM in a tokamak. The converter topology solution is evaluated to optimize the current and voltage level requested in designing the NAS coil system for the DTT facility. Despite being based on the DTT requirements, the described approach and results are valid in many similar applications.

A single-phase inverter adopting the IGBT technology and using an interleaved approach and an unfolder switching leg is evaluated. The interleaving allows for obtaining a multilevel

output voltage, while the unfolding leg reduces the total converter losses. The inverter interleaved switching pole is achieved by 4 legs consisting of suitable IGBT modules. The unfolder switching leg is obtained with two high current IGBT modules, one for the high side and one for the low side of the half-bridge arrangement. The selection of the IGBT technology results in a trade-off among converter performance requested, size, and cost.

In future research, a power loss estimation and thermal management of the dc/ac converter will be approached to define the design procedure of the single inverter module for each NAS coil.

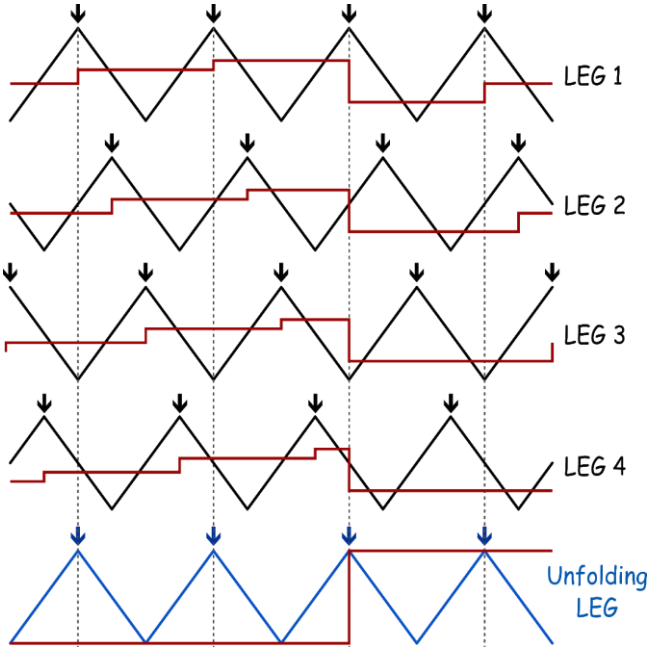

Fig. 19 Triangular carrier and reference duty cycles of the four switching and unfolding legs. The interrupt service routine and the output duty cycle updates for all the converter legs are performed in correspondence with the green arrow.

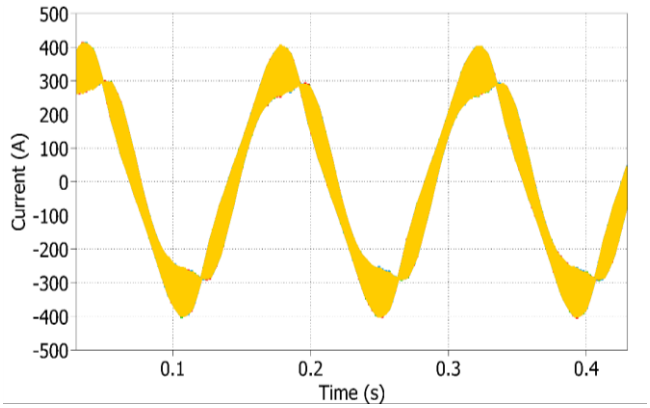

Fig. 20 Current in the four switching legs during the digital PLECs implementation.

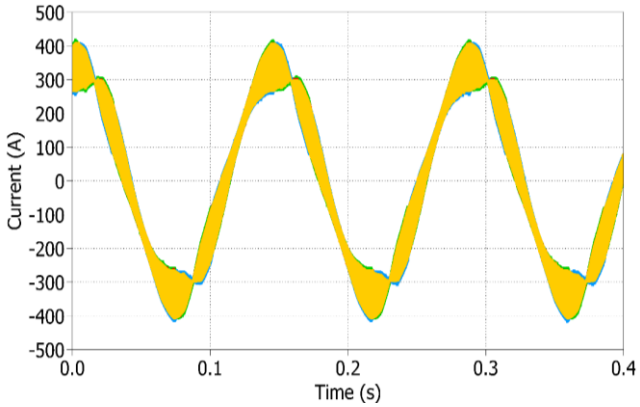

Fig. 21 Currents in the four switching legs (traces are overlapped) during the HIL implementation.

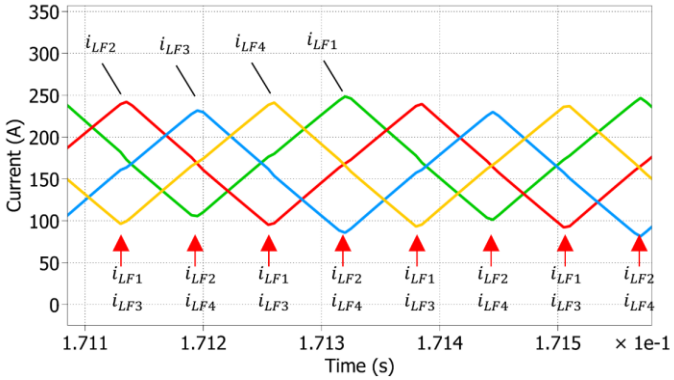

Fig. 22 Detail of Fig. 21 showing the current ripple and the optimal sampling time.

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