Optimal Dead Time Selection in GaN FET Switching Leg Via Thermal Analysis

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***Abstract*— Correct dead time selection is crucial in Gallium Nitride (GaN) devices having a significant impact on the overall performance, efficiency, and reliability of power electronic systems. Incorrect dead time selection can cause a variety of issues, including increased power losses, reduced efficiency, and increased device operating temperatures. This paper investigates the impact of dead time on the operating temperature of GaN devices employed in hard-switching converters. A measurement methodology where the dead time is selected to minimize the operating temperature of the hottest switch is proposed. Optimal dead time as a function of the device current is experimentally derived. Obtained data are discussed by comparing the optimal thermal derived dead time with the measured switching catachrestic of the device.**

Keywords—GaN FET, Dead Time, Thermal Management, Inverter, Switching Leg

I. Introduction

In power converter applications with switching legs, such as half-bridge or full-bridge DC-DC converters or in DC-AC inverter applications, dead time is necessary to avoid possible cross-conduction due to the actual device's transients [1]. In such applications, for Gallium Nitride (GaN) devices, the contribution of the switching losses during the dead time to the overall converter efficiency becomes noticeable. In a half-bridge configuration, dead time leads the devices to operate in reverse conduction, causing power losses that are related to the structure technology of the antiparallel diode. Enhancement GaN FET devices have higher equivalent reverse diode forward voltage compared to other anti-parallel diodes normally employed in switching devices [2]. Consequently, in GaN FETs, the reverse conduction power losses associated with the equivalent diode are a major drawback when compared to those of Silicon (Si) MOSFETs [3]. Therefore, the reverse conduction must be reduced to the minimum by shortening the dead time. Moreover, the decrease in dead time in inverter applications improves the quality of the output waveforms without the aid of compensation software systems [4]. However, additional switching losses may be generated if the dead time is shortened below a certain limit especially when the devices are operated at low load currents.

Thus, in converter power loss optimization, the correct dead time selection for these HEMT power devices becomes a crucial point. Optimal dead time selection is not trivial as requires measuring voltages and currents through the power device during the switching transient, however, this may not always be feasible, especially in GaN FET devices where optimized commutation loops do not allow the insertion of probes. Furthermore, as discussed in the subsequent paragraphs, the optimal dead time value is also impacted by the equivalent capacitance of the switching node, which is composed of both the semiconductors and load parasitics. Therefore, the selection of the optimal dead time should consider not only the characteristics of the semiconductor but also those of the load. Hence, it is crucial to derive the optimal dead time directly in the target application (e.g. DC-DC converter) to fully leverage the enhanced performance offered by GaN technology.

This paper proposes an optimal dead time selection methodology based on the thermal analysis of the device during the switching operations. The optimal selection of the dead time by a thermal analysis is explored, and several tests to demonstrate the goodness of the proposed solution are carried out. Thermal and electrical measurements are then compared. The main benefits of the proposed methodology are the easiness of implementation combined with its accuracy as demonstrated through experimental validation.

II. GaN FET in Reverse Conduction

The GaN FET is an enhancement mode (e-mode) device belonging to the High Electronic Mobility Transistors (HEMT). The actual GaN-based power electronic devices feature a planar structure with unipolar carriers involved in the conduction operation. When the Gate-Source voltage is over the threshold voltage the 2DEG phenomena leads to a conductive continuous path between Source and Drain with a reduced R_{DSon} [5]. In Fig. 1a the e-mode GaN FET structure with 2DEG operation path is depicted. In the reverse conduction operation, when $V_{GS} > V_{GSth}$ enough to fully reach 2DEG operation, the GaN FET operates in an ohmic region with R_{SDon} quite similar to the resistance in direct conduction (Fig. 1b), from which the voltage drop is equivalent to the direct operation [2]. Therefore, the GaN transistor is a naturally bidirectional switch [6]. When $V_{GS}<V_{GSth}$ the GaN FET features an equivalent diode behaviour as shown in Fig. 1b.

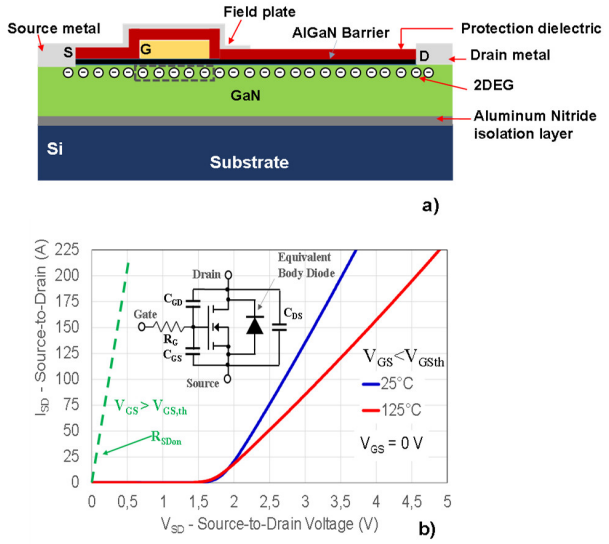

Fig. 1. GaN FET structure with a high mobility conductive path between Source a Drain due to the 2DEG phenomena. b) the reverse conduction with $V_{GS}>V_{GSth}$ showing a R_{SDon} similar to the direct conduction and the equivalent diode behaviour when $V_{GS}<V_{GSth}$ at 25°C and 125°C.

In case of a switching leg with inductive load, during the dead time interval, the load current is conducted by the equivalent body diode, thus resulting in additional losses. Furthermore, the condution characteristics of the equivalent body diode worsten with the temperature Fig. 1b [7]. The equivalent diode voltage drop for the GaN FET EPC2065 used as a case study in this paper (Typical R_{DSon}=2.7 mΩ, with 80 V of maximum voltage, from EPC Corporation) is 2 V at 25 A (Fig.1b). In this operative condition, the voltage drop of GaN FET is considerably higher than a body diode voltage drop of an equivalent Si MOSFET [8]. Considering the Si MOSFET BSC026N08NS5 (Typical R_{DSon}=2.6 mΩ, with 80 V of Drain-Source breakdown voltage, from Infineon) the body diode voltage drop V_{SD} is at maximum equal to 1.1V. Therefore for GaN FET devices power losses for the same dead time are considerably higher than in Si devices. Moreover, from the comparison of the dynamic characteristic of the two different technologies' power electronic devices, the GaN FET features higher-speed transients compared with Si MOSFET [9], [10]. The lower switching transient for GaN-based power transistors allows reducing the required dead time and, consequently, the power losses due to the high equivalent diode drop decrease. The power losses lead to an increase in junction temperature that increases further the voltage drop, as shown in Fig. 1b. Consequently, the device offers a sensitivity to the temperature variation. Therefore, the temperature can be used to sense the reverse power losses to estimate these variations during the dead time operation [11].

III. Dead Time in Switching Leg

In modern power electronic conversion systems, GaN FETs switching legs are commonly used to drive loads with varying current demands. Fig. 2 and Fig. 3 display the theoretical node voltage transients (V_{SW}) of a switching leg. The simulation results obtained with LT Spice considering a GaN FET model validated in [12], depicted in Fig. 2, show the typical switching waveforms in case of positive load current (from the voltage source to the inductive load) and positive dV_{SW}/dt, while Fig. 3 shows the same condition with negative dV_{SW}/dt. The impact of the dead time on the switching transients is highlighted by setting it to 40 ns during simulation. As shown in Fig. 2, when Q_L is turned OFF and Q_H is turned ON after the dead time is imposed, the output voltage slope (V_{SW}) remains constant with varying load currents. Therefore, in this case, dead time selection is independent of the load current value (as far as remains positive) and should always be minimized thus avoiding the conduction of the equivalent diode of Q_L switch. Per contrary in Fig. 3 where Q_H is turned OFF and Q_L is turned ON the optimal dead time depends on the load current. Immediately after Q_H turn-OFF, the voltage switching node starts lowering with a slope that depends on the output current and the equivalent parasitic capacitance [3]. Ideally, Q_L is turned ON as soon as the switching node voltage reaches zero, thus avoiding the reverse conduction of the equivalent diode of the GaN FET. E.g. in this specific case the 40 ns dead time allows performing a zero voltage commutation when the load current is about 2 A. Whereas at lower current a hard switching commutation is performed and the voltage of the switching node is forcibly brought to zero by the low side switch turn-ON thus causing additional switching losses. Per contrary at higher current, the switching node voltage transition is faster and the equivalent diode starts conducting thus causing additional losses in the

device. Thus, at high currents (above 15 A) the voltage transition is dominated by the gate voltage variation of Q_H and becomes independent from the load current (minimal dead time must be selected). Similar considerations can be done in case of negative load current (from the inductive load to the switching leg). In the actual switching leg operation, it is challenging to understand which is the optimal dead time selection.

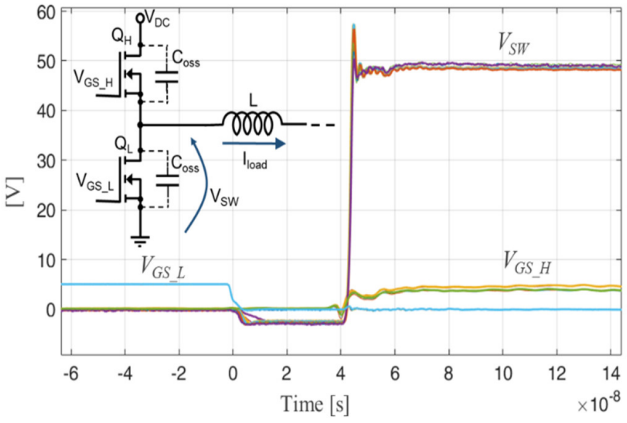

Fig. 2. Simulation waveforms during Q_H turn-ON. Different load current values (0.5 A; 1 A; 1.5 A; 2 A; 10 A; 15 A; 20 A) are considered

The switching currents cannot be easily measured as the current in the device cannot be evaluated without modifying the switching power loop layout to insert the current probe would be necessary. However, such HEMT devices cannot be effectively operated in case of large switching power loops (i.e. overvoltages caused by the power loop parasitics may damage the device). In the proposed approach the device is tested at different dead times and load currents while measuring the temperature of the hottest switch. This method is easy to implement and does not require the measurement of voltages and currents in a short timescale.

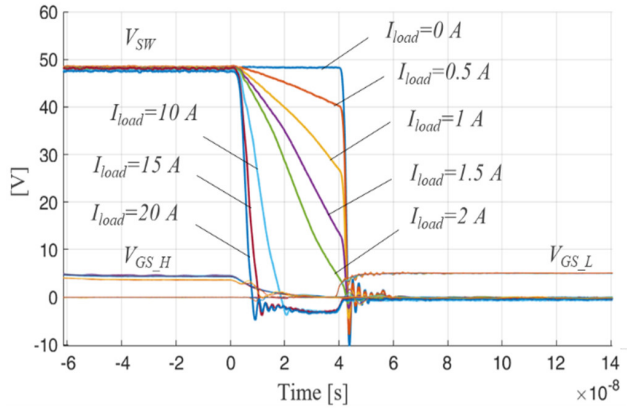

Fig. 3. Simulation waveforms during Q_L turn-ON. Different load current values (0.5 A; 1 A; 1.5 A; 2 A; 10 A; 15 A; 20 A) are considered.

IV. Experimental Evaluation of the Optimal Dead Time Via Thermal Analysis

The proposed methodology aims at minimizing the temperature of the hottest switch by selecting an optimal dead time specific for each load condition. Experimental validation is performed using the EPC90137 evaluation board housing two EPC2065 GaN FET having a nominal breakdown voltage of 80 V and a rated DC current of 60 A @T_{case}=25°C. Besides the power switches the evaluation board houses their respective gate driver. The switching signals are externally provided using an STM32H7 Nucleo board whose MCU high-resolution timer modulator can generate switching signals with a time discretization of less than 1 ns. All tests are conducted at a constant switching frequency of 500 kHz. This frequency was deliberately chosen to be sufficiently high, ensuring that the switching losses and, consequently, the effects of dead time become noticeable and have a discernible impact on the overall efficiency (i.e. operating temperature) of the converter. The duty cycle is set to 50%, meaning that the upper side switch and the low side switch are in conduction for the same amount of time. Dead time insertion is considered and compensated for, ensuring that both switches are conducting for half of the time. As the current load sign is known it is possible to know which switch is in conduction during the dead time and the reference duty cycle can be changed accordingly so to keep both switches in conduction for exactly half of the time. E.g. if the current is exiting from the switching node, during the dead time the current is recirculated through the equivalent body diode of the low side switch, therefore this extra conduction time can be easily compensated. The measurement setup and its functional schematic are shown in Fig. 4 and Fig. 5. A programmable closes-loop current-controlled inverter (operating at a switching frequency of 10 kHz) is used as an electronic load to control the output current of the GaN FET leg. The two converters are interfaced using an LCL filter so that the current ripples due to the PWM modulation of the two converters do not interact with each other. The two ferrite core filtering inductors are identical with a nominal value of 300 µH, while the capacitor filter has a nominal value of 820 µF. The two converters share the same 48 V DC-link so only the losses to the system must be provided via an external DC source. During the tests, the GaN FET leg is operated at positive output currents (buck mode) with a constant duty cycle of 50%. While the load converter is closed loop current controlled thus enabling to set multiple values of load current. If we assume that the two converters are decoupled, and we have a 300 µH filtering inductor, a 48V DC-link voltage, a 500 kHz switching frequency, and a 50% duty cycle, then the resulting current ripple at the output of the GaN leg is 160 mA. This current ripple can be neglected and the output current can be assumed as constant. The case temperature of the two GaN

FETs is monitored via an IR camera (Fig. 6). The devices are tested for different load currents and dead times. Each measurement point is maintained for 10 minutes (i.e. thermal transients are over) after that the temperature of the hottest device is recorded. The results are shown in Fig. 7 where the temperature has been normalized for each current tested using the lowest value recorded (i.e. the temperature for a load current of 2 A is normalized using the lowest hotspot temperature measured during the test at 2 A). Remarkably for each current, there is an optimal dead time that minimizes the temperature of the hottest switch. For example, when operating at a low current the optimal dead time is tens of ns while when operating at a high current is below 10 ns reaching a minimum of 6 ns when the output current is above 10 A. This is due to the different slope of V_{SW} with the current value (see Fig. 3). The trend demonstrates that in the case of current exiting from the switching node and positive dV_{SW}/dt, the optimal dead time is close to the zero voltage switching point because the minimized switching losses are achieved as the best trade-off between the hard switching losses and the reverse conduction losses. For dead time values longer than the optimal one, temperatures rise in proportion to the dead time duration. The reason is that the reverse conduction losses, resulting from the constant reverse conduction voltage drop and the constant load current, are dominating the total energy loss during the dead time. A higher current load makes the iso-temperature lines steeper. On the other hand, for dead time values shorter than the optimal one, losses are due only to the hard switching. It is important to note that if the value of the equivalent capacitance changes (i.e. the same inverter board is connected with a different load or electrical machine) also the optimal dead time value will change. In this case, the presented procedure can be repeated. The easy repetitiveness of the procedure is useful also because new results can take into account the parametric change due to the ageing of the components. Additional tests at different ambient temperatures have demonstrated that the V_{SW} waveform does not change significantly with the temperature this behaviour has also been confirmed by the existing literature [13]. This means that repeating the procedure also for different ambient temperatures is useless because the same minimum dead time value will be obtained for a given load current amplitude. It must be noted that the proposed approach does not necessarily minimize the overall losses but minimize the temperature of the hottest device (i.e. there may be a value of dead time that may better distribute the losses between the two components rather than their absolute lowering). Furthermore, due to their proximity (indispensable to minimize the parasitics of the commutation loop), the two devices cannot be considered thermally independent. Fig. 8 shows the optimal dead time for the Q_L turn-ON commutation in the function of the load current when exiting from the switching node. It can be observed that the curve tends to be infinite when the current value tends to zero. Nevertheless, for low current values (i.e. < 1 A), a finite dead time value (i.e. 60 ns maximum) is recommended. On the contrary, the figure shows that by growing the current, the optimal dead time diminishes until it reaches the minimum value of 6 ns. In this example, the minimum optimal dead time value is reached for currents higher than 7 A. The reason why there is no change in the optimal dead time is that with these current values, the slope of the voltage fall remains maximum and almost unchanged. Additional experimental measurements are shown in Fig. 9 and Fig. 10 where the low switch gate voltage and the commutation loop voltage are measured for different values of dead time at a constant current load of 5 A. According to the thermal analysis, the optimal dead time, in this case, is 10 ns. Regarding Fig. 9 it can be noticed that at 10 ns the low side switch performs a zero voltage switching (i.e. lowest commutation losses) while at a lower dead time, the parasitic capacitance of the high side switch is forcibly charged by the low side switch commutation causing additional switching losses. On the contrary, at higher dead times (i.e. 20 ns) the equivalent diode of the low-side switch is brought into conduction causing additional conduction losses. Fig. 10, shows that when the high side GaN FET is turned ON the dead time must be always minimized being independent of the commutated current.

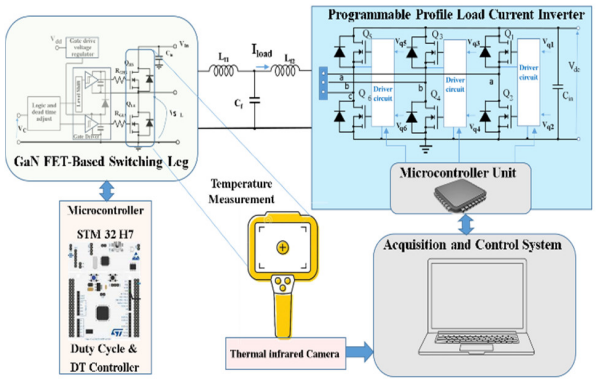

Fig. 4. Measurement setup arrangement.

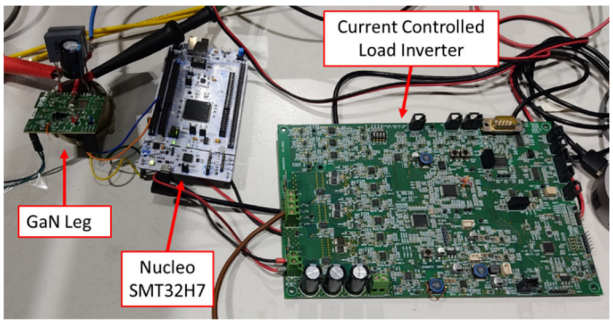

Fig. 5. The test rig overview.

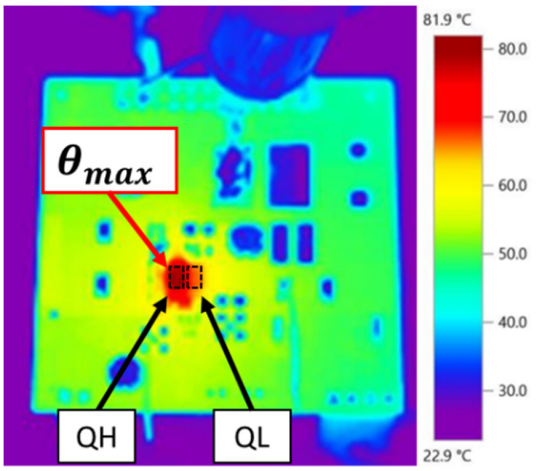

Fig. 6. Infrared image of the devices under test.

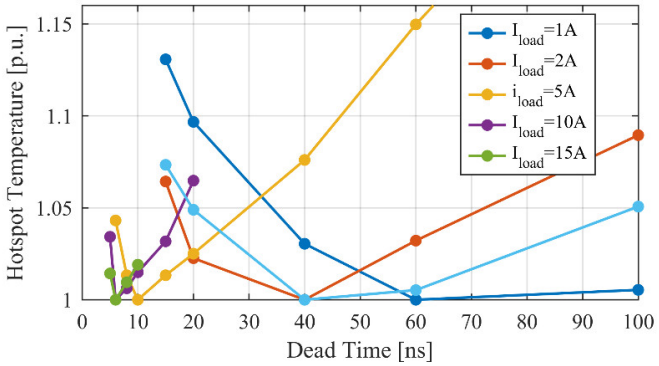

Fig. 7. Measured hotspot temperature as a function of the dead time for different load currents. Results are normalized to the minimum measured temperature for each I_{load}.

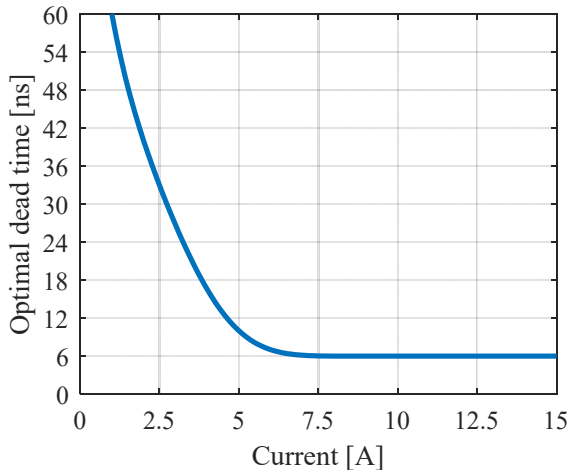

Fig. 8. Optimal dead time for Q_L turn-ON as a function of the load current.

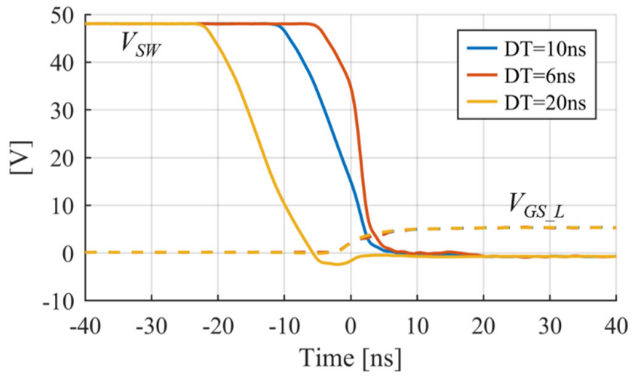

Fig. 9. Experimental switching waveforms @I_{load}=5 A for different dead times. Q_H turn-OFF.

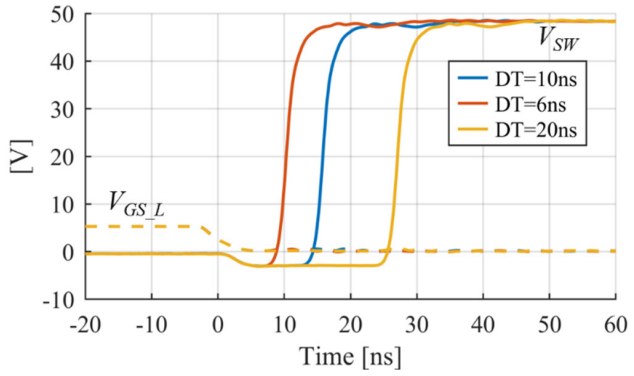

Fig. 10. Experimental switching waveforms @I_{load}=5 A for different dead times. Q_H turn-ON.

V. Conclusions

An optimal dead time selection methodology based on thermal measurement of the power devices was presented for GaN FET devices. The proposed methodology can be applied similarly on different converter topologies [14] and does not require measuring voltages and current during the fast switching transients. Furthermore, the same methodology can be applied to different semiconductors technologies, however additional considerations and measurements may be needed for devices in which the switching transient is temperature dependent. This can be the case of Si MOSFETs where the switching voltages are affected by the junction temperature of the device. The optimal dead time computed via the thermal analysis can be stored inside the controller unit in the form of a look-up table where the input is the commutated current while the output is the optimal dead time. In the final application, the controller can ideally vary the dead time depending on the load current. In this study, the temperature of the switching devices was monitored using an infrared (IR) camera. Alternatively, two thermistors can be used to directly measure the case temperature of the devices. The temperature data acquired by the thermistors can be directly read by the microcontroller unit (MCU), enabling the automation of

the dead time characterization procedure. In this work a "symmetrical" dead time was used, meaning that the same dead time is applied between Q_H turn-OFF and Q_L turn-ON, and between Q_L turn-OFF and Q_H turn-ON. However, as previously shown in Fig. 2 and Fig. 3 the optimal dead time in the two cases is different. For example, in case of current exiting from the switching node, the optimal dead time between Q_L turn-OFF and Q_H turn-ON should be the minimum one required for avoiding the leg short circuit, independently from the current level.

It must be noted that most industrial MCUs do not allow the use of asymmetrical dead time. However, most modern MCUs like the STM32H743ZI from STMicroelectronics used during the tests make use of a high-resolution timer that allows the implementation of asymmetrical dead times. This was previously possible only using programmable logic devices such as FPGAs. It is therefore plausible, that in the near future, multiple industrial MCUs will have the ability to use asymmetrical dead times. Therefore, in future work, the use of asymmetrical dead times will be investigated using a similar approach. This will enable an additional reduction of the dead time losses caused by the reverse conduction of the equivalent body diode.

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