Impact of current collecting grids on the scalability of 3-terminal perovskite/silicon tandems with bipolar transistor architecture

Gemma Giliberti1, Federica Cappelluti1,* Senior Member, IEEE

Department of Electronics and Telecommunications, Politecnico di Torino, Corso Duca degli Abruzzi 24, 10129 Torino, Italy

Abstract—The heterojunction bipolar transistor (HBT) structure is an attractive solution for developing three-terminal perovskite/silicon tandem solar cells compatible with dominant silicon photovoltaic devices, such as PERC and heterojunction. However, in contrast to three-terminal tandems based on interdigitated back contact silicon cells, the three-terminal HBT requires the implementation of the third contact at the base (middle) layer. To this aim, the simplest solution is to access the base layer from the cell front side by implementing a grid layout with top interdigitated contacts (TIC). In this work, we elaborate on the feasibility of the HBT structure for 3T perovskite/silicon tandem solar cells. We report, based on optical and drift-diffusion simulations, proof-of-concept designs with high efficiency potential, and we analyze, with the aid of circuit level simulations, the implications of a TIC grid layout in the perspective of scaling up to large areas. Our results show that the HBT architecture is a promising candidate for developing 3T perovskite/silicon tandem solar cells compatible with industry standard silicon photovoltaics.

Index Terms—perovskite-silicon tandem solar cell, three-terminal, power loss, physics-based simulation, circuit-level simulation.

I. INTRODUCTION

Perovskite/silicon (PVS) tandem solar cells are among the most promising candidates for next generation photovoltaics [1]. They recently achieved the efficiency record of 32.5% [2], approaching that one of costly III-V double-junction solar cells [2]. Besides two- and four-terminal approaches, three-terminal (3T) tandems based on interdigitated back contact (IBC) silicon cells are currently being investigated [3], in view of the advantages of the 3T approach in terms of energy yield in the field [4].

The 3T-HBT solar cell [5], [6] offers an attractive alternative for the development of 3T PV tandem solar cells suitable for integration with industry standard photovoltaic technologies such as PERC and heterojunction (HTJ) silicon cells. The 3T-HBT solar cell has a theoretical (material-based) efficiency limit as high as that one of a perfectly matched 2-terminal tandem, but with a simpler structure because the top and bottom subcells are seamlessly connected, without the need of any additional interconnecting layer. However, in the perspective of large-area devices, the drawback might come from the realization of the third terminal at the base layer. In fact, implementing the 3T-HBT in the PERC or HTJ silicon platform requires, as simplest possible solution, adopting a top-interdigitated-contact (TIC) [7], whose implications in terms of shading and resistive losses must be carefully evaluated.

In this work, we report a simulation study of 3T-HBT PVS tandem solar cells aimed at investigating their efficiency potential and perspectives for scaling up to large areas. We present proof-of-concept 3T-HBT PVS devices designed by means of optical and transport simulations and analyze the power losses induced by the current collecting grid and how they scale with the cell area based on circuit-level simulations.

II. DEVICE & METHODS

Fig. 1(a) sketches a 3T-HBT PVS tandem made of a n-i-p PVK subcell on top of a planar homojunction n+/p Si bottom cell with design parameters in line with [1]. From the top, the TCO (34 nm)/PTAA (11 nm) / PVK(480 nm) layer stack constitutes the p-emitter layer; the SnO$_2$ (25 nm) electron transport layer (ETL) and n-Si (150 nm) one form the base layer on top of the 150µm thick p-type c-Si collector. The cell uses a 92 nm thick MgF antireflection coating. As shown in Fig. 1(b,c), emitter and base are accessed from the top with a TIC layout, with the base contact (Z) placed on the n-Si layer and the emitter contact (T) on the TCO layer. A full-area contact (R) is used at the collector.
parameters assumed are available.

### III. RESULTS & DISCUSSION

Fig. 3 shows the External Quantum Efficiency and J-V characteristics of the subcells of the 3T-HBT PVS tandem under study, and the J-V characteristics reproduced by the Ebers-Moll model. Transport simulations showed that band discontinuities and materials resistivity are such that the two subcells substantially work as independent, i.e. no appreciable transistor effect occurs through the SnO$_2$/n$^+$-Si base [8]. The intrinsic device has high efficiency of $\approx 29.4\%$.

In order to analyze the influence of the TIC grid on the device performance and scalability to large areas, we consider typical metal grid parameters [9], [11] as summarized in Table II. A shading loss factor of $2w_f/d_t$ is applied to the bottom sub-cell, and $3w_f/d_t$ to the top one, assuming for the etched region, needed to access the base layer, a width twice that of the metal finger.

First, we consider relatively small devices ($l_t = 1.5$ cm), in which resistive effects are dominated by lateral transport, and study the efficiency loss in terms of finger spacing and sheet resistance of the base layer, with fixed ITO/TCO emitter sheet resistance ($\approx 274\,\Omega/\square$). The HBT base region is composed of the bottom layer of the PVK subcell and the top layer of the Si one, therefore its sheet resistance is strongly dependent on the HBT configuration (p-n-p or n-p-n) and bottom cell technology. As seen in Fig. 4 for $R_{sheet}^{base}$ up to $100\,\Omega/\square$ (representative of PVS tandems on homojunction c-Si cells as in Fig. 1) the efficiency loss can be minimized to less than 3%
Fig. 4. Efficiency loss as a function of the finger distance \((d_f)\) and base sheet resistance \((R_{sh}^{\text{Base}})\).

Fig. 5. (a) Emitter and base resistance components for a PVS 3T-HBT tandem with 1.5 cm x 1.5 cm area and (b) associated fractional resistive power loss.

with finger distance of 1.5 mm or larger. On the other hand, for PVS 3T-HBT tandems on HTJ silicon cells, the high sheet resistance of the a-Si:H layers \((\approx 10^5 \Omega/\text{sq})\) must be mitigated by exploiting a highly conductive transport layer for the PVK top cell, such as the SnO\(_2\) layer used in the \(p-n-p\) HBT under study (sheet resistance \(\approx 10^3 \Omega/\text{sq}\)).

Fig. 5 shows the emitter and base resistance and the corresponding fractional power loss estimated for the 3T-HBT PVS in Fig. 4 with \(R_{sh}^{\text{Base}} = 74 \Omega/\square\), finger length 1.5 cm, finger distance 1.5 mm. Here, the dominant resistive path is associated to the lateral transport across base and emitter. The total base resistance is about 1/3 of the emitter one, but the fractional power loss \((\propto R_f^2)\) associated to base and emitter grids is comparable since the current through the base, which corresponds to the sum of the top and bottom subcell currents, is about 70% higher than that of the emitter. Therefore, as the cell area and finger length increase, the resistive effects of the base grid become the dominant cause of efficiency loss.

In Fig. 4 we analyze the variation of efficiency loss with scaling up of the finger length for two values of the base sheet resistance, representative of 3T-HBT tandems on homojunction and heterojunction silicon cells. An optimized interdigitated front grid can keep power losses below 5% for finger lengths up to about 6-8 cm depending on the base sheet resistance. Such power loss could be reduced by material and device optimization, and by developing more advanced grid designs, for example employing overlapped contact grids to reduce shading losses. Overall, these results show the potential, even in the perspective of scaling up to large areas, of using the HBT architecture to develop high efficiency three-terminal perovskite/silicon tandems that can be integrated with industry standard silicon bottom cells.

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REFERENCES


