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Impact of current collecting grids on the scalability of 3-terminal perovskite/silicon tandems with bipolar transistor architecture

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Abstract—The heterojunction bipolar transistor (HBT) structure is an attractive solution for developing three-terminal perovskite/silicon tandem solar cells compatible with dominant silicon photovoltaic devices, such as PERC and heterojunction. However, in contrast to three-terminal tandems based on interdigitated back contact silicon cells, the three-terminal HBT requires the implementation of the third contact at the base (middle) layer. To this aim, the simplest solution is to access the base layer from the cell front side by implementing a grid layout with top interdigitated contacts (TIC). In this work, we elaborate on the feasibility of the HBT structure for 3T perovskite/silicon tandem solar cells. We report, based on optical and drift-diffusion simulations, proof-of-concept designs with high efficiency potential, and we analyze, with the aid of circuit level simulations, the implications of a TIC grid layout in the perspective of scaling up to large areas. Our results show that the HBT architecture is a promising candidate for developing 3T perovskite/silicon tandem solar cells compatible with industry standard silicon photovoltaics.

Index Terms—perovskite-silicon tandem solar cell, three-terminal, power loss, physics-based simulation, circuit-level simulation.

I. INTRODUCTION

Perovskite/silicon (PVS) tandem solar cells are among the most promising candidates for next generation photovoltaics [1]. They recently achieved the efficiency record of 32.5% [2], approaching that one of costly III-V double-junction solar cells [2]. Besides two- and four-terminal approaches, three-terminal (3T) tandems based on interdigitated back contact (IBC) silicon cells are currently being investigated [3], in view of the advantages of the 3T approach in terms of energy yield in the field [4].

The 3T-HBT solar cell [5], [6] offers an attractive alternative for the development of 3T PVS tandem solar cells suitable for integration with industry standard photovoltaic technologies such as PERC and heterojunction (HTJ) silicon cells. The 3T-HBT solar cell has a theoretical (material-based) efficiency limit as high as that one of a perfectly matched 2-terminal tandem, but with a simpler structure because the top and bottom subcells are seamlessly connected, without the need of any additional interconnecting layer. However, in the perspective of large-area devices, the drawback might come from the realization of the third terminal at the base layer. In fact, implementing the 3T-HBT in the PERC or HTJ silicon plat-
Under illumination, photogenerated electrons and holes induce current flows collected at the T, Z and R terminals. As depicted in Fig. 1 carrier transport through materials with finite conductivity and contacts cause power loss mechanisms that can be modeled as resistive effects. The resulting equivalent circuit model of the 3T-HBT is shown in Fig. 2. It consists of the Ebers-Moll circuit of the intrinsic device under illumination [5], [8] completed by parasitic series resistances at each terminal. In particular, as summarized in Table I the equivalent base and emitter series resistance account for the contribution of lateral current flow ($R_{S,lateral}$) and of contact ($R_C$) and finger ($R_{finger}$) resistance of the current collecting grids. These are calculated based on the equivalent lumped circuit model of the unit cell of the metal grid (Fig. 1) the efficiency loss can be minimized to less than 3% (representative of PVS tandems on homojunction c-Si cells as in Fig. 3) the efficiency loss can be minimized to less than 3%.

In order to analyze the influence of the TIC grid on the device performance and scalability to large areas, we consider typical metal grid parameters [9], [11] as summarized in Table II. A shading loss factor of $2w_l/d_l$ is applied to the bottom sub-cell, and $3w_l/d_l$ to the top one, assuming for the etched region, needed to access the base layer, a width twice that of the metal finger.

First, we consider relatively small devices ($l_t = 1.5$ cm), in which resistive effects are dominated by lateral transport, and study the efficiency loss in terms of finger spacing and sheet resistance of the base layer, with fixed ITO/TCO emitter sheet resistance ($\approx 274 \, \Omega / \square$). The HBT base region is composed of the bottom layer of the PVK subcell and the top layer of the Si one, therefore its sheet resistance is strongly dependent on the HBT configuration ($p$-$n$-$p$ or $n$-$p$-$n$) and bottom cell technology. As seen in Fig. 4 for $R_{sheet}^{base}$ up to $100 \, \Omega / \square$ (representative of PVS tandems on homojunction c-Si cells as in Fig. 3) the efficiency loss can be minimized to less than 3%.

### Table I: Expressions of parasitic resistances

<table>
<thead>
<tr>
<th>Resistive loss</th>
<th>Label</th>
<th>Expression [\Omega , \text{cm}^2]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lateral conduction</td>
<td>$R_{S,lateral}$</td>
<td>$\frac{1}{12} , R_{S} , d_l^2$</td>
</tr>
<tr>
<td>Contact</td>
<td>$R_c$</td>
<td>$\frac{1}{2} , d_l , \sqrt{\frac{R_{S}}{\rho_c}} , \coth \left( \frac{w_l}{2} \sqrt{\frac{R_{S}}{\rho_c}} \right)$</td>
</tr>
<tr>
<td>Fingers</td>
<td>$R_l$</td>
<td>$\frac{1}{3} , \frac{w_l}{d_l} , \rho_c , d_l^2$</td>
</tr>
<tr>
<td>Emitter</td>
<td>$R_E$</td>
<td>$R_{E, lateral}^B + R_E^B + R_E^B$</td>
</tr>
<tr>
<td>Base</td>
<td>$R_B$</td>
<td>$R_{B, lateral}^B + R_B^B + R_B^B$</td>
</tr>
<tr>
<td>Collector</td>
<td>$R_C$</td>
<td>$\rho_{p, Si} , \text{collector}$</td>
</tr>
</tbody>
</table>

### Table II: Grid geometrical and material parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Label</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Finger width (\mu m)</td>
<td>$w_l$</td>
<td>40</td>
</tr>
<tr>
<td>Finger height (\mu m)</td>
<td>$l_t$</td>
<td>15</td>
</tr>
<tr>
<td>Contact resistivity (Ag/ITO) (m\Omega , \text{cm}^2)</td>
<td>$\rho_c$</td>
<td>1.27</td>
</tr>
<tr>
<td>Contact resistivity (Ag/Si) (m\Omega , \text{cm}^2)</td>
<td>$\rho_c$</td>
<td>1</td>
</tr>
<tr>
<td>Gridline resistivity (\Omega , \text{cm})</td>
<td>$p_{mo}$</td>
<td>$2.65 \times 10^{-6}$</td>
</tr>
<tr>
<td>ITO resistivity (\Omega , \text{cm})</td>
<td>$p_{ITO}$</td>
<td>$9.31 \times 10^{-4}$</td>
</tr>
<tr>
<td>c-Si (n, carriers) resistivity (\Omega , \text{cm})</td>
<td>$p_{Si}$</td>
<td>$1.11 \times 10^{-3}$</td>
</tr>
<tr>
<td>SnO$_2$ resistivity (\Omega , \text{cm})</td>
<td>$p_{SnO_2}$</td>
<td>$5.2 \times 10^{-3}$</td>
</tr>
</tbody>
</table>
fractional power loss ($R_{\text{sh}}^{\text{Base}}$) associated to the lateral transport across base and emitter. The finger distance 1.5 mm. Here, the dominant resistive path is and device optimization, and by developing more advanced sheet resistance. Such power loss could be reduced by material and device optimization, and by developing more advanced grid designs, for example employing overlapped contact grids to reduce shading losses. Overall, these results show the potential, even in the perspective of scaling up to large areas, of using the HBT architecture to develop high efficiency three-terminal perovskite/silicon tandems that can be integrated with industry standard silicon bottom cells.

IV. ACKNOWLEDGEMENTS

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REFERENCES


