Discontinuous PWM Modulation for Active Power Filters Operating in Disturbed Environments

Discontinuous PWM Modulation for Active Power Filters Operating in Disturbed Environments

Alessandro Roveri
Prima Electro S.p.A.
Moncalieri (TO), Italy
alessandro.roveri@primaelectro.com

Fabio Mandrile
Dipartimento Energia
Politecnico di Torino, Italy
fabio.mandrile@polito.it

Vincenzo Mallemaci
Dipartimento Energia
Politecnico di Torino, Italy
vincenzo.mallemaci@polito.it

Radu Bojoi
Dipartimento Energia
Politecnico di Torino, Italy
radu.bojoi@polito.it

***Abstract*—Active power filters (APFs) are power converters able to compensate for the distorted current components injected into the mains by non-linear loads. To reduce the APF switching losses and thus to allow using higher switching frequencies, discontinuous pulse-width modulation (DPWM) techniques have been developed in the literature. However, the DPWM techniques applied to APFs are highly sensitive to the high frequency disturbances on the power lines. Therefore, this paper proposes a dedicated discontinuous modulation technique for APFs installed in disturbed environments, able to minimize the switching losses for any operating condition. The proposed solution has been experimentally validated on a 100 kVA 2-level APF inverter compensating a regenerative system used for the final functional test of industrial inverters at the end of the production line.**

***Index Terms*—Active power filters, discontinuous pulse-width modulation, inverter losses, common mode voltage, disturbed environments**

I. Introduction

The active power filter (APF) is a power converter used to limit the low frequency current harmonics injected into the grid by non-linear loads, as diode or thyristor front-end rectifiers. The distorted current components lead to an overall increase of the current drawn from the grid with subsequent overheating of the supplying line cables and the triggering of the line protection devices and interference with neighboring sensitive electronic components. Therefore, international standards and recommendations, such as the IEEE 519, provide harmonic distortion limitations to mitigate the negative effects on power systems. The shunt-type APF is an effective solution to respect these standards. It is connected in parallel to the distorting load and injects non-sinusoidal currents to make the overall grid current sinusoidal at unity power factor [1-3]. The case study of non-linear load presented in this paper is a regenerative system used for the final functional test of industrial drive inverters (DUT) at the end of the production line, as shown in Fig. 1. The power consumption during the test is minimized, since the active power recirculates in the regenerative system through a line transformer and only an active current is drawn from the grid to compensate for the system losses. Therefore, the distorted current produced by the DUT three-phase passive rectifier is the current drawn from the grid, thus resulting in a non-compliance of the power system with the regulations for the harmonic control.

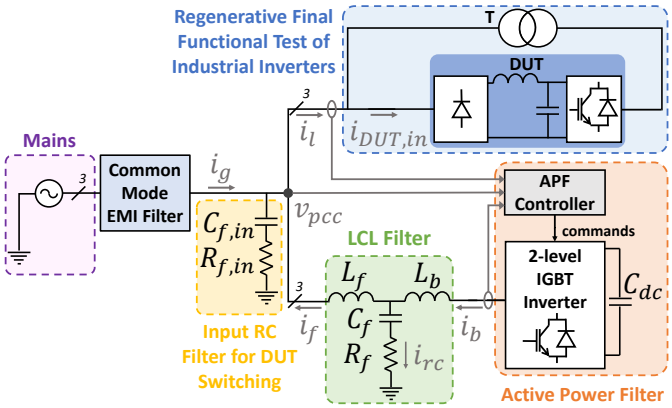


Fig. 1. Scheme of a shunt-type APF in parallel to a regenerative system used for the final functional tests of industrial inverters.

While improving the power quality, the installation of the APF leads to an increase of the active power absorption at the point of common coupling (PCC) due to the converter losses. Therefore, the APF efficiency has to be maximized to reduce the impact on power line consumption and the use of discontinuous pulse width modulation techniques (DPWMs) is a valid solution to achieve this goal. Indeed, DPWMs for 2-level 3-phase inverters are well-known to reduce the switching losses and each technique is optimized for a specific power factor value [4]. For any DPWM solution, the output of each inverter leg is clamped to the positive or negative rails of the DC-link for one third of the fundamental period (120°), thus eliminating the switching losses in the clamped phase. An uniform distribution of the switching losses between the power devices is obtained dividing the clamped region in two symmetrical sub-intervals of 60°, thus the leg output is clamped respectively to the positive and negative rails for the same period. Furthermore, the clamped intervals of each phase have to be located in the proximity of the positive and negative current peaks to perform the maximum switching losses reduction [5]. For a three-wire power converter, a suitable zero sequence voltage injection can be exploited to implement the discontinuous modulation [6]. Generalized DPWMs have been proposed in the literature to combine the standard DPWMs according to the output current [5] or the power factor [6]. However, these techniques are developed for

standard applications such as electrical drives [4-6] or active front-end (AFE) power converters [7-10], where the current low order harmonic content mainly consists of the fundamental frequency. For these applications, the power factor and the current vector position can be easily estimated and the optimal clamped interval for each phase is then computed. Instead, the APF has to provide multiple harmonic currents according to the non-linear load behavior. The current waveform differs from the sinusoidal wave and various current peaks may occur in a fundamental period. Therefore, the instantaneous phase shift between the voltage and current vectors is difficult to estimate. According to the above-mentioned reasons, the generalized DPWM methods based on the power factor and peak current estimation are not suitable to minimize the switching losses in an APF.

A generalized DPWM dedicated to APFs was proposed in [11]. This algorithm is performed each control period and determines which is the phase to be clamped according to the instantaneous values of the three phase reference voltages and currents. Thus, the switching losses are minimized with respect to continuous PWM solutions, such as the space vector pulse width modulation (SVPWM). However, this solution was only validated in laboratory conditions using a three-phase diode rectifier as non-linear load, where the inductive or capacitive behaviors were alternatively obtained by changing the dc output configuration. Therefore, some challenges inherent to the installation of the APF in an industrial plant have not been considered. Indeed, this method is highly sensitive to the noise on the line currents in disturbed environments, such as the regenerative system considered as case study (Fig. 1). The DUT injects high frequencies disturbances into the mains due to the commutations of its inverter switches. This noise is imposed over the low order harmonic currents absorbed by the load and acquired by the APF line sensors, thus affecting the computation of the zero sequence voltage. Indeed, unwanted repetitive changes of the clamped phase may occur, resulting in an increase of the high frequency common mode voltage and a reduction of the APF efficiency. The circulating common mode current causes the grid current distortion, safety issues, increase of the system losses and electromagnetic interference [**?**-13]. Therefore, as shown in Fig. 1, a grid-side common mode filter has to be installed to limit such currents. A reduction of the high frequency common mode voltage benefits the filter design, leading to the common mode choke losses and size minimization. [14-15].

To overcome the limits of the methods available in the literature, this paper proposes an improved generalized DPWM solution that is robust against line high frequency disturbances affecting APFs operating in industrial applications. The proposed solution (APF-GDPWM) reduces the common mode voltage that is injected into the grid. Moreover, when applied to a standard 2-level IGBT inverter connected to the grid through a differential mode LCL filter, it allows the doubling of the switching frequency with respect to the SVPWM without changing the thermal converter design. The doubling of the switching frequency has the big benefit of the increase of the dynamic APF performance due to the higher regulation bandwidth, resulting in better compensation of the distorted currents [16]. Furthermore, the LCL filter size and losses are minimized, while meeting the harmonic attenuation requirements [17-20]. This paper is organized as follows. Section II provides the description of the proposed modulation technique. Moreover, the effects of the implemented solution on the common mode voltage injection are investigated. In Section III the power devices losses are analyzed according to the non-linear load operation. The effectiveness of the APF-GDPWM in improving the converter efficiency is thus demonstrated. The experimental results for an APF connected in parallel to a production line are reported in Section IV. Section V concludes the paper.

II. APF-GDPWM Algorithm

The proposed APF-GDPWM is based on the common mode computation algorithm reported in Fig. 2. The inputs of the algorithm consist of the reference voltages v^*_{abc} and currents i^*_{abc}. The reference voltages v^*_{abc} are obtained as output of the current control regulators, while the reference currents i^*_{abc} are computed by removing the active current component at the fundamental frequency from the line current measurement. The reference voltage components v^*_a, v^*_b and v^*_c are compared to find which are the maximum (v_x) and the minimum (v_y) phase voltages and consequently their corresponding phase reference currents are defined as i_x and i_y. The voltages v_x and v_y can be respectively clamped to the positive and negative rails of the DC-link, while the clamping of the remaining phase is not allowed. The maximum linearity range is thus guaranteed. The maximum switching losses reduction is obtained in each control period if one of the phases v_x or v_y, working with the highest reference current as absolute value, is clamped to the positive ($\frac{V_{dc}}{2}$) or negative ($-\frac{V_{dc}}{2}$) rail. As shown in Fig. 3, six clamping sectors can be thus identified for the reference volatages v^*_a, v^*_b and v^*_c. The APF output phase voltage is assumed as sinusoidal, even if it provides multiple harmonic currents. Indeed, the fundamental components of the APF reference voltages are dominant and they must balance the grid voltage that can be considered as sinusoidal. A small amount of voltage is provided to compensate for the higher current frequencies proportionally to the line impedance. For each sector, the phases allowed to be clamped to the positive and negative rails are reported in Table I.

However, high frequencies current disturbances circulate in power lines, i.e. the current ripple due to the commutations of the DUT in the system of Fig. 1. The frequencies of these current disturbances are very often in the range defined by the APF control bandwidth and the sampling frequency, so they cannot be removed or compensated through software filtering. These disturbances, combined with a non negligible sensitivity of the line sensors, affect the current reference and then the zero sequence voltage computation. Indeed, when the absolute values of i_x and i_y are close to each other, the repetitive change of the clamped phase may occur. Therefore, a hysteresis selector is introduced to avoid the negative effect

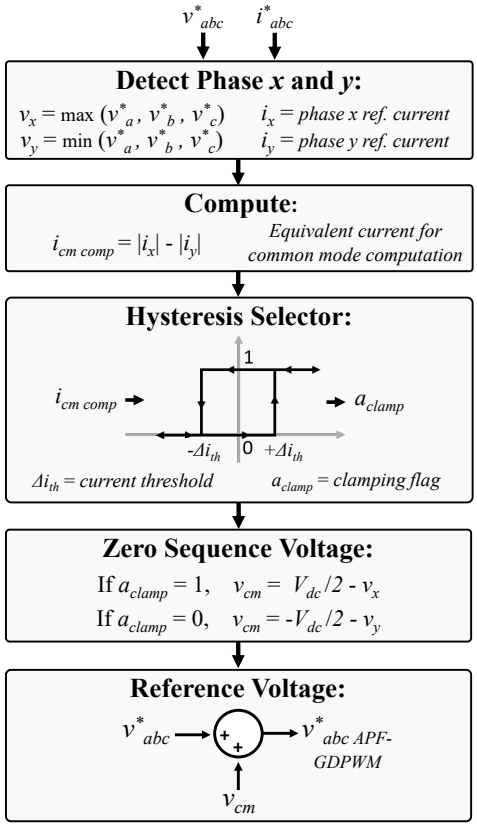


Fig. 2. APF-GDPWM algorithm for the zero sequence voltage computation.

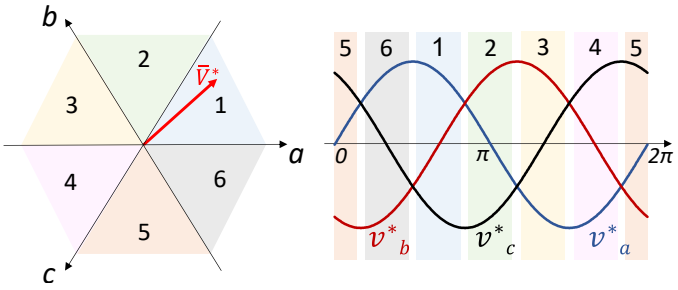


Fig. 3. Voltage space vector diagram divided in six clamping sectors.

mentioned above. An equivalent common mode computation current $i_{cm\ comp}$ is defined as the difference between the absolute values of i_x and i_y. A change of the clamped pole is executed only if it exceeds a threshold $\pm\Delta i_{th}$, that is tuned considering the current sensors sensitivity and the noise amplitude.

The noise effect on the zero sequence voltage is illustrated in Fig. 4. A constant 4 kHz disturbance with a 5% amplitude of the peak reference current is injected into the line while the APF is compensating the 5th and 7th harmonic order provided by a capacitive non-linear load (current total harmonic distortion THD_i = 102%). The sampling frequency of the power converter is 16 kHz. The clamping region n° 6 is highlighted and the algorithm computation in this interval is analyzed. For a wide range i_a^* and i_b^*, corresponding respectively to i_x and

TABLE I
PHASE VOLTAGE CLAMPING SECTORS

Sector	*Positive clamped phase* (v_x)	*Negative clamped phase* (v_y)
1	v_a	v_c
2	v_b	v_c
3	v_b	v_a
4	v_c	v_a
5	v_c	v_b
6	v_a	v_b

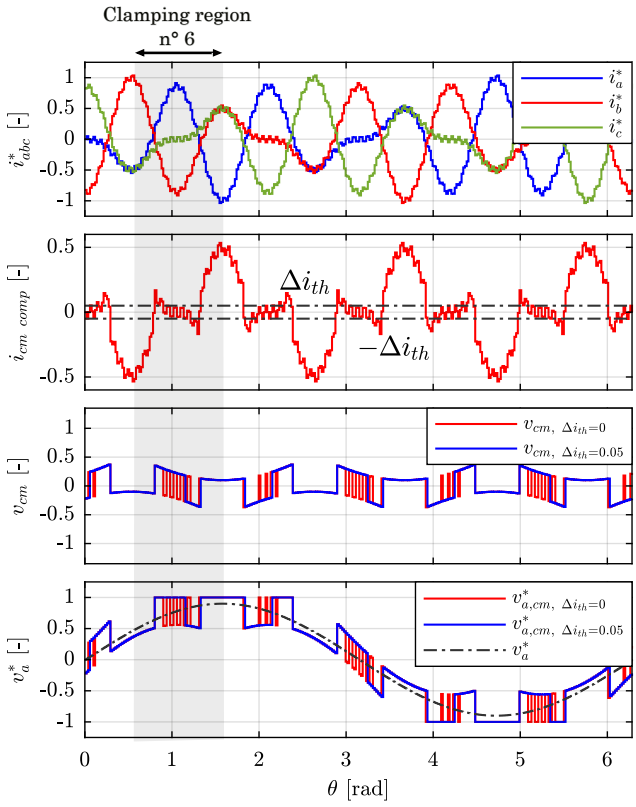


Fig. 4. APF operation with the proposed APF-GDPWM in presence of disturbances in the power lines. Currents and voltages are normalized. The clamping sector n° 6 is gray highlighted. From top to bottom: reference current, common mode computation current, zero sequence voltage and a reference voltage.

i_y, are similar in absolute values. It results in multiple zero crossings of $i_{cm\ comp}$, with a consequent repetitive change of clamped phase between v_a and v_b when Δi_{th} is null and the hysteresis selector is thus disabled. Instead, the side effect is eliminated by setting Δi_{th} to a comparable value with the noise amplitude. Therefore, the implementation of a hysteresis selector improves the robustness of the algorithm to disturbances on the line currents, thus avoiding unnecessary changes of clamping phase and a consequent injection of high frequency common mode voltage related to the zero sequence computation. Furthermore, the efficiency is increased since the number of switching transitions are minimized when the absolute values of i_x and i_y are similar.

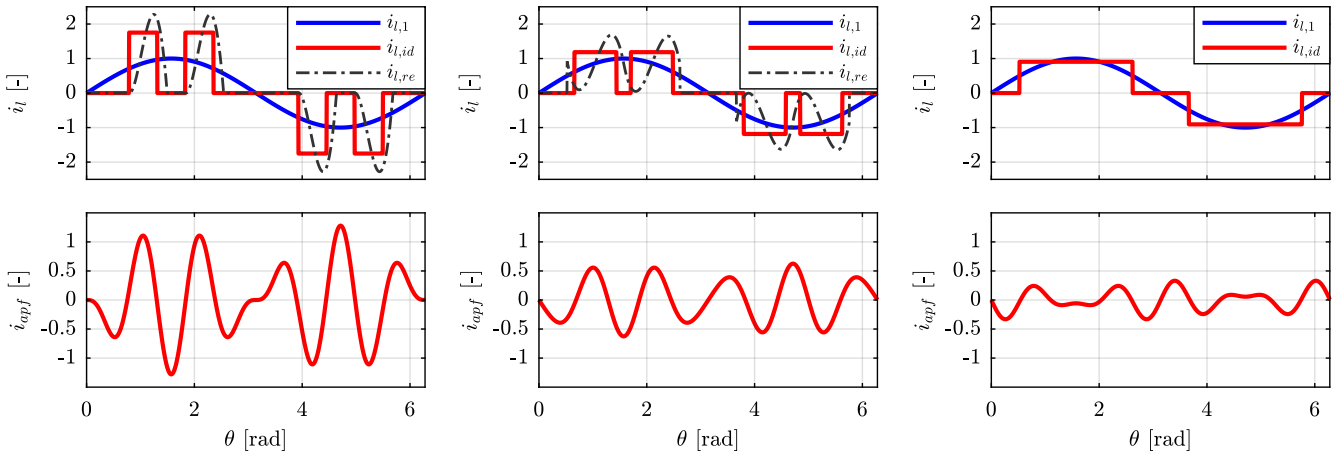


Fig. 5. 5th and 7th harmonic compensation of a non-linear load. From top to bottom: ideal load current ($i_{l,id}$) and its fundamental component ($i_{l,1}$), APF output current (i_{apf}). The currents are normalized with respect to the peak of $i_{l,1}$. (a) Rectifier with capacitive output $\left(\tau = \frac{\pi}{6}\right)$ and input $THD_i = 102\%$. (b) Rectifier with LC output $\left(\tau = \frac{\pi}{4}\right)$ and input $THD_i = 63\%$. (c) Rectifier with inductive output $\left(\tau = \frac{\pi}{3}\right)$ and input $THD_i = 31\%$. A real rectifier input current $i_{l,re}$ with the same THD_i and RMS of $i_{l,id}$ is also reported for (a) and (b).

III. Power Devices Losses

The conduction and switching losses for a 2-level PWM inverter for electrical drives have been exhaustively investigated in [4] and [6]. However, the results are not a priori extendable to an APF, where multiple harmonic currents are provided. The mean values of the conduction (P_c) and switching (P_{sw}) losses for a power device are obtained by integrating the instantaneous values over the fundamental period and the results are reported respectively in (1) and (2):

$$P_c = \frac{R_{on}}{2} \cdot I^2_{switch,rms} + \frac{V_{th}}{2} \cdot I_{switch,m} \tag{1}$$

$$P_{sw} = \frac{E_{sw,n}}{V_{dc,n} \cdot I_n} \cdot f_{sw} \cdot V_{dc} \cdot k_{sw} \cdot I_{switch,m} \tag{2}$$

where R_{on} and V_{th} are the power device on-resistance and threshold voltage; $E_{sw,n}$, $V_{dc,n}$, I_n are the reference (provided by datasheet) total energy loss, dc-link voltage and output current; f_{sw} is the switching frequency; V_{dc} is the dc-link voltage; $I_{switch,rms}$ and $I_{switch,m}$ are the RMS and mean current in the device.

The k_{sw} is the switching loss factor and relates the losses obtained with the APF-GDPWM and standard continuous pulse-width modulation techniques (CPWMs), as SVPWM:

$$k_{sw} = \frac{P_{sw,APF-GDPWM}}{P_{sw,CPWM}} \tag{3}$$

Differently from electric drives applications, P_c depends only on the current in the power devices. Indeed, neither the power factor, that is null, nor the output voltage (or the modulation index) affect the conduction losses. Instead, the P_{sw} formula remains unchanged. However, the relationship between $I_{switch,rms}$ and $I_{switch,m}$ is not unique (as in case of single harmonic control) and it is strictly dependent on the type of non-linear load to be compensated.

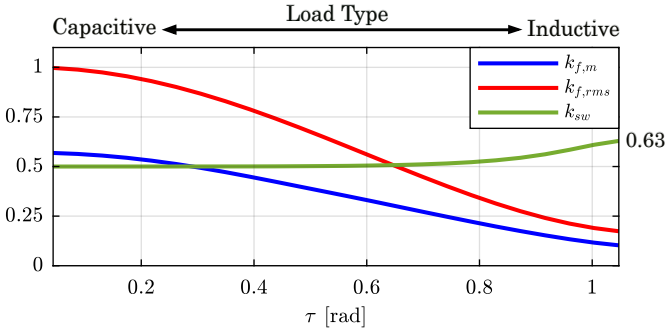


Fig. 6. The form factors $k_{f,m}$, $k_{f,rms}$ and k_{sw} according to the load typology.

Two form factors that relate the device and load currents are defined as:

$$\begin{cases} k_{f,m} = I_{switch,m}/I_{l,1,rms} \\ k_{f,rms} = I_{switch,rms}/I_{l,1,rms} \end{cases} \tag{4}$$

where $I_{l,1,rms}$ is the load RMS current at the fundamental frequency. Thus, (1) and (2) become:

$$P_c = \frac{R_{on}}{2} \cdot k^2_{f,rms} \cdot I^2_{l,1,rms} + \frac{V_{th}}{2} \cdot k_{f,m} \cdot I_{l,1,rms} \tag{5}$$

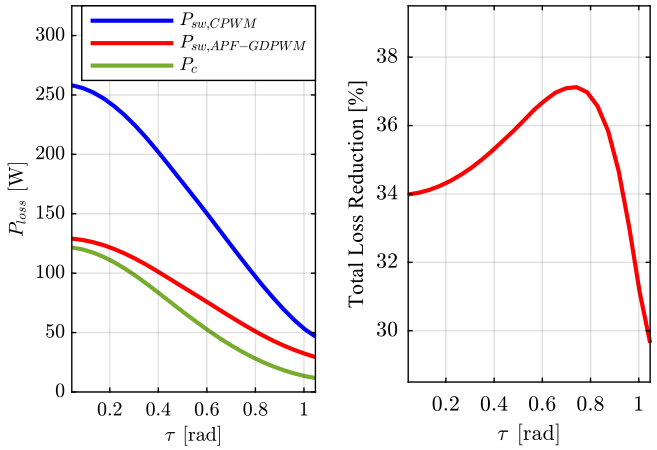
$$P_{sw} = \frac{E_{sw,n}}{V_{dc,n} \cdot I_n} \cdot f_{sw} \cdot V_{dc} \cdot k_{sw} \cdot k_{f,m} \cdot I_{l,1,rms} \tag{6}$$

For the same fundamental current absorbed by the non-linear load, the APF effort to compensate for the distortion increases in case of high form factor values.

TABLE II
CM660DX-24T1 DATA AND SYSTEM PARAMETERS FOR POWER LOSSES COMPUTATION

IGBT Electrical Data[a]				*System Parameters*	
R_{on}	2.2 mΩ	V_{th}	0.75 V	V_{dc}	750 V
$E_{on,n}$	53 mJ	$E_{off,n}$	56 mJ	$I_{l,1,rms}$	250 A_{rms}
$V_{dc,n}$	600 V	I_n	600 A	f_{sw}	8 kHz

[a] Data for junction temperature $T_{v,j}$ = 150 °C and gate-emitter voltage $V_{g,e}$ = 15 V



(a) (b)

Fig. 7. Power device losses for CM660DX-24T1 IGBT module according to the non-linear load typology. (a) Switching losses with CPMWs and APF-GDPWM, conduction losses. (b) Total losses reduction obtained with APF-GDPWM with respect to CPWMs.

The benefits of the proposed technique on the switching losses are analyzed for an APF compensating the 5th and 7th load harmonics produced by an ideal diode rectifier and described as:

$$i_{load}(n,\theta,\tau) = \sum_{n=1}^{\infty} \frac{4\sqrt{3}}{n\pi} \cdot \sin\left(n \cdot \frac{\tau}{2}\right) \cdot \sin\left(n \cdot \theta\right) \cdot K(n) \quad (7)$$

$$K(n) = \begin{cases} -1, & \text{if } n = 6k-1 \\ +1, & \text{if } n = 6k+1 \\ 0, & \text{otherwise} \end{cases} \quad ,\forall k \in \mathbb{N} \quad (8)$$

Non-linear capacitive and inductive behaviors are obtained respectively for $\tau \to 0$ and $\tau \to \frac{\pi}{3}$ (Fig. 5). The relationship between $k_{f,m}$, $k_{f,rms}$ and k_{sw} with the load typology is reported in Fig. 6. The maximum switching loss reduction of 50% (k_{sw} = 0.5) is obtained for capacitive loads, when the form factors and consequently the overall devices losses are higher. Similarly, a considerable switching loss reduction (37%) is obtained in case of inductive load, where k_{sw} is equal to 0.63.

The device losses computation is performed for the commercial CM660DX-24T1 IGBT module to show the effectiveness of APF-GDPWM on the overall losses reduction. The module

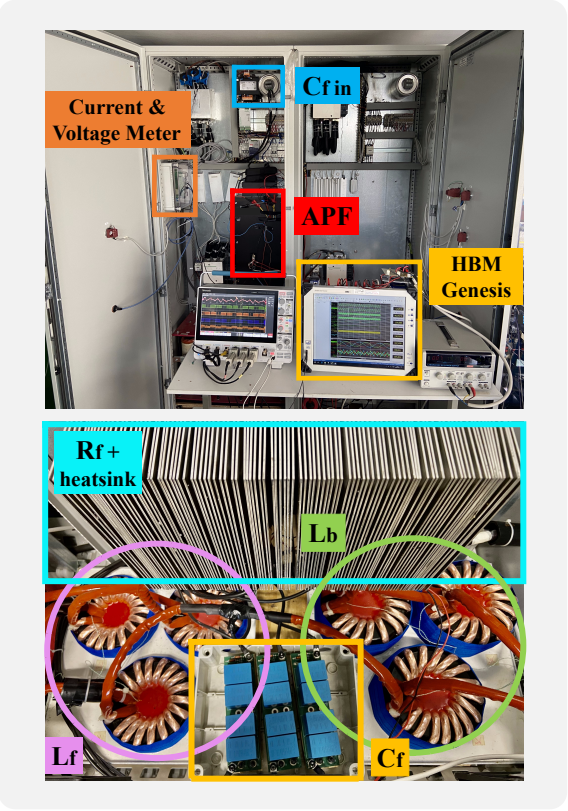


Fig. 8. System setup: APF cabinet with measuring equipment (top) and differential mode LCL filter (bottom).

TABLE III
SYSTEM PARAMETERS

APF		*LCL Filter*		*Grid*		*Reg. system*	
I_n	150 A_{rms}	L_b	75 µH	V_g	400 V_{rms}	P_{reg}	265 kW
S_n	100 kVA	L_f	40 µH	f_g	50 Hz	$C_{f,in}$	150 µF
V_{dc}	750 V	C_f	64 µF	$\tilde{L}_g$	20 µH	$R_{f,in}$	300 mΩ
C_{dc}	2.2 mF	R_f	200 mΩ				

electrical characteristics are taken from its datasheet and are reported in Table II with the other system data. As illustrated in Fig. 7, P_{sw} is the main contribution for the device losses. A minimization of the switching losses with APF-GDPWM results in a total loss reduction of 29.6-37.1% according to the non-linear load typology.

IV. EXPERIMENTAL RESULTS

The APF-GDPWM algorithm has been implemented on a 100 kVA 2-level inverter connected in parallel to a regenerative system through an LCL filter with the configuration reported in Fig. 1. The DUT is a 265 kVA power converter for electrical drives consisting of a diode three-phase rectifier with output LC filter in the AC/DC stage and a 2-level 3-phase IGBT inverter in the DC/AC stage. The THD_i of the current absorbed by the diode rectifier during the full-power operation

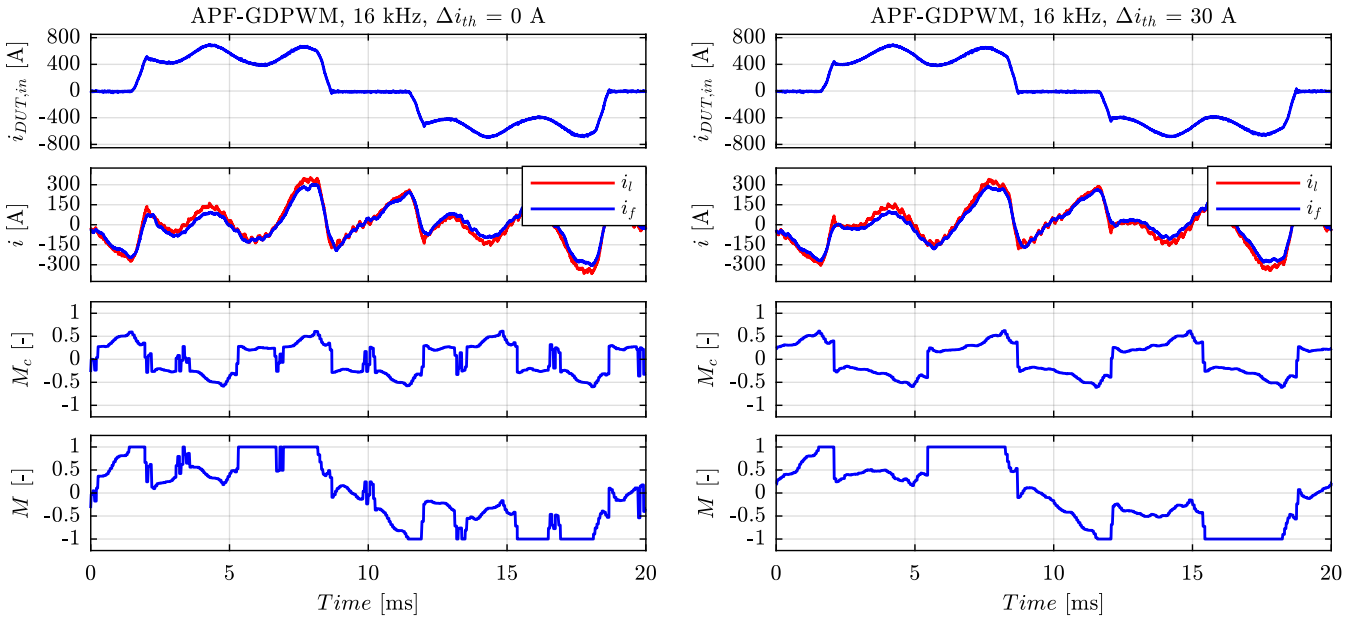


Fig. 9. APF steady-state operation with f_{sw} = 16 kHz and APF-GDPWM in case of hysteresis selector disabled (a) and enabled with Δi_{th} = 30 A (b). From top to bottom: current absorbed by the rectifier $i_{DUT,in}$, line and grid-side LCL filter current i_l and i_f, zero sequence modulation index M_c and phase modulation index M.

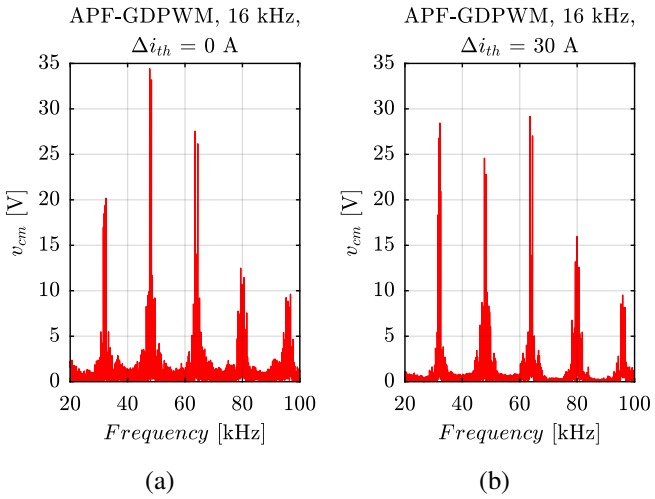


Fig. 10. High frequency common mode voltage injection with f_{sw} = 16 kHz and APF-GDPWM. (a) Hysteresis selector disabled (null Δi_{th}). (b) Hysteresis selector enabled and Δi_{th} = 30 A.

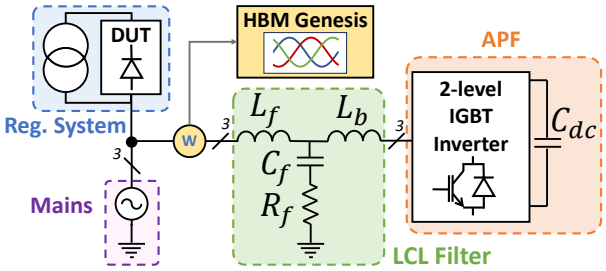


Fig. 11. Scheme of power losses measurement setup.

TABLE IV
MEASURED APF POWER LOSSES

Modulation	f_{sw} [kHz]	Δi_{th} [A]	P_{loss} [W]
SVPWM	8	-	1661
APF-GDPWM	16	30 A	1605

is 33%. The system setup is shown in Fig. 8, while Table III reports the main data.

The adopted APF control method is the one proposed in [21]. A 50 Hz proportional resonant regulator (P-Res) operating in stationary (α,β) reference frame is implemented to perform the fundamental current control and the DC bus voltage regulation. Instead, resonant regulators operating in synchronous (d,q) reference frame and rotating at the grid frequency are tuned at the harmonic orders $6k$, with $k = 1, 2....$ Each resonant regulator compensates for the $6k-1$ and $6k+1$ harmonics of negative and positive sequence, collapsing on the $6k$ harmonic in synchronous (d,q) reference frame. The controller computational effort to reach the desired harmonic compensation is thus minimized. The APF is tuned to compensate for the current distortion up to the 25th harmonic. It is the upper order the APF is able to properly compensate operating with a switching/sampling frequency of 8/16 kHz. The compensation capability is reduced for higher orders,

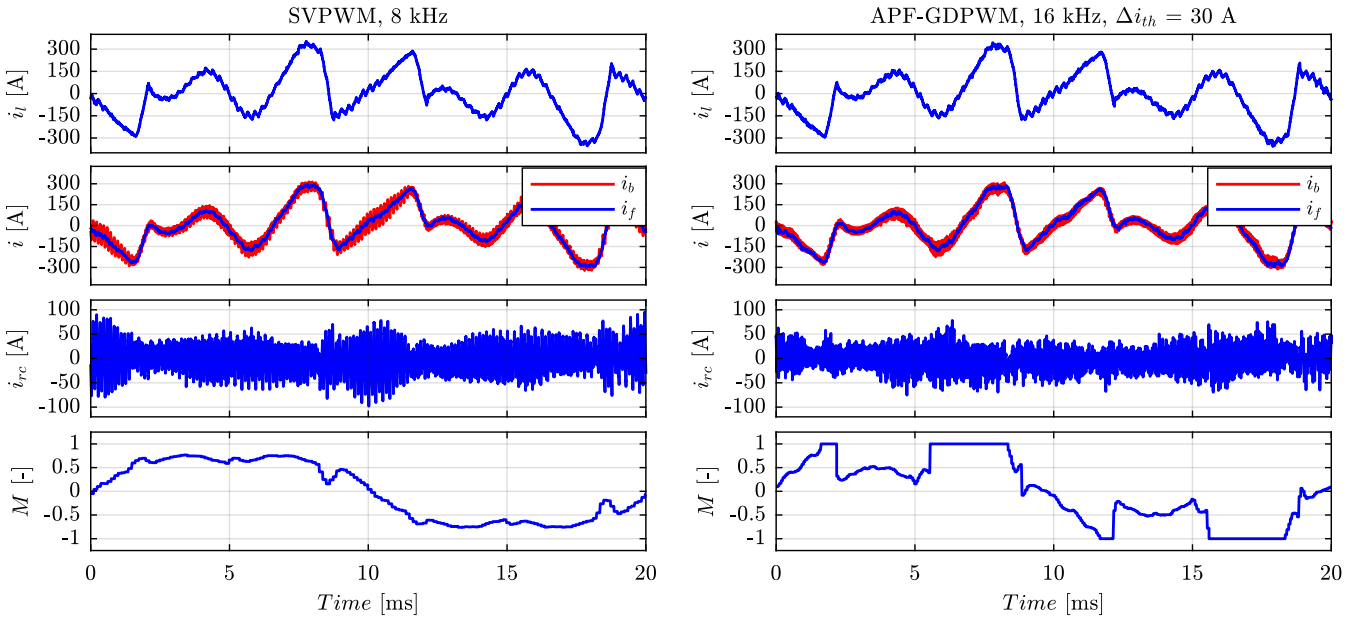


Fig. 12. APF steady state operation in case of SVPWM at f_{sw} = 8 kHz (a) and APF-GDPWM at f_{sw} = 16 kHz with Δi_{th} = 30 A (b). From top to bottom: line current i_l, APF output current i_b and grid-side current i_f, RC filter current i_{rc} and phase modulation index M.

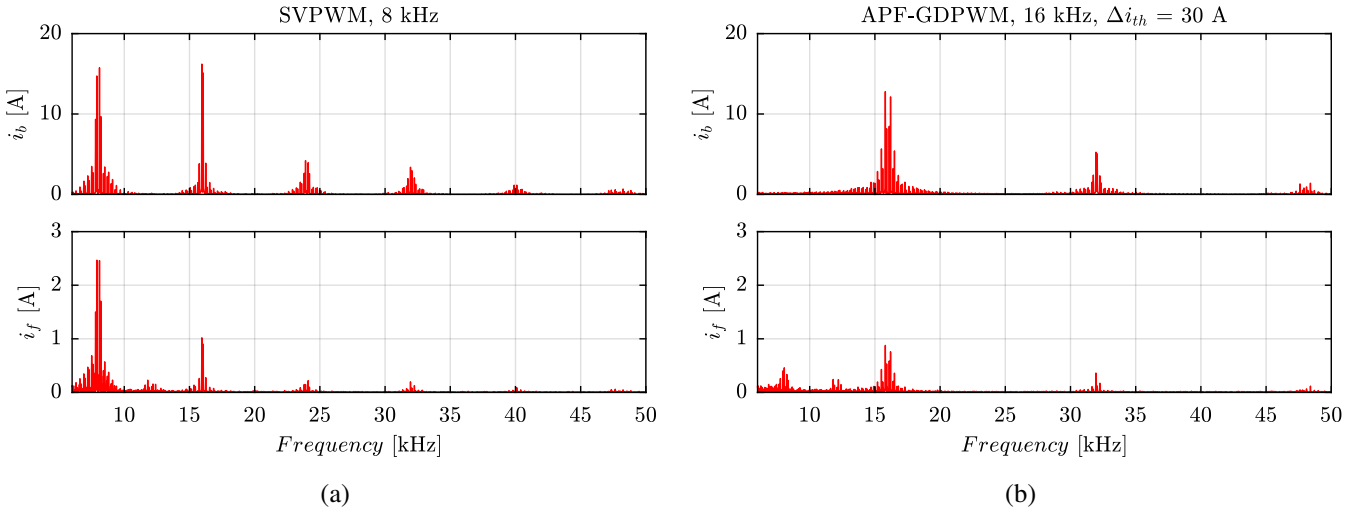


Fig. 13. High frequency harmonic content of APF output current i_b and grid-side current i_f. (a) SVPWM at f_{sw} = 8 kHz. (b) APF-GDPWM at f_{sw} = 16 kHz and Δi_{th} = 30 A.

since the number of acquired samples for every harmonic period is low.

The steady-state operation of the APF with APF-GDPWM and a switching frequency f_{sw} = 16 kHz is illustrated in Fig. 9 to demonstrate the effectiveness of the hysteresis selector. When the hysteresis selector is disabled (Δi_{th} is null), the unwanted repetitive changes of the clamped phase occur many times in a fundamental period. The side effect is completely eliminated by setting Δi_{th} = 30 A. The benefits of the hysteresis selection on the high frequency common mode voltage limitation are shown in Fig. 10. With a null Δi_{th}, the injected common mode voltage in the range 20-100 kHz is $V_{rms,20-100kHz}$ = 71.7 V_{rms}. By enabling the hysteresis selector with Δi_{th} = 30 A, the same RMS voltage is reduced of 7% ($V_{rms,20-100kHz}$ = 66.7 V_{rms}). Furthermore, the maximum voltage peak in the analyzed spectrum is reduced.

The overall power converter losses are measured by an HBM Genesis data recorder, connected between the LCL filter

and the grid to evaluate both the inverter and LCL filter losses (Fig. 11). Power measurements have been performed for two different operation conditions: SVPWM and f_{sw} = 8 kHz, APF-GDPWM with Δi_{th} = 30 A and f_{sw} = 16 kHz. The obtained results are reported in Table IV. Thanks to APF-GDPWM, the switching frequency of the grid converter can be doubled without increasing the total losses. Indeed, the measured losses for the converter operating at f_{sw} = 8 kHz using SVPWM are slightly higher than the losses obtained with the converter operating at f_{sw} = 16 kHz with APF-GDPWM. An overall converter loss reduction is obtained although the regenerative system is an inductive non-linear load (THD_i = 33%) and the switching losses reduction is less effective in this case, as demonstrated in Section III. Notably, the application of APF-GDPWM reduces also the losses in the LCL filter. Indeed, the current absorbed by the RC filter $I_{rc,rms}$ is 28.6 A_{rms} in case of SVPWM at f_{sw} = 8 kHz, while it is reduced to 20.4 A_{rms} with APF-GDPWM at f_{sw} = 16 kHz. The filter losses were not considered in the theoretical discussion and their reduction further validates the effectiveness of the proposed solution. The APF steady-state operation for the two test conditions is reported in Fig. 12, while the harmonic content of the APF output current (i_b) and the grid-side current (i_f) (as defined in Fig. 1) is shown in Fig. 13. The doubling of the switching frequency allows the reduction of the high frequency content injected into the mains by the APF. The LCL filter current stress is reduced since the amount of i_b high frequency content to be filtered is lower. An unexpected 8 and 12 kHz harmonic content is measured in i_f, but not in i_b, both in case of SVPWM and APF-GDPWM. This contribution is related to a part of the DUT switching ripple at 4 kHz that sinks in the RC branch of the LCL filter.

V. Conclusion

This paper proposes an improved discontinuous modulation technique (APF-GDPWM) suitable for APFs operating in disturbed environments. Thanks to the introduction of a hysteresis selection in the zero sequence voltage computation algorithm, the unwanted repetitive changes of clamped phase are avoided and the high frequency common mode voltage injection is minimized. The power devices losses for an APF are analytically computed according to the non-linear load operation, both for CPWMs and the proposed APF-GDPWM. The theoretical results demonstrate the effectiveness of the proposed method in improving the power converter efficiency. The experimental tests, carried out on an industrial 2-level IGBT APF, have shown the APF-GDPWM provides a better exploitation of the existing hardware by doubling the switching frequency from 8 kHz to 16 kHz, with the benefit of current ripple reduction. The LCL filter can be minimized in size and cost, while ensuring the same compensation performances. Moreover, the control bandwidth may be increased, thus resulting in a better dynamic performance and higher harmonic orders compensation. Therefore, the 2-level configuration may become competitive with respect to more expensive solutions, such as 3-level inverters.

References

[1] W. M. Grady, M. J. Samotyj and A. H. Noyola, "Survey of active power line conditioning methodologies," *IEEE Trans. Power Del.*, vol. 5, no. 3, pp. 1536-1542, Jul. 1990.

[2] H. Akagi, "New trends in active filters for power conditioning," *IEEE Trans. Ind. Appl.*, vol. 32, no. 6, pp. 1312-1322, Nov.-Dec. 1996.

[3] B. Singh, K. Al-Haddad and A. Chandra, "A new control approach to three-phase active filter for harmonics and reactive power compensation," *IEEE Trans. Power Syst.*, vol. 13, no. 1, pp. 133-138, Feb. 1998.

[4] J. W. Kolar, H. Ertl and F. C. Zach, "Influence of the modulation method on the conduction and switching losses of a PWM converter system," *IEEE Trans. Ind. Appl.*, vol. 27, no. 6, pp. 1063-1075, Nov.-Dec. 1991.

[5] T. D. Nguyen, J. Hobraiche, N. Patin, G. Friedrich and J. -P. Vilain, "A Direct Digital Technique Implementation of General Discontinuous Pulse Width Modulation Strategy," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4445-4454, Sept. 2011.

[6] A. M. Hava, R. J. Kerkman and T. A. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1059-1071, Sept.-Oct. 1998.

[7] B. Ciftci and A. M. Hava, "Performance evaluation and selection of PWM switching and control methods for grid connected modular multilevel converters," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, Canada, 2015, pp. 3622-3629.

[8] H. Xu, L. Xu, K. Wang, Z. Zheng and Y. Li, "Switching Losses Reduction of Grid-tied Inverters With Variable Switching Frequency Discontinuous PWM," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 1567-1573.

[9] Z. Jankovic, P. Murthy, L. Wei and A. Nasiri, "Dynamic Discontinuous PWM for Grid-tied Inverter Applications," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, 2020.

[10] P. Karamanakos, M. Nahalparvari and T. Geyer, "Fixed Switching Frequency Direct Model Predictive Control With Continuous and Discontinuous Modulation for Grid-Tied Converters With LCL Filters," *IEEE Trans. Control Syst. Technol.*, vol. 29, no. 4, pp. 1503-1518, Jul. 2021.

[11] L. Asiminoaei, P. Rodriguez and F. Blaabjerg, "Application of Discontinuous PWMModulation in Active Power Filters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1692-1706, Jul. 2008.

[12] O. Lopez et al., "Eliminating Ground Current in a Transformerless Photovoltaic Application," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 140-147, Mar. 2010.

[13] M. C. Cavalcanti, K. C. de Oliveira, A. M. de Farias, F. A. S. Neves, G. M. S. Azevedo and F. C. Camboim, "Modulation Techniques to Eliminate Leakage Currents in Transformerless Three-Phase Photovoltaic Systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 4, pp. 1360-1368, Apr. 2010.

[14] H. Akagi, H. Hasegawa and T. Doumoto, "Design and performance of a passive EMI filter for use with a voltage-source PWM inverter having sinusoidal output voltage and zero common-mode voltage," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1069-1076, Jul. 2004.

[15] S. Gulur, V. Mahadeva Iyer and S. Bhattacharya, "A CM Filter Configuration for Grid-Tied Voltage Source Converters," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8100-8111, Oct. 2020.

[16] C. Lascu, L. Asiminoaei, I. Boldea and F. Blaabjerg, "High Performance Current Controller for Selective Harmonic Compensation in Active Power Filters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1826-1835, Sep. 2007.

[17] M. Liserre, F. Blaabjerg and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1281-1291, Sep.-Oct. 2005.

[18] E. Kantar and A. M. Hava, "Optimal Design of Grid-Connected Voltage-Source Converters Considering Cost and Operating Factors," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5336-5347, Sep. 2016.

[19] Q. Liu, L. Peng, Y. Kang, S. Tang, D. Wu, Y. Qi, "A Novel Design and Optimization Method of an LCL Filter for a Shunt Active Power Filter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 4000-4010, Aug. 2014.

[20] D. Cittanti, F. Mandrile, M. Gregorio and R. Bojoi, "Design Space Optimization of a Three-Phase LCL Filter for Electric Vehicle Ultra-Fast Battery Charging," *Energies* 2021.

[21] R. I. Bojoi, G. Griva, V. Bostan, M. Guerriero, F. Farina and F. Profumo, "Current control strategy for power conditioners using sinusoidal signal integrators in synchronous reference frame," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1402-1412, Nov. 2005.