TCAD-based Pseudo-Common-Gate X-PAR Model for GaAs Stacked Power Amplifier Design

TCAD-based Pseudo-Common-Gate X-PAR Model for GaAs Stacked Power Amplifier Design

Chiara Ramella, Simona Donati Guerrieri, Marco Pirola
DET - Politecnico di Torino, Turin, Italy
ORCID: 0000-0003-0634-1474 (C.R.), 0000-0002-1204-7047 (S.D.G) and 0000-0002-5759-9697 (M.P.)

***Abstract*—Series device stacking has proved to be a very interesting solution for developing high-voltage high-power microwave amplifiers in low-breakdown technologies. The availability of 3-terminal device nonlinear models that are accurate and reliable, yet computationally efficient, in simulating a pseudo-common-gate stage are of crucial importance for developing a stacked power amplifier. This work presents the extraction and validation of a 3-terminal X-parameter model of a GaAs MESFET from physics-based simulations. Remarkable accuracy can be obtained by properly selecting the port terminations, accounting for the peculiar circuit scheme adopted for model extraction.**

***Index Terms*—GaAs, device modeling, X-parameters, stacked power amplifier**

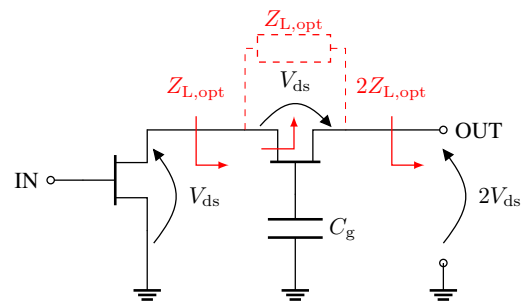


Fig. 1: Architecture of a 2-stacked-FET PA.

I. Introduction

The stacked power amplifier (PA) series power combination technique [1] can be profitably exploited in high-frequency GaAs technology [2]–[6], as a solution for overcoming the breakdown voltage limit and developing high-voltage and high-power MMICs. Moreover, it overcomes the main limitation of the classical parallel combining approach, i.e. the decrease of the optimum impedance with the increasing number of transistors, which affects the achievable bandwidth due to a larger impedance ratio with the external load. Developing compact stacked macro-cells providing high output power and improved gain in a footprint which is still comparable to that of a single multi-finger transistor [2], can be the key solution for keeping GaAs technology in a leading position with respect to GaN, with advantages in terms of reliability, linearity and maximum operating frequency.

In the 2-stacked FET architecture (Fig. 1), a common-source (CS) device is coupled in series with a pseudo-common-gate (CG) one, where the gate terminal is not grounded but loaded by a gate capacitance C_{g}. To let both the CS and CG stages reach full drain-source voltage swing, the optimum impedance $Z_{\mathrm{L,opt}}$ must be synthesized simultaneously at the input of the CG stage and across its drain-source terminals, when loaded with $2Z_{\mathrm{L,opt}}$, by adjusting the gate capacitance and the optional inter-stage matching elements that may be required for parasitic reactances compensation at high frequency [7], [8]. Therefore, the design of a stacked PA relies on the availability of 3-terminal nonlinear device models which provide accurate and reliable results when adopted in CG configuration, which currently represents a key issue. In fact, many commercially available foundry models are 2-terminal equivalent circuits, with internally grounded source. Even when the source terminal is available, model parameters are typically extracted and optimized to match CS device measurements, and, at least in principle, there is no guarantee that such model are also accurate when used for simulating in large-signal a CG stage, especially a pseudo-CG one where the estimation of the total nonlinear gate capacitance is crucial for the design of C_{g}.

Physics-based simulation with technology CAD (TCAD) tools can provide a highly accurate device model, and in previous works [9], [10] we stressed out how X-parameters (Xpar) are the ideal tool to interface advanced/ad-hoc device analysis tools, like TCAD, and commercial high-frequency CAD tools. In particular, we demonstrated that Xpars extracted from TCAD simulations are simultaneously highly computationally efficient and highly accurate in analyzing the device sensitivity with respect to load variations [9]. Nonetheless, the adoption of Xpar models for device-level modeling and circuit optimization requires some care with respect to conventional system-level modeling [11], [12], especially in a non-standard configuration as the CG.

In this contribution, we present the extraction and validation of a 3-terminal Xpar model of a GaAs device from physical simulations in pseudo-common-gate configuration, adopting an in-house developed TCAD tool and Xpar extraction procedure [13], [14]. The model then is validated against physical simulations, also varying C_{g} or adding a matching inductance, demonstrating remarkable accuracy.

II. Device model extraction

The adopted device is the $0.5\,\mu$m gate-length epitaxial MESFET with 1 mm total gate-periphery already adopted in previous works [10]. The optimum drain-source voltage is $V_{\mathrm{DS}} = 8\,\mathrm{V}$: accounting for a $5\,\Omega$ gate stabilization resistance, preliminary CS physical simulations at 12 GHz and 30 % class-

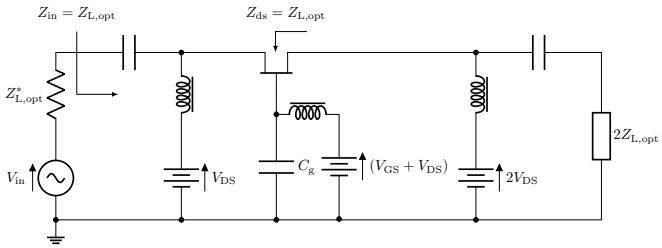


Fig. 2: Pseudo-common-gate stage in a 2-stacked FET PA.

AB bias (90 mA) give an optimum load $Z_{\rm L,opt} = (47 + j11)\,\Omega$, a transconductance $g_{\rm m} = 80$ mS and a gate-source capacitance $C_{\rm gs} = 0.7$ pF. The circuit adopted to extract the FET model in pseudo-CG configuration is shown in Fig. 2: to emulate the operation within a stacked PA, the source must be set at the operating $V_{\rm DS}$, while the drain at twice this value (16 V) to accommodate for maximum voltage swing of both stages. The quiescent drain current is determined by the CS stage, through its $V_{\rm GS}$, while the CG stage must allow the same current to flow, thus the DC gate voltage must be $V_{\rm GS} + V_{\rm DS}$. In this case, $V_{\rm GS} = -2$ V, thus the CG gate is biased at 6 V. Finally, the output load should be $2Z_{\rm L,opt}$. Then, according to the classic stacked PA theory derived for purely real impedances, the gate capacitance should be set to

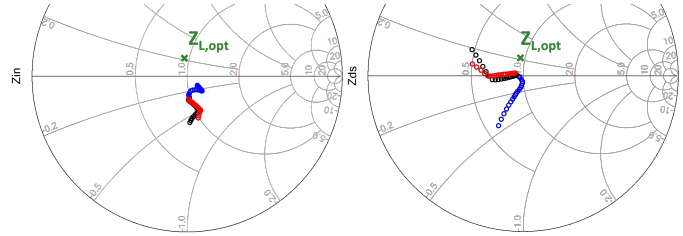
$$C_{\rm g} = \frac{C_{\rm gs}}{g_{\rm m} R_{\rm L,opt} - 1} \approx 0.22\,\text{pF} \qquad (1)$$

i.e., $Z_{C_{\rm gs}} \approx -j60\,\Omega$ at 12 GHz, to achieve the desired inter-stage matching. Clearly, in case of complex impedances, $C_{\rm g}$ can match only the real part of $Z_{\rm L,opt}$, while the imaginary part requires additional elements to match the optimum CS reactance [2], [6], which is typically inductive at high frequency.

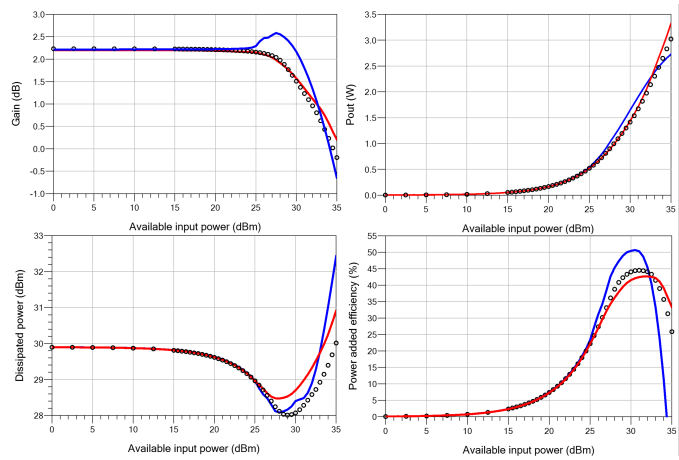
A. Physical simulation

Physics-based simulations of the MESFET in CG configuration have been carried out using our in-house code implementing the Harmonic Balance algorithm. It allows mixed-mode simulations of complete microwave stages, including multiple active devices [15]. As such, all the device terminals are independent and referenced to the external circuit common reference potential, hence it represents an ideal simulation environment for the extraction of 3-terminal model needed for the CG stage. Xpars are extracted from the admittance conversion matrices of the physics-based small-signal/large-signal analysis, sweeping the available input power from -10 dBm to roughly 2 dB of gain compression, and stored in a standard *.xnp* file counting 6 ports (3 DC + 3 RF).

X-parameters are a variational model whose accuracy critically depends on the extraction point, which needs to be close enough to the expected operating conditions. Hence, the Xpar model has been extracted with the device terminated on ideal loads whose values are close to those required in the ideal CG stage. Considering the circuit of Fig. 2, the source and drain port terminations were set to $\Re e\{Z^*_{\rm L,opt}\}$ and $2\Re e\{Z_{\rm L,opt}\}$, respectively, hence neglecting the imaginary part of the optimum load. The gate RF port is the most critical: the expected termination is almost purely capacitive but, accounting also for the $5\,\Omega$ stabilization resistance considered in the CS case, the complex impedance $(5 - j60)\,\Omega$ was selected. For comparison, a second Xpar model has been extracted with standard $50\,\Omega$ termination at all RF ports.



(a) Input and drain-source impedances. The green cross is the optimum impedance for power matching.



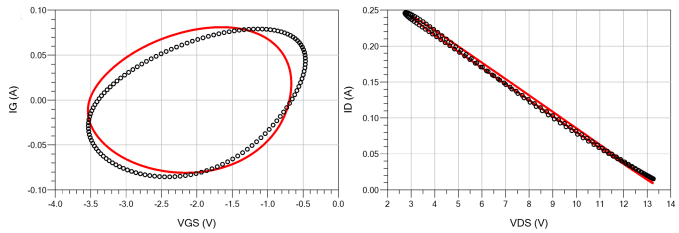
(b) RF performance: transducer gain, output power, dissipated power and power added effciency.

Fig. 3: Comparison, at nominal operating conditions, among TCAD simulation (black) and the two Xpar models extracted with selected (red) and standard ($50\,\Omega$, blue) terminations. Power levels are reported in linear units to better highlight the accuracy of the model.

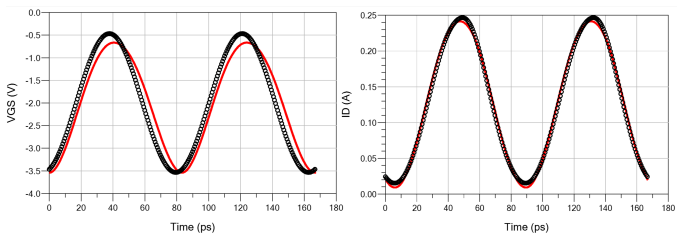
III. Model validation

The pseudo-CG stage of Fig. 2 has been simulated in ADS with the Xpar model adopting the nominal terminations: $Z^*_{\rm L,opt}$ source impedance, $2Z_{\rm L,opt}$ load and 0.22 pF $C_{\rm g}$, with harmonic shorts enforced at all ports. The results have been validated against physical simulations of the MESFET with the same loads.

The two extracted Xpar models are compared in Fig. 3: as expected form the local nature of the X parameters, the "standard" Xpar model extracted with $50\,\Omega$ loads is much less accurate than the model extracted with terminations close, but not equal, to the operating ones [9]. The latter, considered hereafter, compares very well to physical simulations in terms of impedance levels, which are key parameters to be optimized for stacked PA operation, and RF performance up to 2 dB of



(a) Gate-source and drain-source load-lines.



(b) Gate-source voltage and drain current waveforms.

Fig. 4: Comparison, at nominal operating conditions, between TCAD simulation (black) and Xpar model: time-domain simulation results at $P_{\mathrm{out}} = 28\,\mathrm{dBm}$.

gain compression, which is a typical/reasonable level of nonlinearity for a GaAs design. Good agreement is obtained also in reproducing time-domain waveforms, as reported in Fig. 4. Notice that, as expected from the stacked PA theory [1], only the real part of Z_{in} and Z_{ds} (see Fig. 2) is matched to the optimum value, therefore, the transducer gain obtained is only 2.2 dB, against a maximum ideal value of 3 dB.

To asses the robustness of the proposed Xpar model on load conditions different from the nominal ones, we simulated the CG stage with a variation of $\pm 20\,\%$ of C_{g}: the results are shown in Fig. 5. As expected C_{g} sensibly impacts on matching and thus transducer gain, hence should be optimized for stacked PA design. Considering the large C_{g} variation, the model accuracy with respect to TCAD simulation is satisfactory, especially in terms of impedance levels, which are paramount for design. A more accurate model, allowing for even larger C_{g} swing, may be obtained with parameterized X-parameters [16] extracted with different gate terminations, corresponding to selected C_{g} values.

As a final verification, and first step towards the use of the model for stacked PA design, we developed a simple inductance-based matching network to match the imaginary part of Z_{in} to $\Im m\{Z_{\mathrm{L,opt}}\}$ at $P_{\mathrm{out}} = 28\,\mathrm{dBm}$. As shown in Fig. 6, the simulated input impedance at this power level is very close to the constant-resistance circle passing through $Z_{\mathrm{L,opt}}$ (green dotted line), thus the easiest matching option is to insert just a series inductance of $0.35\,\mathrm{nH}$ at the CG input port [8]. Although this represents a deviation of the source termination with respect to extraction one, the results obtained with the Xpar model, compared to physical simulations, demonstrate again a very good agreement, as reported in Fig. 7. As expected, the inductance matches the imaginary part of Z_{in}, while it has nearly no effect on Z_{ds}.

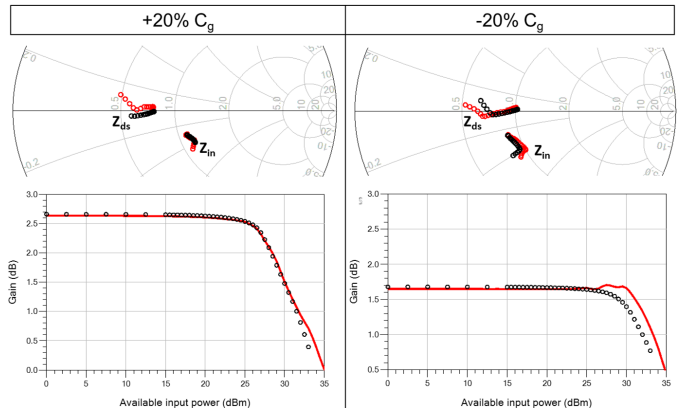


Fig. 5: Comparison between TCAD simulation (black) and Xpar model (red) with $+20\,\%$ (left) and $-20\,\%$ (right) gate capacitance variations: input and drain-source impedances (top) and transducer gain (bottom).

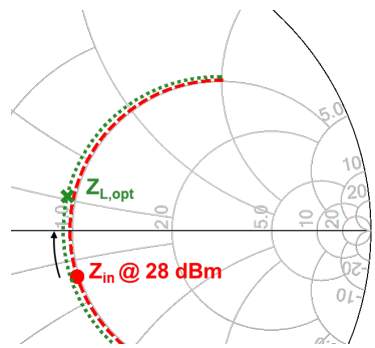


Fig. 6: Matching of the imaginary part of the input impedance with a series inductance that rotates the impedance clockwise along a constant-resistance circle (red dasehd line).

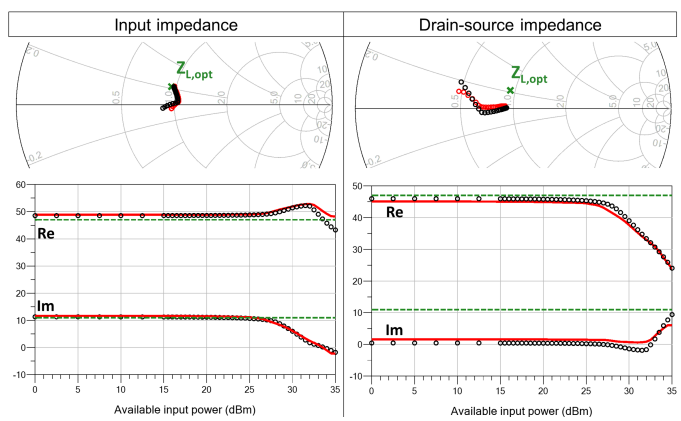


Fig. 7: Comparison, at nominal operating conditions, between TCAD simulation (black) and Xpar model (red). The green cross and dashed lines indicate the optimum impedance for power matching.

IV. Conclusion

We reported the extraction and validation of a physics-based 3-terminal X-parameter model of a GaAs MESFET in pseudo-

common-gate configuration. As highlighted in this work, the selection of the port terminations for model extraction is crucial and must account for the peculiar operating conditions of the device. Very good agreement of the selected X-parameter model with physical simulation is demonstrated, opening the way to its potential use for the design of stacked and, in general, non-common-source-based PA architectures.

REFERENCES

[1] A. K. Ezzeddine, H. C. Huang, and J. L. Singer, "UHiFET - a new high-frequency High-Voltage device," in *IEEE IMS 2011*, Jun 2011, pp. 1–1.

[2] T. Fersch *et al.*, "Stacked GaAs pHEMTs: Design of a K-band power amplifier and experimental characterization of mismatch effects," in *IEEE IMS 2015*, 2015, pp. 1–4.

[3] D. P. Nguyen and A. Pham, "An Ultra Compact Watt-Level Ka-Band Stacked-FET Power Amplifier," in *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 7, Jun 2016, pp. 516–518.

[4] F. Thome *et al.*, "Broadband High-Power W-Band Amplifier MMICs Based on Stacked-HEMT Unit Cells," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 3, pp. 1312–1318, March 2018.

[5] A. Piacibello *et al.*, "A Ku-band Compact MMIC PA based on Stacked GaAs pHEMT cells," in *INMMiC 2018*, 2018, pp. 1–3.

[6] G. van der Bent, P. de Hek, and F. E. van Vliet, "Design Procedure for Integrated Microwave GaAs Stacked-FET High-Power Amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 9, pp. 3716–3731, 2019.

[7] H. Dabag *et al.*, "Analysis and Design of Stacked-FET Millimeter-Wave Power Amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1543–1556, April 2013.

[8] C. Ramella *et al.*, "Space-Compliant Design of a Millimeter-Wave GaN-on-Si Stacked Power Amplifier Cell through Electro-Magnetic and Thermal Simulations," *El.*, vol. 10, no. 15, p. 1784, 2021.

[9] S. Donati Guerrieri *et al.*, "Global Assessment of PA variability through concurrent Physics-based X-parameter and Electro-Magnetic simulations," in *EuMIC 2020*, 2021, pp. 213–216.

[10] ——, "Bridging the Gap between Physical and Circuit Analysis for Variability-Aware Microwave Design: Modeling Approaches," *El.*, vol. 11, no. 6, p. 860, 2022.

[11] D. E. Root *et al.*, "Device modeling with NVNAs and X-parameters," in *INMMiC 2010*, 2010, pp. 12–15.

[12] R. M. Biernacki, M. Marcu, and D. E. Root, "Circuit optimization with X-parameter models," in *IEEE IMS 2017*, 2017, pp. 1498–1500.

[13] S. Donati Guerrieri, M. Pirola, and F. Bonani, "Concurrent Efficient Evaluation of Small-Change Parameters and Green's Functions for TCAD Device Noise and Variability Analysis," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1269–1275, 2017.

[14] S. Donati Guerrieri *et al.*, "Efficient Sensitivity and Variability Analysis of Nonlinear Microwave Stages Through Concurrent TCAD and EM Modeling," *IEEE J. Multiscale and Multiphys. Comput. Techn.*, vol. 4, pp. 356–363, 2019.

[15] S. Donati Guerrieri, E. Catoggio, and F. Bonani, "Analysis of Doherty Power Amplifier Matching Assisted by Physics-Based Device Modelling," *El.*, vol. 12, no. 9, 2023.

[16] E. Catoggio *et al.*, "Thermal modeling of RF FinFET PAs through temperature-dependent X-parameters extracted from physics-based simulations," in *INMMiC 2022*, 2022, pp. 1–3.