A Stacked Doherty Power Amplifier For Ka-Band Space Applications

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***Abstract*—This paper presents the design and preliminary experimental characterization of a Monolithic Microwave Integrated Circuit (MMIC) Doherty Power Amplifier (DPA) conceived for satellite downlink Ka-band (17.3–20.3 GHz), manufactured in Gallium Nitride on Silicon (GaN-Si) High Electron Mobility Transistor technology with 0.1 µm gate length available at OMMIC foundry. The DPA is based on a three-stage architecture in which the devices in the output stage of both Carrier and Peaking branches are implemented in a stacked configuration. The MMIC shows preliminary experimental results in agreement with the simulations achieving a small signal gain larger than 25 dB and input and output return losses better than 10 dB. Expected nonlinear performances show a saturation output power of 38 dBm, a gain better than 22 dB, and a Power-Added Efficiency of 37%, which remains higher than 25% at 6 dB of output power back-off.**

I. Introduction

Space communication systems are rapidly evolving toward higher carrier frequencies, multi-beam active antenna arrays, and signals based on complex modulation schemes [1]. If, from one side, these innovations allow to achieve higher data rates and flexible and better area coverage, on the other side they put more stringent requirements on the RF components of the payload and, above all, on the adopted power amplifier (PA), which has to be more linear and efficient as compared to the past. In fact, the adoption of spectrally efficient modulated signals, which are characterized by high Peak-to-Average Power Ratio (PAPR), asks for a PA with high efficiency not only at saturation but also in back-off. Efficiency is of paramount importance in space since power budget, thermal and mechanical design, as well as the weight of the overall payload is heavily affected by it. Additionally, the PA should also guarantee an acceptable linearity along its dynamic to reduce at minimum the need for additional linearizing blocks, thus leading to a system with low complexity, which is really important to assure good reliability.

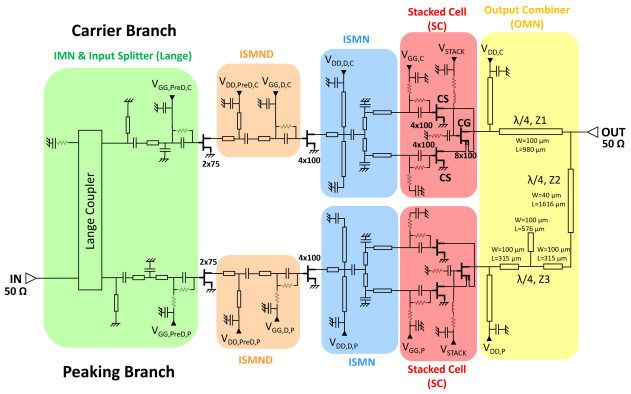
Therefore, high-efficiency PA architectures, such as the Doherty Power Amplifier (DPA), which is nowadays the most adopted solution in the ground communication systems, at least in the sub-6 GHz range, are also starting to be investigated for high frequency space applications [2]–[9].

From a technological point of view, considering that the typical output power requirement at chip level is in the order of 6 W to 10 W minimum, in downlink Ka-band (i.e., 17.3-20.3 GHz), the most suitable Monolithic Microwave Integrated Circuit (MMIC) technology to be used seem to be the Gallium Nitride (GaN) one, either on silicon carbide (SiC) or on pure silicon (Si) substrate [1]. In fact, such power levels are typically beyond the possibility of other semiconductor technologies usually adopted for space systems.

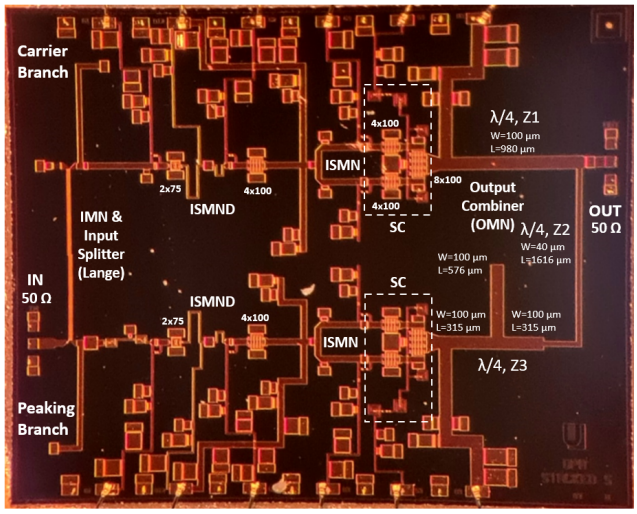
This paper focuses on this quite novel research trend, presenting the design and the preliminary experimental characterization of a Ka-band DPA MMIC in which the active devices of the final stage are in a stacked cell (SC) configuration. The latter consists of one or more devices in a pseudo-common-gate (CG) configuration stacked on top of a common-source (CS) one, which theoretically allows to achieve better performance with respect to the more traditional parallel configuration. Indeed, the SC has the advantage of having an optimum output impedance higher than that of the single active device, resulting in a lower impedance transformation ratio required to match the 50 Ω termination, thus leading to benefits in terms of broadband behavior and lower losses [10], [11]. The reported DPA is implemented in the D01GH GaN-Si process with a gate length of 0.1 µm from OMMIC. It achieves a peak power of 38 dBm, a Power-Added Efficiency (PAE) of more than 37 %, and an associated gain of approximately 22 dB in the downlink Ka-band.

II. DPA Design

The design goals of the DPA are to achieve a saturated output power of 6 W and a high efficiency at both saturation and 6 dB output power back-off (OBO) in the 17.3 – 20.3 GHz band. In this DPA, the SC was used in the final stage of both Carrier and Peaking branches. A load pull analysis was carried out to select the devices to be used for CS and CG, considering that the chosen technology provides a power density of approximately 2 W/mm. To achieve the output power requirements, a gate periphery of the final stage of about 3 mm must be chosen. Therefore, as a first step in the design flow, the SC was assembled according to the compact, symmetrical, and high-performing topology presented in [5], where the CS is divided into two devices with 4x100 µm gate periphery each, and the CG is implemented by using a single 8x100 µm device. Electromagnetic simulations are essential at this stage, to correctly evaluate the coupling and crosstalk effects present among the components of the SC [12] and thus optimize its performance.



(a) Schematic



(b) Photo

Fig. 1. DPA Schematic (a) with the different sub-networks highlighted: the SC is realized by two 4x100 µm CS devices and single 8x100 µm CG. There are two cascaded CS driver stages, 4x100 µm and 2x75 µm, respectively. The OMN consists of two short-circuited stubs in parallel to the drain of the SCs and three $\lambda/4-f_0$ transmission lines with different characteristic impedances (Z1, Z2, Z3). Between the final-driver and driver-pre-driver stages are the ISMN and ISMND matching networks, respectively. Finally, at the input there are the IMNs and the input splitter realized by a Lange uneven coupler. Photo (b) of the realized Stacked DPA: chip size 5x4 mm^2.

In Fig.1 are reported the schematic (a) and photo (b) of the realized chip of the DPA (chip size 5x4 mm^2). As can be noted, together with the SCs in the final stage, two cascaded CS driver stages, with a gate periphery of 4x100 µm and 2x75 µm, respectively, were added in both branches with the aim of increasing the gain of the entire amplifier. The drain bias voltage is set to 18 V for the SCs and 9 V for the single-ended devices in the driver and pre-driver stages. Such values result to be a good trade-off between performance and reliability since they allow to limit the junction temperature of the devices to 160 °C in the worst case, i.e., when the backside temperature of the MMIC is assumed to be $T_{BS}=75$ °C. The thermal behaviour of power devices for space applications, especially if GaN-Si technology is employed, is fundamental for its impact on the lifetime of satellite MMICs [13]. The bias classes of the devices are summarized in Table I.

TABLE I
DPA BIAS CONDITIONS.

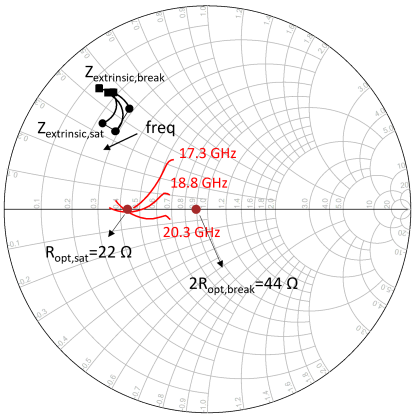
Stage	Parameter	Value	Unit	Class
	Carrier Branch			
Pre-Driver	$V_{GG,PreD,C}$	-1.4	V	AB
	$V_{DD,PreD,C}$	9	V	
	$I_{D,PreD,C}$	3.7	mA	
Driver	$V_{GG,D,C}$	-1.44	V	AB
	$V_{DD,D,C}$	9	V	
	$I_{D,D,C}$	5.4	mA	
SC	$V_{GG,C}$	-1.32	V	AB
	V_{STACK}	7.6	V	
	$V_{DD,C}$	18	V	
	$I_{D,C}$	45.7	mA	
	Peaking Branch			
Pre-Driver	$V_{GG,PreD,P}$	-1.4	V	AB
	$V_{DD,PreD,P}$	9	V	
	$I_{D,PreD,P}$	3.7	mA	
Driver	$V_{GG,D,P}$	-2	V	C
	$V_{DD,D,P}$	9	V	
	$I_{D,D,P}$	-	mA	
SC	$V_{GG,P}$	-2.6	V	C
	V_{STACK}	7.6	V	
	$V_{DD,P}$	18	V	
	$I_{D,P}$	7.7	mA	

The unconditional stability of the SC under small signal conditions was ensured through an R-C series network connected to the gate of the CG device an a stabilization network connected to the gate of the CS, consisting of a parallel R-C and series R-L. The latter network topology was also used to stabilize the devices in the driver and pre-driver stages.

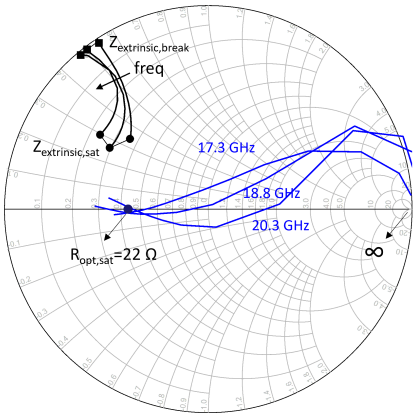
Referring to Fig.1, the synthesized output combiner (OMN) includes two short-circuited stubs connected in parallel to the drain of the SCs, and three $\lambda/4-f_0$ transmission lines with different characteristic impedances (Z1, Z2, and Z3), whose values have been selected according to [14]. The length of the parallel stubs was properly selected to resonate out the output parasitic of the SC, whereas through a careful selection of the characteristic impedances Z1, Z2 and Z3, it was possible to achieve a broadband matching to 50 Ω without adding any further post-matching components. The designed OMN ensures the correct modulation of the load seen by the SCs in the final stage, i.e., from $2R_{opt}=44\,\Omega$ to $R_{opt}=22\,\Omega$ for the Carrier and from ∞ to $R_{opt}=22\,\Omega$ for the Peaking one, as shown in Fig.2, being R_{opt} the intrinsic optimum load of the device inferred from the Load Pull analysis.

The matching networks between final and driver stages (ISMNs) were synthesised to transform the input loads of the two CS of the SCs into the optimal output load of the stabilized driver devices. A similar approach was applied to design the matching networks between the driver and pre-driver stages (ISMNDs).

Finally, the 50 Ω pre-driver input matching networks (IMNs) and the input splitter were implemented. The latter consists of a uneven Lange coupler that provides more power to the Peaking branch with respect to the Carrier one ($P_{IN,P}/P_{IN,C}=1.6$) and simultaneously compensates for the phase shift introduced by the output combiner.



(a) Carrier



(b) Peaking

Fig. 2. Synthesised load modulation by output combiner (OMN) of Carrier (a) and Peaking SCs (b) at 17.3, 18.8 and 20.3 GHz.

The design of the DPA was carried out using Keysight PathWave Advanced Design System (ADS) software.

III. Results

The realized MMIC DPA was measured under small signal excitation at the nominal bias condition reported in Section II. Fig.3 shows the comparison between measured and simulated scattering parameters. Notably, a good agreement is achieved with a measured small signal gain (S_{21}) and input return loss (S_{11}) that are better than 25 dB and 10 dB, respectively, in the band from 17.3 GHz to 20.3 GHz.

The simulated nonlinear performance, as a function of the output power, are shown in Fig.4. The realized MMIC shows the typical DPA behaviour achieving a saturated output power of $P_{out,sat}$=38 dBm (6 W) with a PAE peak around 37 %, which remains higher than 25 % at 6 dB of OBO. The gain is around 22 dB in the Doherty region.

The output power, PAE and gain as functions of the frequency are shown in Fig.5, at both saturation and 6 dB OBO. Notably, these features show an almost flat behaviour all over the bandwidth.

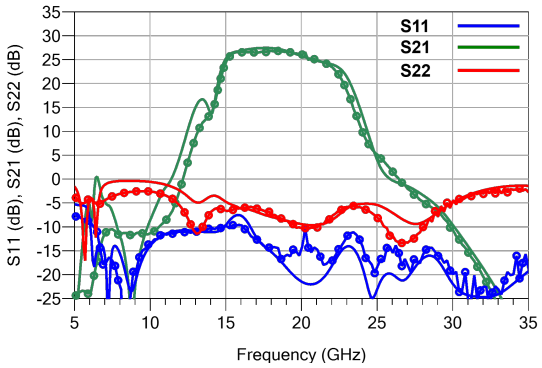


Fig. 3. Comparison between simulated (solid lines) and measured (lines with circles) scattering parameters of the DPA.

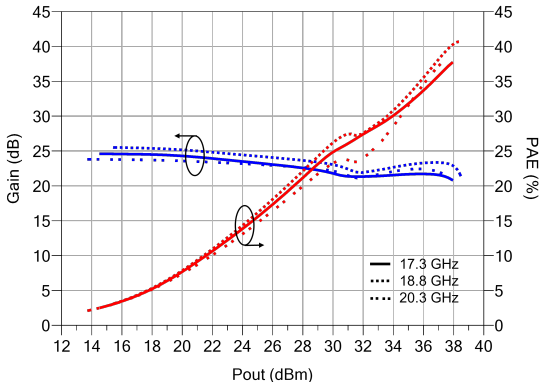


Fig. 4. Simulated DPA performance at 17.3 GHz, 18.8 GHz and 20.3 GHz as a function of the output power.

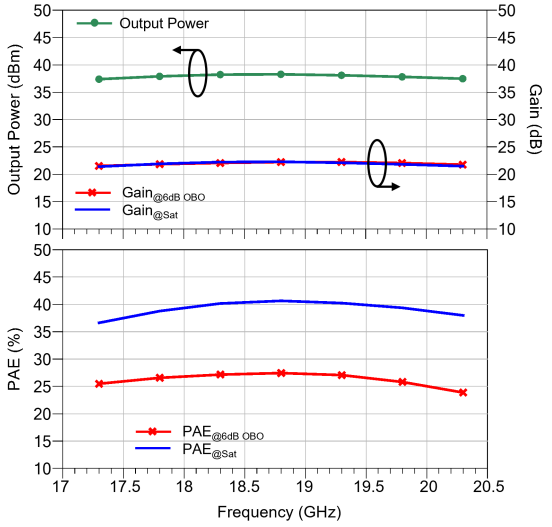


Fig. 5. Output power, PAE and gain at saturation and 6 dB OBO as a function of the frequency.

IV. Conclusion

This work presents the design and preliminary results of a DPA for Ka-Band space applications, in which the output stage devices of the Carrier and Peaking branches are implemented in a stacked configuration. The MMIC is realized in the GaN-Si High Electron Mobility Transistor (HEMT) technology with 0.1 µm gate length available at OMMIC foundry. The measured performance are in good agreement with the expected one, at least in terms of small-signal, whereas nonlinear characterization is still on going. The small-signal gain and input return loss are greater than 25 dB and 10 dB, respectively, while nonlinear simulations show a peak power of 38 dBm (6 W), with a PAE of 37 % and a gain around 22 dB.

Acknowledgment

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