dV/dt Immunity of Half Bridges Based on 650V Enhancement Mode GaN HEMTs

# dV/dt Immunity of Half Bridges Based on 650V Enhancement Mode GaN HEMTs

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***Index Terms*—Enhancement mode GaN HEMTs, switching noise, immunity, electromagnetic interference, e-mode GaN gate driver.**

***Abstract*—E-mode GaN HEMTs in half bridges can be turned on by spurious voltage spikes resulting from output voltage switching or even damaged by undervoltages (overvoltages) caused by the gate driver output switching. This work proposes a solution to address such problems without lowering the gate loop stray inductance.**

## I. Introduction

Last generation high voltage enhancement mode (e-mode) GaN HEMTs allow getting faster switching speed and reduced power losses that enable power converters to work at higher frequency, with enhanced control bandwidth and higher power density [1]. However, the potential of such power devices cannot be exploited at the best due to the fast switching of gate drivers and power transistors causing unwanted overvoltages, undervoltages and oscillations, which affect gate-source voltages and output voltages [2] [3]. Indeed, in half bridges (HBs) like that shown in Fig. 1, the stray inductance of each gate loop ($L_{\mathrm{G-H}}$, $L_{\mathrm{G-L}}$), which comprises of the gate drive output stage, the wiring connecting the gate driver to the power transistor gate and source terminals and the power transistor input capacitance $C_{\mathrm{ISS}}$ resonate at each commutation of the gate driver. Similarly, the fast turn on (turn off) of the HB power transistors drives the power loop stray inductance $L_{\mathrm{D}}$, i.e., the inductance of loop composed by $T_1$, $T_2$ and the DC link decoupling capacitors ($C_{\mathrm{D}}$ in Fig. 1) to resonate with the parasitic output capacitance of the transistor, which is switched off. For instance, at the turn on of the high side ($T_1$ in Fig. 1) $C_{\mathrm{OSS-2}}$ is

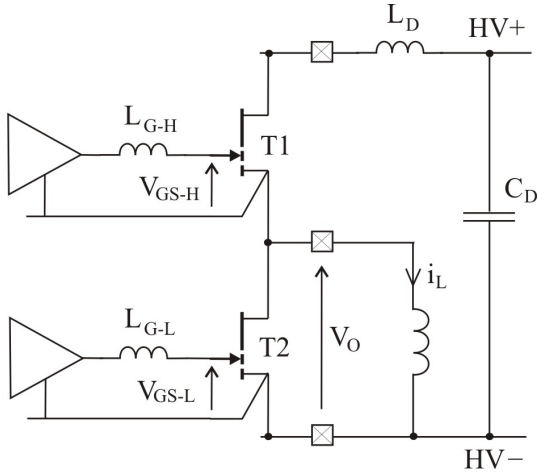


Fig. 1. Half bridge based on e-mode GaN transistors driving an inductive load.

charged quickly by the current flowing in the power loop causing overvoltages and oscillations superimposed onto the nominal output voltage. Regardless of the considered loop, overvoltages and undervoltages can be high enough to exceed the maximum values bearable by the power transistor causing permanent damages or lowering their life time. About the oscillations caused by the fast turn on (turn off), they limit the dead time and the maximum switching speed of the circuit.

Furthermore, the fast switching of the output voltage (it can exceed $100\ V/ns$) causes spurious voltage spikes between the gate and source terminals of the switched off transistor ($T_2$ in the previous example). This is due to the charge injected into the gate terminal through the gate-drain stray capacitance of the power device. The magnitude of such voltage spikes can exceed the transistor threshold turning it on, thus inducing uncontrolled

shoot through currents in the HB [4] [5] [6].
Common approaches to address the above mentioned issues require to reduce the gate driver strength (off chip resistors are included in series to the output of the gate driver), and to lower the gate loop inductance by reducing the distance between the gate driver and the power transistor. Aiming to that, the package size of the power devices as well as that of the gate driver have been reduced over time and in some cases the gate driver has been encapsulated in the power device package or even embedded in the power transistor die. However, this solution exposes the gate driver to continuous thermal cycles affecting its operation and reliability [7].
This paper investigates the cases in which the power transistors and the gate drivers are separated, i.e., mounted on different printed circuit boards, and connected one to the other through common pin headers ($2.54mm$ pitch). The limitations due to such interconnects are discussed and a solutions to make them suitable to driving e-mode GaN HEMTs is proposed.
The paper is organized as follows. Section II analyzes the commutation of an e-mode GaN leg focusing on the dead time. The origin of overvoltages, undervoltages, oscillations and spurious spikes is discussed in Section III, and a solution to mitigate such unwanted effects is proposed in Section IV. The test results highlighting its effectiveness are presented in Section V and some concluding remarks are drawn in Section VI.

## II. Half-bridge hard switching

Nowadays, most of high voltage power switching circuits like those used in DC-DC converters and in power inverters are based on switching legs like that shown in Fig. 1. Besides the power transistors, it comprises of two isolated gate drivers like those shown in Fig. 2, which in turn include an input IC or low voltage chip (IN) and an output IC, known as high voltage chip (OUT). A microcontroller (not shown in Fig. 2) provides the input ICs with the commands to switch the related power transistors on and off. The information (cmd-x) is transferred to the HV chip over a galvanic isolation, which can be a transformer based circuit as shown in Fig. 2. The output IC drives the gate driver output transistors $M_{\mathrm{p}}$, $M_{\mathrm{n}}$ in a coherent fashion to switch the related power transistor on and off. Furthermore, the power supply needed for the operation of each gate driver is provided by isolated DC-DC converters followed by linear voltage regulators (LDO) that allows a fine tuning of the power supply voltages. Such auxiliary circuits are not shown in Fig. 2 for brevity.
The nominal operation of a switching leg can be pre-

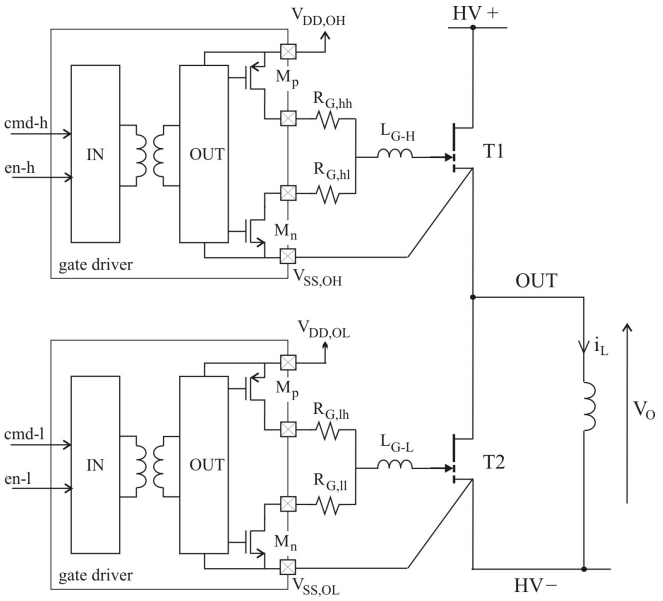


Fig. 2. e-GaN HB comprising the schematic view of the gate driver.

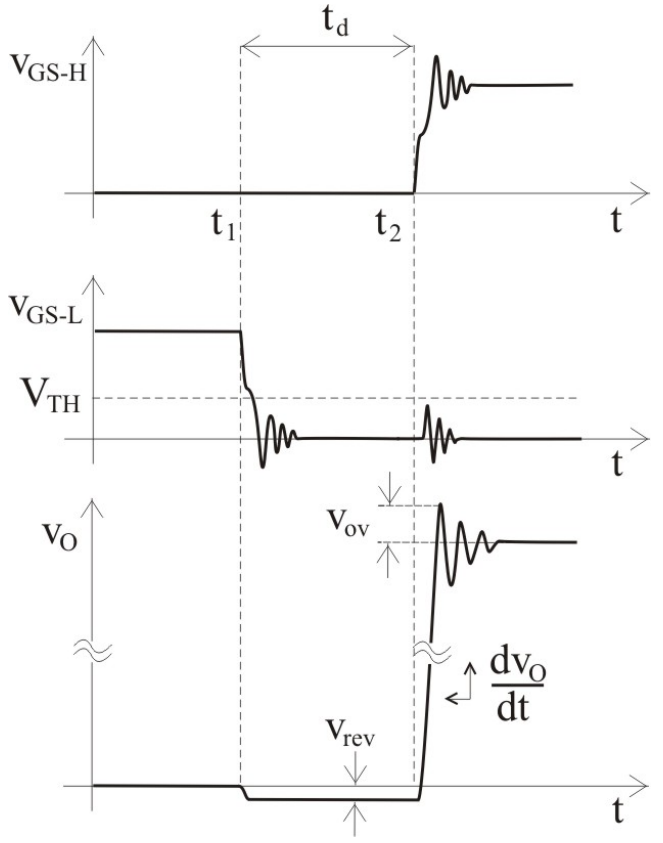


Fig. 3. HB output voltage close to the rising edge and the related HS and LS gate-source voltages versus time.

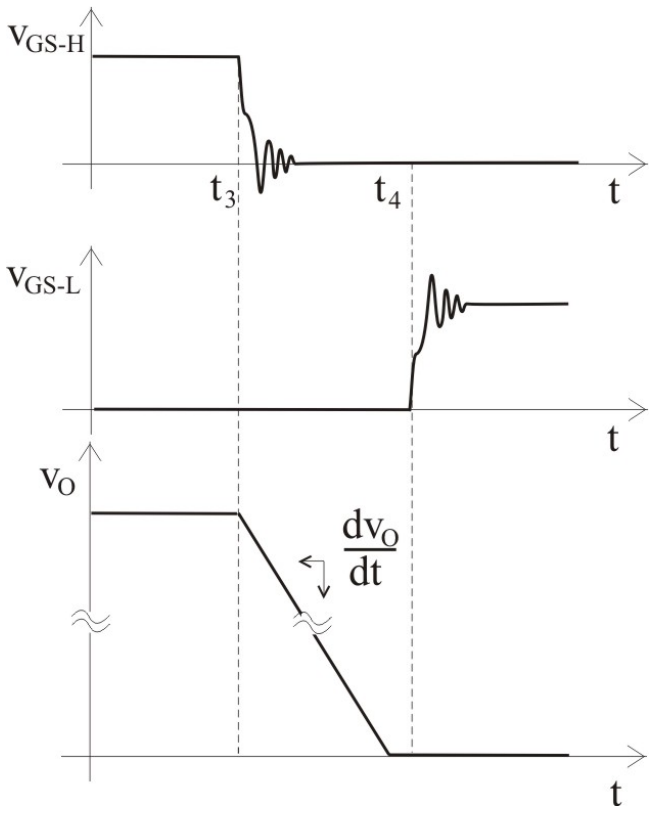


Fig. 4. HB output voltage close to the falling edge versus time and related HS and LS gate-source voltages.

sented referring to the waveforms shown in Figs. 3 and 4. The former refers to the turn on of the high side ($T_1$) while the low side is in free wheeling, the latter, to the turn off of the same transistor with no zero load current. With reference to Fig. 3 and Fig. 1, $T_1$ and $T_2$ are initially off and on, respectively. Wanting to drive the power load, $T_2$ is switched off at $t_1$, but being the load current not null, $T_2$ is driven by the load current in reverse conduction mode as long as the high side ($T_1$) remains switched off. At the end of the dead time ($t_{\rm d}$), i.e., at $t_2$, the turn on of $T_1$ brings the output voltage to the DC link voltage level. The slope of such commutation depends on the power transistor switching speed and on the parasitic capacitance loading the output node, i.e., the transistor output capacitances ($C_{\rm OSS}$) and the load stray capacitance.

The commutation of the output voltage from high to low starts at $t_3$ (see the waveforms in Fig.4) when the high side ($T_1$) is turned off. In this case, the commutation of the output voltage results from the charging (discharging) of the capacitances loading the output node, which is carried out by the load current. Therefore, the slope of the output voltage does not deal with the switching speed of the power transistor, but it depends on the magnitude of the load current.

## III. Origin of oscillations and spikes

As wrote in the introduction, the gate source voltages of the two power transistors are usually affected by overvoltages (undervoltages) at each switching. For instance, in Fig. 3 the undervoltage experienced by $T_2$ at $t_1$ is due to the resonance of its input capacitance with the parasitic inductance ($L_{\rm G-L}$) of the wiring connecting the gate driver output terminals to the power transistor input. Such an undervoltage must not exceed the minimum value declared by the transistor manufacturer. To avoid this, designers are used to including a damping resistor in the gate loop. For the considered case, the damping resistor is $R_{\rm G-ll}$. Similarly, the undershoot affecting $v_{\rm GS-H}$ at $t_3$ (see Fig. 4) can be reduced by adding $R_{\rm G-hl}$, and the overshoots at $t_2$ and $t_4$ by means of $R_{\rm G-hh}$ and $R_{\rm G-lh}$, respectively. Furthermore, it should be noted that the output voltage $V_{\rm o}$ is also affected by overvoltages and oscillations close to $t_2$ as shown in Fig. 3. They are due to the resonance of the power loop parasitic inductance ($L_{\rm D}$ in Fig. 1) and the parasitic capacitance loading the output node, which is dominated in this case by $C_{\rm OSS-2}$, the $T_2$ output capacitance.

Depending on the power loop damping resistance, i.e., the DC link capacitors equivalent ESR and the on resistance of the turned on power transistor, the overshoots can exceed the DC link voltage by $40-50\%$. Such overvoltages reduces the lifetime of the power transistors and the oscillations that follow contribute to enrich the electromagnetic emission delivered by the power circuit. Given that, both the overvoltages and the oscillations deal with the slope of the output voltage at $t_2$, and being this related with the current injected into the gate terminal of $T_1$, both issues can be addressed by selecting a proper value for $R_{\rm G-hh}$.

Furthermore, with reference to Fig. 3, it should be mentioned that the fast transition of the output voltage causes a voltage spike affecting the gate source voltage of $T_2$ ($v_{\rm GS-L}$), which is driven to stay off. This is due to the voltage divider composed of the low side gate drain parasitic capacitance ($C_{\rm GD}$) and the gate-source parasitic capacitance ($C_{\rm GS}$), which is in parallel to the gate driver output impedance including the interconnect stray inductance. A reduced view of the low side transistor driven to be switched off is shown in Fig. 5. The circuit includes the gate loop parasitic elements, i.e., the gate loop inductance $L_{\rm G-L}$, the power transistor parasitic capacitances, the gate driver internal resistance $R_{\rm on}$ ($M_{\rm n}$ on resistance) and the off-chip resistor $R_{\rm G-ll}$.

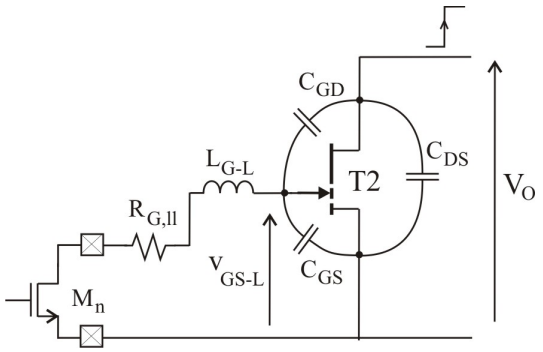


Fig. 5. A reduced view of the HB with the LS transistor switched off. The parasitic capacitances and inductances are pointed out to highlight how the output voltage switch is propogated to the gate-source voltage.

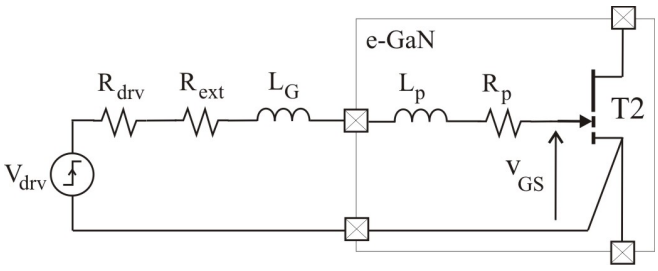


Fig. 6. Equivalent circuit of the gate loop comprising the gate driver Thevenin equivalent circuit ($v_{\rm drv}$,$R_{\rm drv}$).

If the gate-driver output impedance comprised of the output resistance ($R_{\rm on}$) only, the voltage spike affecting $v_{\rm GS-L}$ would have been greatly attenuated. In practice, the presence of the off-chip resistance $R_{\rm G-ll}$ and that of the parasitic inductance $L_{\rm G-L}$ increases the impedance at higher frequency resulting in higher voltage spikes. Since the parasitic inductance of the gate loop can be controlled hardly, and wanting such a voltage spike not to exceed the transistor threshold $V_{\rm TH}$, a negative voltage level is used to increase the noise margin. This avoids the unwanted turning on of $T_2$ when $T_1$ is already on, which would result in uncontrolled shoot through currents. Complementary, also the gate-source voltage of $T_1$ ($v_{\rm GS-H}$), which is driven to be off, can be affected by the voltage spikes resulting from the negative slope transition of the output voltage. However, it should be noted that $v_{\rm GS-L}$ is more likely affected by such voltage spikes because the positive slope transition of the output voltage is much greater than the negative one. Indeed, the first is due to the switching of $T_1$, the second is triggered by the turn off of the high side, as shown in Fig. 4, and it depends on the load current magnitude. The slope of the negative transition can be expressed as

$$\frac{dv_{\rm o}}{dt} \simeq \frac{I_{\rm L}}{(C_{\rm OSS-1} + C_{\rm OSS-2} + C_{\rm p})}, \qquad (1)$$

where $I_{\rm L}$ is the load current, $C_{\rm OSS-1}$ and $C_{\rm OSS-2}$ are the output capacitances of $T_1$ and $T_2$ and $C_{\rm p}$ is the load stray capacitance.

Based on that, the worst case in terms of spike magnitude occurs when the HB is not loaded, therefore this specific case is considered in what follows.

## IV. Gate Loop Oscillation Damping

As discussed in the previous section, the gate source voltages can be affected by overvoltages, undervoltages and oscillations at each transition of the gate driver output voltage. These are mostly due to the gate loop inductance, i.e., $L_{\rm G} + L_{\rm p}$ in Fig. 6, which resonates with the input capacitance of the power transistor $C_{\rm I-SS}$. The oscillations resulting from such resonances are usually damped including a resistor ($R_{\rm ext}$ in Fig. 6) in the gate loop. The transfer function relating the gate source voltage ($v_{\rm gs}$) to the gate driver Thevenin equivalent source ($v_{\rm drv}$) versus frequency, was evaluated for different values of the $R_{\rm ext}$, obtaining the plots shown in Fig. 7. Furthermore, the gate source voltage is also affected by the charge injected into the gate terminal through the gate-drain capacitance at each transition of the output voltage. For instance, $v_{\rm GS-L}$ in Fig. 3 is affected by a voltage spike at $t_2$. The magnitude of such spikes depends on the impedance $Z_{\rm GS}$ loading the gate-source terminals, which in turn depends on the off-chip resistor $R_{\rm ext}$, as it is shown by the plots in Fig. 9. In particular, the higher the value of such a resistor is the higher $|Z_{\rm GS}|$, and the higher is the magnitude of the voltage spike affecting the gate-source voltage. The parameters used to obtain the plots shown in Figs. 7 and 9 are listed in Tab. II.

Based on the above, on one hand, $R_{\rm ext}$ should be selected to damp the oscillations due to the gate driver switching, but it should be also as low as possible to reduce the magnitude of the voltage spike resulting form the switching of the output voltage.

Wanting to address both issues, meaning to damp the oscillations caused by the gate driver switching and to reduce the magnitude of the gate source impedance in the frequency range of interest, this paper proposes to include a passive snubber as close as possible to the gate-source terminals of the power device, as shown in Fig. 10. The snubber capacitor $C_{\rm S}$ increases the attenuation of the voltage divider composed of the gate-drain stray capacitance $C_{\rm GD}$ and the gate source impedance $Z_{\rm GS}$. The resistor $R_{\rm S}$ is selected to damp the resonator composed by $(C_{\rm S} + C_{\rm GS})$ and the gate loop stray inductance

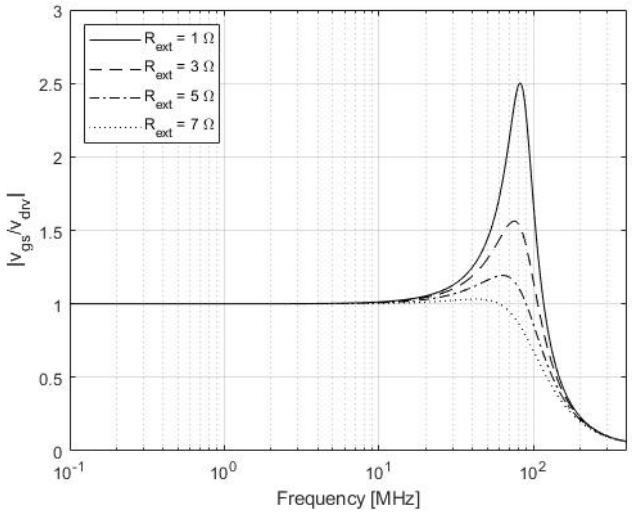


Fig. 7. Magnitude of the gate loop transfer function ($v_{\rm gs}/v_{\rm drv}$) vs. frequency, plotted for different values of the damping resistance.

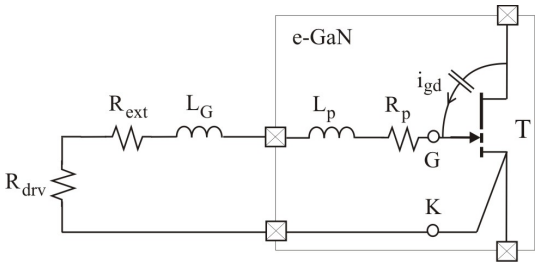


Fig. 8. Equivalent circuit of the gate loop driven by the current $i_{\rm gd}$ due to the commutation of the output voltage. The gate driver is in steady state, therefore it is modeled by the gate driver resistance. $Z_{\rm GS}$ is the impedance between the G and S terminals.

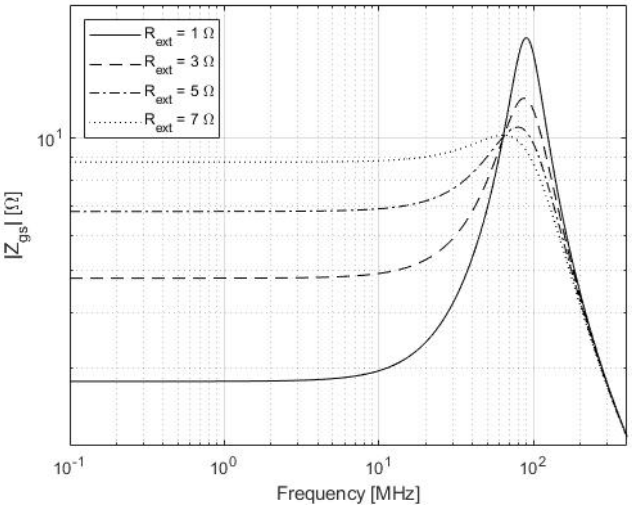


Fig. 9. Magnitude of $Z_{\rm GS}$ versus frequency, evaluated for different values of $R_{\rm ext}$.

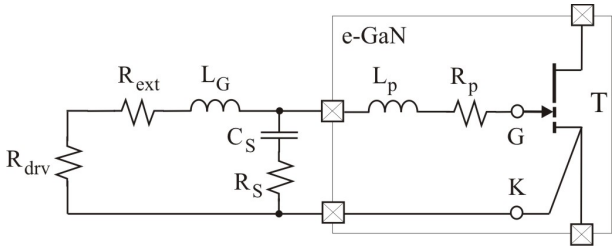


Fig. 10. Equivalent circuit of the gate loop as in Fig.8 comprising the passive snubber $R_{\rm S}$-$C_{\rm S}$.

$L_{\rm G}$. This is correct as long as the impedance shown by the package interconnect ($L_{\rm P}$ and $R_{\rm P}$) plays a minor role.

The next section shows the main features of the prototype developed within this work, the test setup and the measurement results with the aim to highlight the effectiveness of the proposed approach.

## V. Half Bridge Prototype and Experimental Results

A prototype comprising a half bridge based on e-mode GaN transistors, the related gate driver and the DC-link decoupling capacitors was designed and fabricated. The power section is composed of two 650V e-mode GaN HEMTs and the DC link decoupling capacitors. The gate driver board is based on two isolated gate drivers, which output section is supplied by an isolated DC/DC converter followed by a linear voltage regulator. The low voltage section of the gate driver board includes the circuits needed to generate the HS and the LS switching commands from an external PWM signal source. The circuits needed to trim the dead time is also included. The schematic view of the test boards and the cross sectional view of the prototype are shown in Figs. 11 and 12, respectively. The two boards composing the prototype are connected to one another by two couples of headers as highlighted in the prototype cross section shown in Fig. 12. They are needed to provide the power transistors with the respective gate-source voltages. The distance between the headers of each couple is $d_{\rm h} = 2.54\ mm$ and the headers length, meaning the nominal distance between the driver board and the gate driver board is $d_{\rm h} = 10\ mm$. A picture of the prototype is shown in Fig. 13.

Once assembled, the prototype was inserted in the test bench shown in Fig. 14. An arbitrary waveform generator was used to provide the prototype with a PWM signal featuring $f_{\rm sw} = 100\ kHz$ and duty cycle $\delta = 0.2$. The gate source voltage of the LS (HS) transistor was measured using a wideband isolated voltage probe [8]

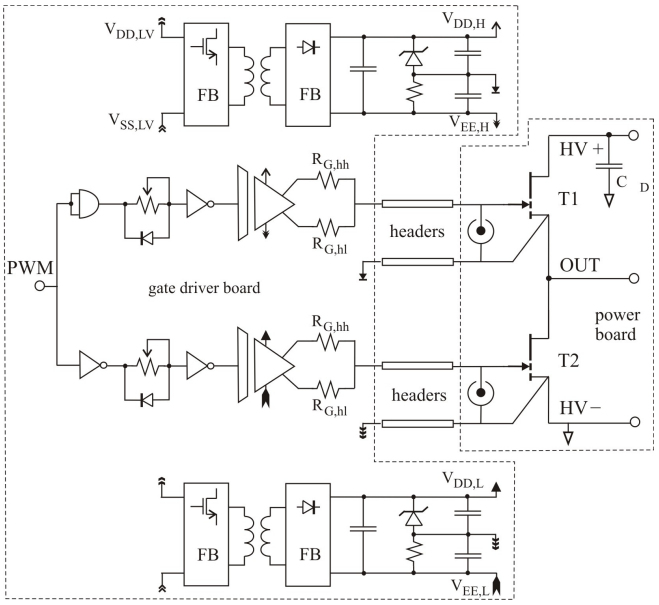


Fig. 11. Prototype schematic view.

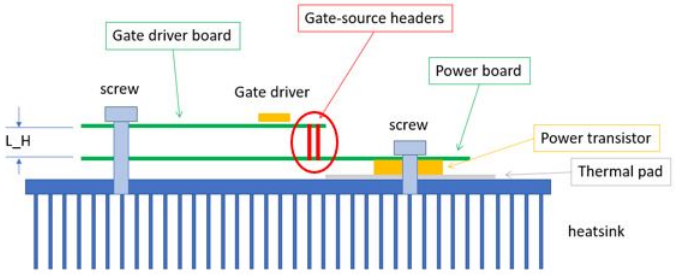


Fig. 12. Cross section of the assembled prototype, which is mounted on the heatsink.

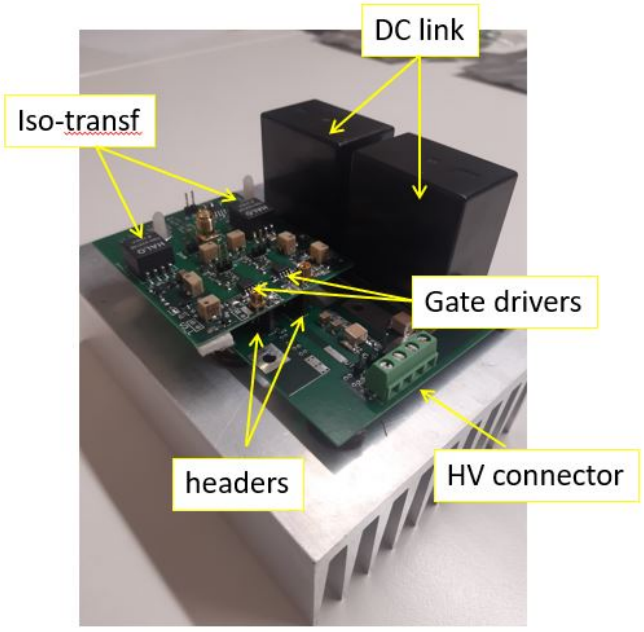


Fig. 13. Picture of the prototype.

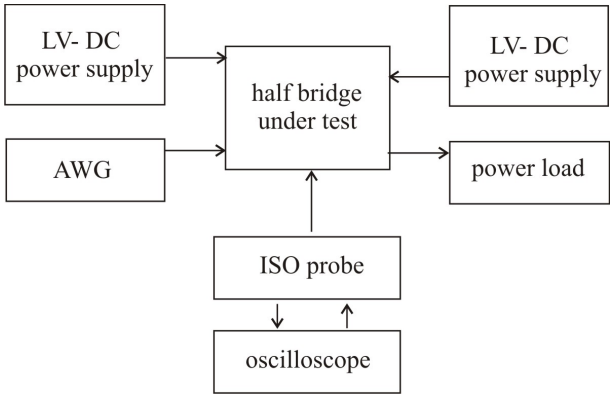


Fig. 14. Test setup.

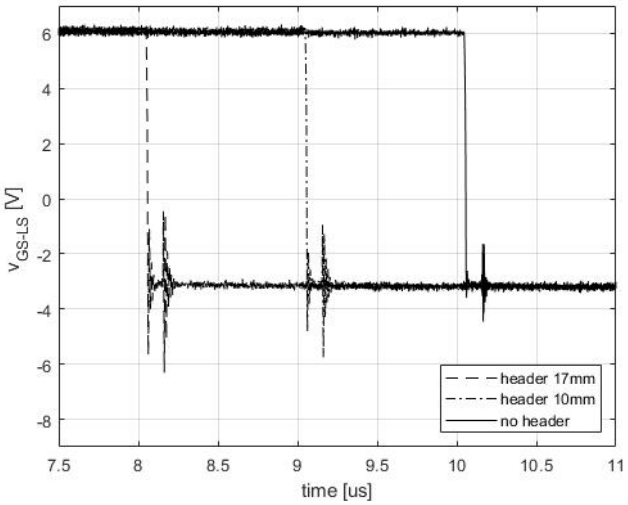


Fig. 15. LS gate source voltage $v_{\mathrm{GS-L}}$ measured at power board MMCX connector. The continuous line refers to $d_{\mathrm{h}} = 0\ mm$, the dash-dotted line to $d_{\mathrm{h}} = 10\ mm$ and the dashed line to $d_{\mathrm{h}} = 17\ mm$. The test boards were the same for the three cases with $R_{\mathrm{G-hh}} = 4.7\Omega$, $R_{\mathrm{G-hl}} = 2.2\Omega$, $R_{\mathrm{G-lh}} = 22\Omega$, $R_{\mathrm{G-ll}} = 0\Omega$

and a digital oscilloscope, as shown in Fig. 14. Furthermore, the low voltage section was supplied by a $5V$ DC power supply, the high voltage section with a $200V$ DC power supply. The voltage probe MMCX male tip was inserted into the female connector of the power board, which is placed on the power board, close to the power transistor gate-source terminals. The impact of the headers' length on the gate source voltages was evaluated for $d_{\mathrm{h}} = 0, 10, 17mm$ measuring the LS gate source voltage. The detail around the transition high-low for the three cases is shown in Fig. 15. The waveforms are shifted to one another to provide the reader with a clear picture of the headers length impact.

Aiming to evaluate the parasitic gate loop inductance

TABLE I
GATE LOOP STRAY INDUCTANCE OBTAINED FROM THE 3D ELECTROMAGNETIC ANALYSIS.

| $d_{\rm h}$ [mm] | $L_{\rm G-x}$ [nH] |
|---|---|
| 0 | 9 |
| 10 | 13 |
| 17 | 16 |

TABLE II
PARAMETERS USED TO OBTAIN THE PLOTS SHOWN IN FIGS. 7 AND 9.

| **Parameter** | **Value** | **Unit** |
|---|---|---|
| $R_{\rm drv}$ | 0.8 | $\Omega$ |
| $L_{\rm pkg}$ | 3.1 | $nH$ |
| $R_{\rm pkg}$ | 1 | $\Omega$ |

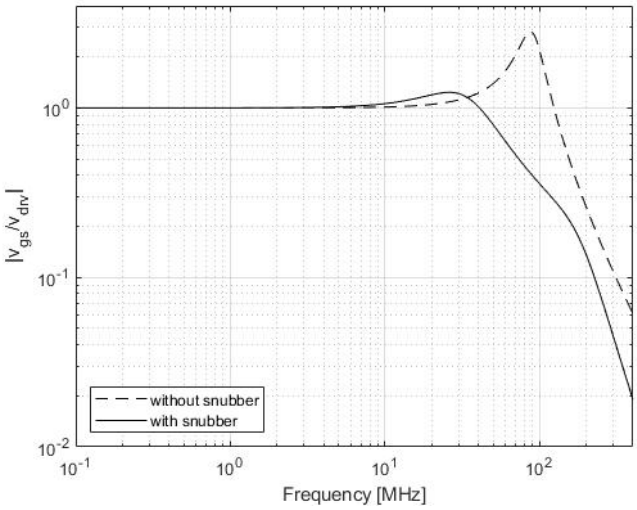


Fig. 16. Magnitude of $v_{\rm gs}/v_{\rm drv}$ versus frequency resulted from the AC analysis of the circuit shown in Fig. 6, with (continuous line) and without (dashed line) snubber and $R_{\rm ext} = 0\ \Omega$.

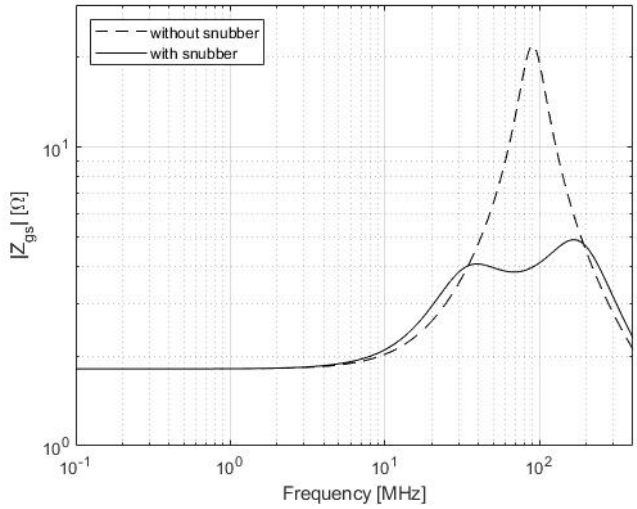


Fig. 17. Magnitude of $Z_{\rm GS}$ versus frequency resulted form the analysis of the circuit in Fig. 8, with (continuous line) and without (dashed line) snubber and $R_{\rm ext} = 0\ \Omega$.

causing the oscillations observed at each commutation, the structure comprising the PCB traces connecting the gate source terminals of the power transistor to the headers at the power board level, the two headers and the PCB traces connecting the headers to the gate driver was analyzed using a 3D electromagnetic field solver. The stray inductances resulted from this analyses are listed in Tab. I. Furthermore, the gate driver is modeled by the on resistance of its low side output transistor, $R_{\rm on-L} = 0.8\ \Omega$, which value was taken from the datasheet of the gate driver.

The parameters listed in Tab. II and the stray inductance $L_{\rm G-L} = 13nH$, which refers to $d_{\rm h} = 10\ mm$, were used to obtain the transfer function $v_{\rm gs}/v_{\rm drv}$ of the equivalent circuit shown in Fig. 6, and the gate loop impedance $Z_{\rm GS}$, meaning that seen from the G-S terminals of the circuit in Figs. 8. The magnitude of these quantities is shown by the dashed line in Figs. 16 and 17. The continuous lines in the same figures were obtained with the passive snubber ($C_{\rm S} = 2nF$ and $R_{\rm S} = 2\Omega$) inserted in the gate loop as show in Fig. 10. $C_{\rm S}$ was chosen much larger than the transistor input capacitance $C_{\rm I-SS}$. This increases the attenuation of the voltage spike induced by the commutation of the output voltage. $R_{\rm S}$ resulted from the parametric analysis of the circuit, as the value that provided the lowest gate source impedance magnitude over the widest frequency range.

The effectiveness of the proposed approach was validated comparing the gate source voltage $v_{\rm GS-L}$ obtained from the measurements carried out with and without snubber, and headers length $d_{\rm h} = 10mm$. The measurement results obtained with (continuous line) and without (dashed line) are shown in Fig. 18. The benefit resulting from the insertion of the snubber is evident. The undervoltage disappeared and the voltage spike induced by the commutation of the output voltage is lowered by more than $80\%$. Similar results were obtained with headers length of $d_{\rm h} = 17mm$.

As a result, the lower level of the spurious voltage spikes obtained with the snubber remove the need of a negative power supply voltage to drive the power

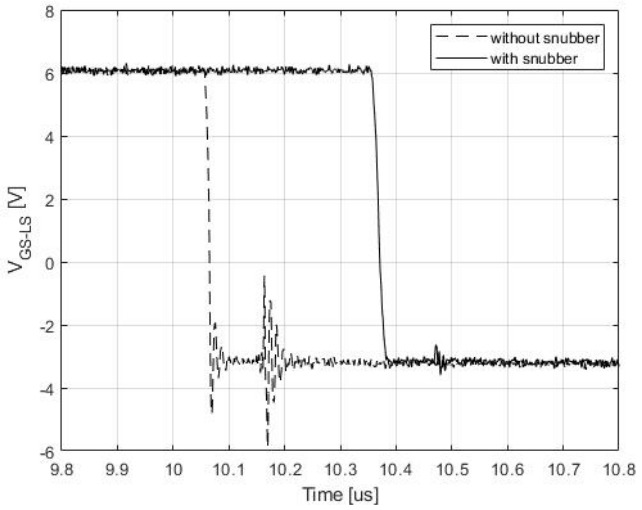


Fig. 18. Gate source voltage of the low side transistor ($v_{\mathrm{GS-L}}$) around the high to low transition. The measurement was repeated with (continuous) and without (dashed) snubber. Furthermore, the external gate driver resistors were $R_{\mathrm{G-hh}} = R_{\mathrm{G-hl}} = R_{\mathrm{G-lh}} = R_{\mathrm{G-ll}} = 0\Omega$ and headers length $d_{\mathrm{h}} = 10mm$.

transistor off, therefore, the switching losses due to the reverse conduction of the power transistors in the dead time are reduced significantly.

## VI. Conclusion

In this work, the immunity of an half bridge based on HV e-mode GaN power transistor to the output voltage switching was discussed focusing on the stray inductances and capacitances of the gate loop. The impact of the gate driver external resistance was discussed getting to the conclusion that the value selected to reduce undervoltages (overvoltages), and to damp the oscillations is not that needed to increase the immunity to spurious spikes. Based on that, the use of a passive snubber placed as close as possible to the gate source pins of the power transistor has been proposed and its effectiveness was checked experimentally. The reduced level of voltage spikes allows one to reduce the magnitude of the gate driver negative power supply, thus reducing the switching losses.

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