A Balanced Stacked GaN MMIC Power Amplifier for 26-GHz 5G applications

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***Abstract* — This work reports the design and experimental characterization of a 4 W Ka-band MMIC power amplifier in GaN/SiC technology, featuring a balanced stacked architecture. The proposed amplifier is composed of a pair of 2-stage amplifier branches, each including a single-transistor driver stage and a 2-stacked-transistor power stage. Small-signal characterization exhibits very good agreement between measurements and simulations, while system-level characterization, employing a 50 MHz instantaneous bandwidth, 10 dB PAPR 5G FR2 signal, demonstrates the very promising linearity performance of the proposed amplifier. The measured minimum ACPR is better than -27 dBc up to an average output power of 24 dBm, from 25 GHz to 27 GHz.**

***Keywords* — GaN, MMIC, power amplifiers, 5G.**

I. Introduction

The need for higher capacity for the next generations of wireless communication standards (5G/6G) requires adapting and partially redefining the architecture of the infrastructure. Traditional frequency bands below 6-GHz (5G FR1) are very crowded but pose fewer challenges from the architecture standpoint, and are therefore very attractive for industry. On the other hand, exploiting mm-wave frequency bands (FR2) would enable the adoption of very dense modulation schemes (up to 1024 Quadrature Amplitude Modulation (QAM)) with wider channel bandwidths (up to 400 MHz) [1].

The power amplifier (PA) plays in this context a key role; it must operate linearly and efficiently at mm-wave frequencies, keeping a high gain over wide bandwidths, handling signals with peak-to-average power ratio (PAPR) increasing from the classical 6 dB to 9-10 dB, and often operating with a variable load due to the presence of phased arrays at its output [2].

From a technology standpoint, Gallium Nitride (GaN) is reaching the competitive stage also at mm-wave frequencies thanks to the availability of short-gate-length ($<$150 nm) Microwave Monolithic Integrated Circuit (MMIC) processes. However, the gain is still an issue of this technology when Ka-band applications are targeted. Furthermore, size and absolute power at MMIC level are fundamental to increase the overall efficiency of the entire transmission system.

For these reasons, we designed, fabricated, and experimentally characterized a balanced stacked Ka-band MMIC power amplifier. Thanks to device stacking we increased the gain of the cell [3], [4] with benefits also in terms of bandwidth thanks to the increased optimum load, closer to 50 Ω. The balanced structure was conceived for a two-fold task: doubling the output power and, at the same time, increasing the load insensitivity of the stage [5]. Finally, the intrinsic linearity of this class-AB amplifier has been optimized by careful selection of the bias levels. The amplifier has promising expected performance in terms of output power (36 dBm) and gain (10 dB) over a 2 GHz bandwidth from 25 GHz to 27 GHz. At the system level, when excited with a 5G 64-QAM signal with 50 MHz bandwidth, the measured Adjacent Channel Power Ratio (ACPR) remains better than -27 dBc over the whole dynamic range, from 25 GHz to 27 GHz with a corresponding average efficiency of the order of 5%.

II. Design and fabrication

The proposed PA is designed adopting the 150 nm GaN HEMT technology of WIN Semiconductors. This GaN process is grown on a 100 μm SiC substrate, and achieves an output power density of about 2.5 W/mm at 20 V bias operation. The cut-off frequency f_T is 35 GHz, while the maximum oscillation frequency $f_{\max}$ is much higher, which makes this process suitable for 5G applications up to 29 GHz.

The PA architecture is shown in Fig. 1: it is a 2-stage balanced PA adopting a 2-transistor stacked cell in the final stage. The layout of the designed cell is shown in Fig. 2: as the main feature, the cell shows a symmetrical layout, achieved by splitting the common-source (CS) stage and the inter-stage matching elements into two parallel circuits. This layout ensures better performance at high frequency with respect to more conventional combinations, as it avoids uneven electromagnetic (EM) coupling effects, which may impair voltage and current distributions inside the cell and thus degrade the stacking efficiency. On the other hand,

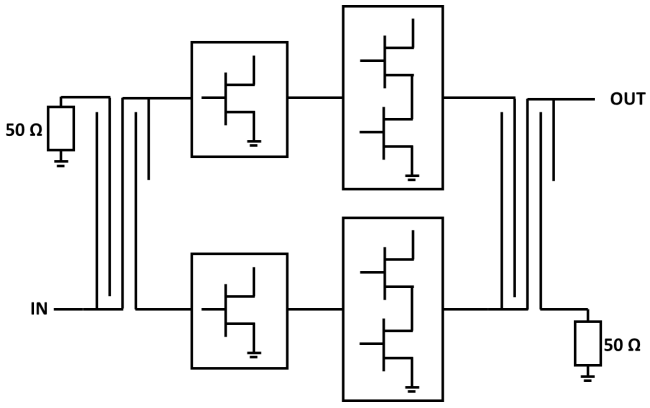

Fig. 1. Block diagram of the proposed balanced stacked PA.

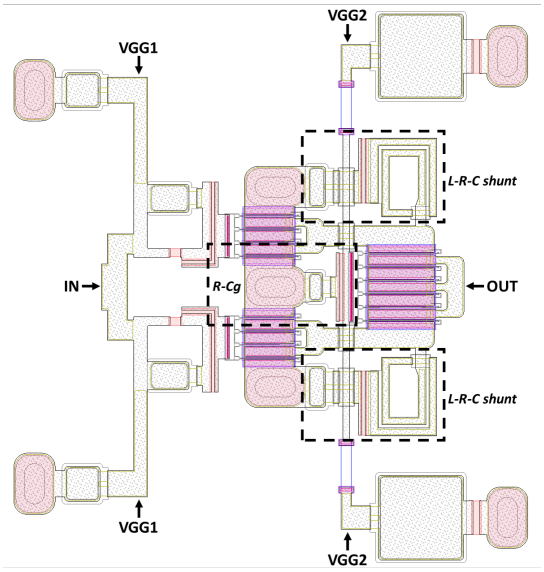

Fig. 2. Layout of the designed stacked cell.

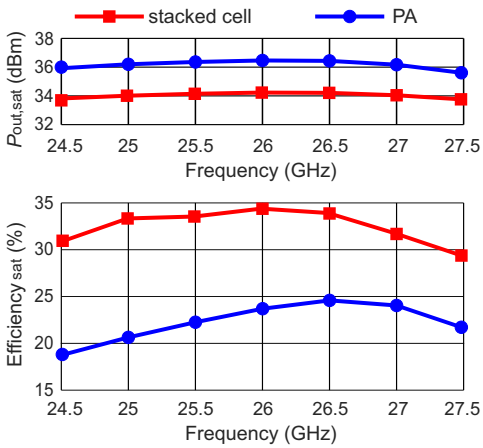

Fig. 3. Expected CW performance of the stacked cell under optimum loading conditions (red, squares) and of the balanced stacked PA (blue, circles) at saturation: output power and efficiency in the 24.5 GHz-27.5 GHz range.

duplication of components increases the required chip area, hence demanding a very dense layout not to compromise cell compactness.

A 6x100 μm transistor is selected as base device: at 26 GHz, at 10% class-AB bias, on its optimum load (9.5+j14.7) Ω, it provides around 32 dBm of output power at 2 dB gain compression, with associated gain and efficiency around 7 dB and 50%, respectively. This device is adopted for the common gate (CG), while the CS is implemented by adopting two 4x75 μm devices in parallel. The use of smaller devices, besides ensuring cell symmetry, can be beneficial in terms of transistor's gain [6]. Each 4x75 μm device is individually stabilized with an R-C pair in series to the gate. Small resistances are added in series to the gate capacitance and to the two L-C shunt pairs adopted for inter-stage matching to further improve small- and large-signal cell's stability. To ensure layout compactness, relatively small AC-shunt capacitors (not shorted at the operating frequency) should be adopted, whose value has been carefully optimized through extensive EM simulations of the whole passive structure [7]. Finally, independent gate bias voltages for the CS and CG stages are supplied, symmetrically from both sides, to allow bias tuning during characterization. A detailed analysis of the cells is reported in [8].

A single-stub output matching network matches the cell on 50 Ω and provides the 40 V drain bias. The saturated output power is nearly 34 dBm, with an associated efficiency of around 30%. A driver stage, made of a single 6x100 μm device matched on the same optimum load of the final stages, and a Π-type input matching network to 50 Ω complete the PA branch. The balanced PA combines with Lange couplers at the input and output two identical single stacked PAs. The balanced configuration assures good input and output matching together with good load insensitivity. The Lange couplers are ideal candidates for power combination at high-frequency thanks to their superior performance in terms of bandwidth, directivity and isolation, as well as losses, symmetry, and area occupation.

Fig. 3 reports the expected large-signal performance of the individual stacked cell and of the complete 2-stage balanced stacked PA under continuous wave (CW) excitation in the 24.5 GHz-27.5 GHz range. The performance of the stacked cell refers to optimum loading conditions, i.e., where its output is terminated on a port with an impedance equal to its optimum load at each frequency. At around 3 dB of gain compression, the stacked cell can provide up to 34 dBm output power with an associated efficiency of 30-35% in the range 25 GHz-27 GHz. In similar gain compression conditions, the overall PA is expected to achieve an output power in excess of 36 dBm (4 W) in the same frequency range, which is consistent with the estimated losses of the output matching network and of the Lange coupler and with a slightly sub-optimal loading condition selected to equalize performance over frequency. As a consequence of the output losses as well as the presence of the driver stages, the efficiency expected from the PA is around 10 points lower than the best performance of the stacked cell, i.e., around 20%-25% in the 25 GHz-27 GHz range.

III. Experimental Characterization

The balanced stacked PA has been characterized both in small-signal and at system-level, adopting a standard 5G FR2 modulated input signal. The photograph of the manufactured chip in the characterization setup is shown in Fig. 4. The nominal bias point is: $V_{\mathrm{DD}} = 20$ V, $V_{\mathrm{GG}} = -2$ V, $I_{\mathrm{D}} = 30$ mA, for the driver stages and $V_{\mathrm{DD}} = 40$ V, $V_{\mathrm{GG_{CS}}} = -2$ V, $V_{\mathrm{GG_{CG}}} = 18$ V, $I_{\mathrm{D}} = 30$ mA for the stacked stages.

The scattering parameters have been measured in the 0.1 GHz-40 GHz range: simulation (solid lines) and measurement (symbols) results are compared in Fig. 5. The agreement is good in the whole frequency range. The small-signal gain is higher than 10 dB from 23 GHz to

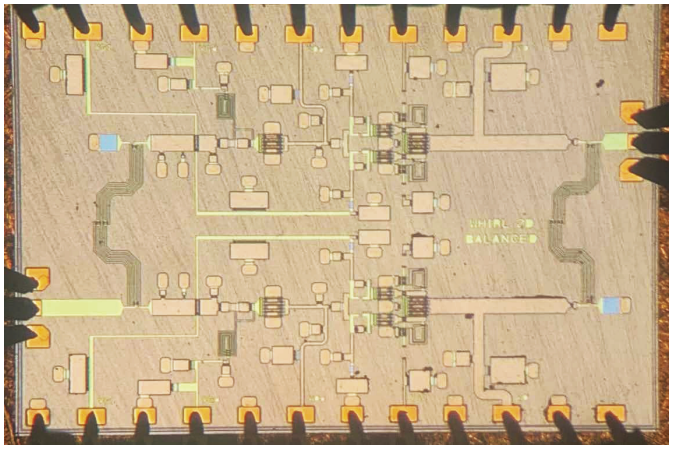

Fig. 4. Photograph of the fabricated balanced stacked MMIC power amplifier (chip size is 3.7 mm×2.4 mm).

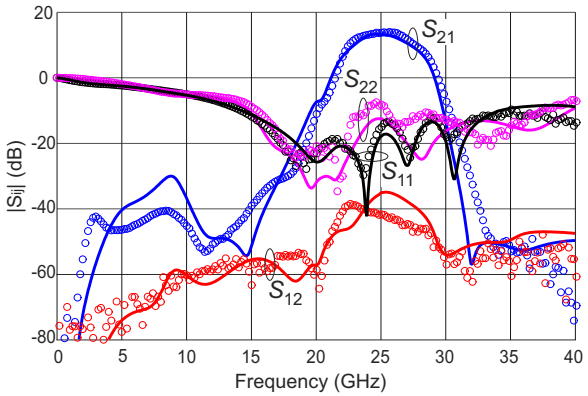

Fig. 5. Simulated (solid) and measured (symbols) scattering parameters of the manufactured balanced stacked PA at the nominal bias in the 0.1 GHz-40 GHz range.

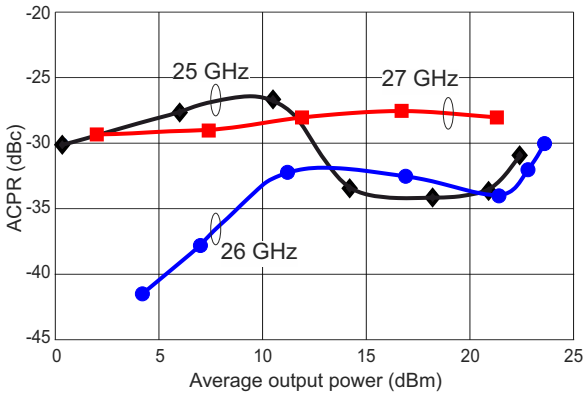

Fig. 6. Measured ACPR versus average output power in the 25-27 GHz band.

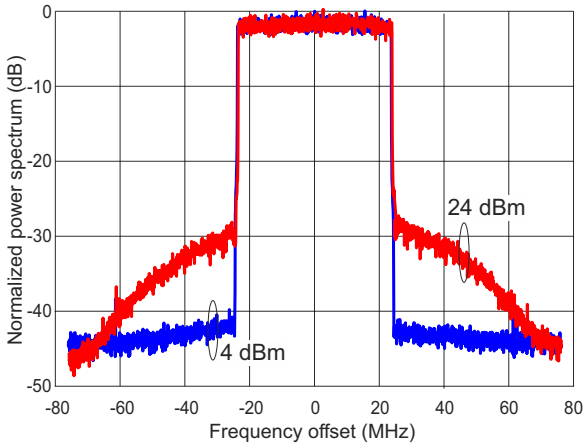

Fig. 7. Normalized measured output power spectrum at 26 GHz at low (4 dBm, blue) and high (24 dBm, red) average output power.

27.5 GHz and around 13 dB in the 25 GHz-26.5 GHz range. The input and output insertion losses are both better than -10 dB from 22 GHz to 30 GHz, also thanks to the presence of the Lange couplers.

The system-level characterization has been carried out with a 5G 64-QAM input signal, featuring 50 MHz instantaneous bandwidth and 10 dB peak-to-average power ratio (PAPR). The carrier frequency was varied from 25 GHz to 27 GHz in 1 GHz step, and a linear pre-amplifier with 35 dB gain and 35 dBm saturated output power was adopted to properly drive the PA. The baseline ACPR related to the test-bench only, has been evaluated using an on-wafer thru and resulted -48 dBc.

Fig. 6 presents the obtained ACPR curves as a function of the average output power up to around 24 dBm, from 25 GHz to 27 GHz. The designed amplifier is almost compliant with the 3GPP 64-QAM 5G NR standard [1] (maximum ACPR lower than -28 dBc) over the whole frequency range, where the ACPR is maintained below -26 dBc. The best linearity performance (ACPR better than -30 dBc) is obtained at the center frequency of 26 GHz, as demonstrated also in Fig. 7, showing the measured output power spectra (normalized) at two different average power levels. The average efficiency achieved under modulated signal excitation is around 3-5%, compatible with the performance at 10 dB back-off of a class-AB PA with a saturated efficiency around 20-25%.

The amplifier performance is compared to literature results in Tab. 1. The proposed balanced stacked PA compares well with the state of the art at the target frequency, and represents a valid solution for 5G applications in the FR2 band.

Table 1. Comparison with state-of-the-art GaAs and GaN MMICs in the 24 GHz-29 GHz range.

Ref ♯	Tech nm	Freq. GHz	Psat dBm	Gain dB	ACPR, dBc @ PAPR, dB
[9]	150 GaAs	28	26	12	-28 @ 7.3
[10]	150 GaAs	28	28.5	23	-30.1 @ 7
[11]	150 GaAs	28	28.7	14.4	-32 @ 10.5
[12]	150 GaN	28	30	6.2	-28.5 @ 9
[13]	150 GaAs	24	30.9	12.5	-30 @ 7.5
[14]	150 GaN	28.5	35.6	12	-27 @ 8
[15]	150 GaN	27.5	36	19	NA
[16]	150 GaN	28.5	39	30	-35 @ 10
This work	**150 GaN**	**26**	**36***	**10**	**-30 @ 10**

* *simulated value*

IV. Conclusion

In this contribution we presented a 4 W Ka-band balanced stacked power amplifier based on a super-symmetrical Stacked power cell in 150-nm GaN/SiC technology. The proposed amplifier has been characterized on-wafer in small-signal conditions, showing a very good agreement between measurements and simulations, and under modulated signal excitation. Adopting a 50 MHz-BW, 10 dB-PAPR 5G signal the obtained ACPR is better than -26 dBc up to 24 dBm of average output power in the full 25 GHz-27 GHz frequency range, a results that is well in line with the state of the art at this frequency and for this application.

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