A 3-Way GaN Doherty Power Amplifier for 28 GHz 5G FR2 Operation

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***Abstract* — This paper presents the design, fabrication, and experimental characterization of a 3-way multi-stage Doherty amplifier working in the 5G NR FR2 bands centered at 28 GHz. The amplifier, realized in the WIN Semiconductors' 150 nm gate-length GaN-SiC integrated technology, is optimized for linearity as well as wide back-off efficient operation. The experimental characterization in continuous wave and under modulated signal excitation evidences performance well in line with the present state of the art in terms of bandwidth, power levels, efficiency, and linearity, without the need for additional pre-distortion.**

***Keywords* — Back-off, Doherty, GaN, High efficiency, MMIC, Power amplifiers, 5G.**

I. Introduction

Wireless communication systems have dramatically progressed over the recent years achieving, nowadays, unpredictable levels of capacity and data rate with very low latency. This is enabled by several factors: the use of millimeter-wave bands, the adoption of phased arrays, and the use of complex modulation schemes with very large Peak-to-Average-Power-Ratio (PAPR) [1]. On the other hand, such disruptive innovations at the network level have posed severe constraints on the transmitter architecture, especially for the power amplifier (PA). PAs operating over multi-gigahertz bandwidth with non-constant envelope signals have been already proposed in the literature, either by introducing new architectures such as the Load Modulated Balance Amplifier (LMBA) [2] and the Distributed Efficient Power Amplifier (DEPA) [3], or by relying upon old-fashioned ones such as the Envelope Tracking (ET) [4] and the Doherty Power Amplifier (DPA) [5].

In general, most of the reported solutions are conceived for sub-6 GHz applications, mostly in hybrid form, and only a few examples are available for higher frequency ranges toward mm-wave bands. Additionally, they are typically designed and optimized for high efficiency when operated at output power back-off (OBO) levels of the order of 6 dB from saturation, whereas next-generation standards (5G/6G) would require efficient handling of signals with increasing PAPR (9 to 12 dB). Therefore, research activities aiming at exploring the feasibility of mm-wave Monolithic Microwave Integrated Circuit (MMIC) PAs capable to meet such stringent requirements are of great interest.

In this paper, we present the design, fabrication, and measurements of a Gallium Nitride (GaN) MMIC 3-way DPA targeting the FR2 5G bands around 28 GHz, optimized for wide OBO, i.e., up to 10 dB. The MMIC is manufactured in the 150 nm GaN-SiC High-Electron-Mobility Transistor (HEMT) process of WIN Semiconductors, and achieves 34 dBm of output power from 27.5 GHz to 29.5 GHz, with PAE in the range of 18-23% and 8-16% at saturation and 10 dB OBO, respectively. The saturated gain is higher than 8 dB in the whole band. Regarding the linearity, the MMIC without predistortion is compliant with the 3GPP standard for FR2 bands with 64-QAM 5G NR signals [6] from 27 GHz to 29 GHz.

II. Design Strategy and Fabrication

The block diagram of the implemented amplifier is shown in Fig.1. The output combiner sums the power of three branches: one three-stage Main biased in class AB and two three-stage Auxiliaries biased in class C.

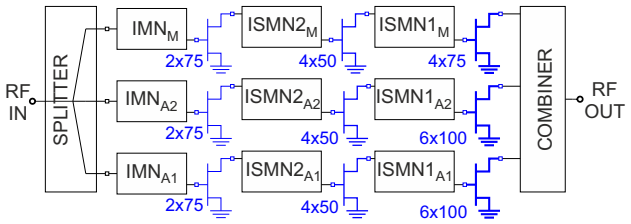

Fig. 1. Block diagram of the implemented 3-way Doherty amplifier.

The operating drain voltage (V_{DD}) is fixed to 20 V, with the selected technology showing a knee voltage of about 4 V and a current density around 400–500 mA/mm. A preliminary load-pull analysis on the available device nonlinear models is conducted to identify the best trade-off between achievable performance and gate periphery in each stage. They are selected targeting an overall saturated output power of about 3 W. The 4x75 µm device results to be the most appropriate one to implement the Main final stage, whereas the 6x100 µm device is used in both Auxiliaries. The number and size of the driver stages are selected trading off linearity and power consumption, considering the gain of the individual transistors (not exceeding 10 dB at the design frequency) and the gain penalty of a DPA for deep back-off efficiency enhancement, resulting in 4x50 µm for all drivers and 2x75 µm for the pre-driver stages. All devices are made unconditionally stable by an $R-C$ parallel network in series to the gate.

On the other hand, specific design choices are made aiming to alleviate the typically higher distortion of the DPAs with respect to similar class AB PAs [7].

The pre-drivers are all biased in class AB, and the driver and power device of each Auxiliary branch are biased in the same class C point thus sharing the same gate bias line. The input and interstage matching networks are implemented in semi-lumped form adopting similar topologies for all branches. The interstage matching networks are designed to provide equally good matching both in back-off and at full power, thus minimizing the effect of input impedance variation due to the modulation of the device output loads. This provides a trade-off among back-off efficiency, gain, and phase distortion.

The output combiner has been synthesized following the scheme proposed in [8] and optimized for 6 dB and 12 dB OBO efficiency peaks. Finally, the uneven 3-way input splitter is synthesized through the cascade of two layers of Lange couplers centered at different frequencies and properly recombined. The latter results be a more robust and reliable solution with respect to a non-isolated alternative thanks to its lower sensitivity to the drivers' input impedance, which may not be accurately predicted by the foundry nonlinear model.

The microscope photograph of the realized MMIC is shown in Fig. 2.

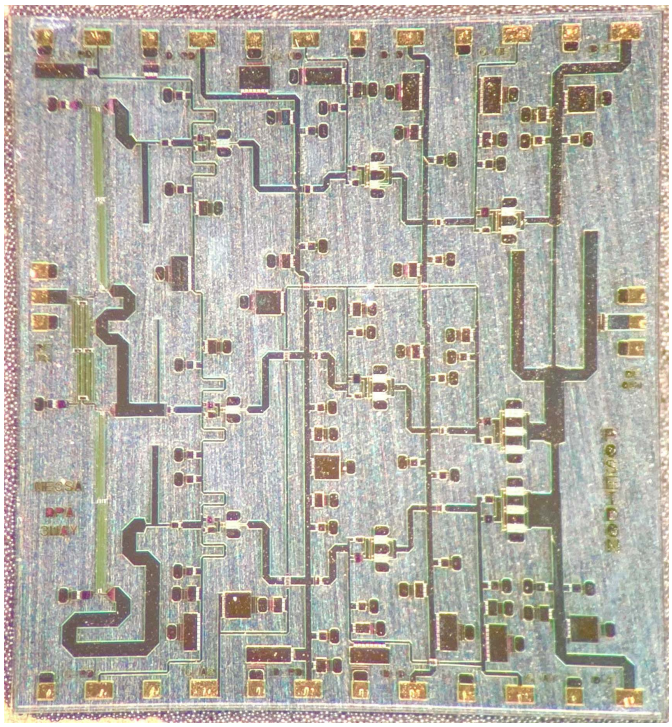

Fig. 2. Microscope photograph of the fabricated 3-way MMIC DPA (size: $3.6 \times 3.9\,\mathrm{mm}^2$).

III. Experimental Characterization

The 3-way DPA is characterized in small signal, large signal and under modulated signal excitation at the nominal bias point: $V_{\mathrm{DD}} = 20\,\mathrm{V}$ for all devices, $V_{\mathrm{Gpd}} = V_{\mathrm{GdM}} = V_{\mathrm{GM}} = -2.0\,\mathrm{V}$, $V_{\mathrm{GdA1}} = V_{\mathrm{GA1}} = -2.2\,\mathrm{V}$, $V_{\mathrm{GdA2}} = V_{\mathrm{GA2}} = -3.4\,\mathrm{V}$, that corresponds to a total quiescent drain current of $I_{\mathrm{D,tot}} = 30\,\mathrm{mA}$.

A. Small signal

The scattering parameters are measured in the range 0.01-55 GHz with a Keysight N5227A Vector Network Analyzer calibrated on-wafer adopting a Load-Reflect-Match (LRM) technique.

Fig. 3 reports the measured (symbols) S_{11}, S_{21}, and S_{22} along with the corresponding simulations (solid lines) performed at the same drain bias current. A good agreement between simulations and measurements is evidenced at all frequencies. The small signal gain is in the range of 15-20 dB from 27 to 30 GHz. The presence of the Lange couplers clearly improves the input return loss, which results higher than 10 dB from 25 to 40 GHz. On the other hand, the output return loss is better than 8 dB from 25 to 30 GHz and than 10 dB over the whole set of FR2 bands.

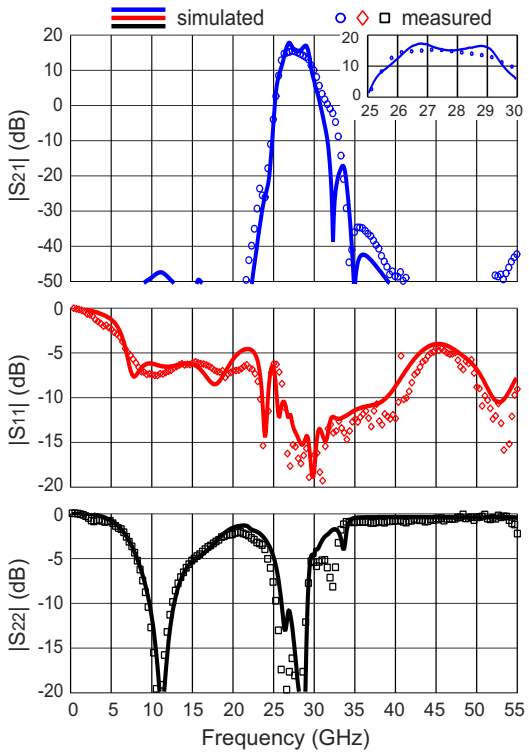

Fig. 3. Comparison between simulated (solid lines) and measured (symbols) scattering parameters of the fabricated 3-way DPA in the range 0.01-55 GHz.

B. Continuous wave

The Continuous Wave (CW) characterization is carried out on a scalar-calibrated test bench adopting two Keysight U8485A power meters for the absolute power measurements. Power sweeps are performed from 27 GHz to 30 GHz in 500 MHz steps. The measured performance as a function of the input power at 27.5 GHz is reported in Fig. 4.

Fig. 5 reports the performance in terms of saturated output power, power gain and PAE, at saturation and at 10 dB OBO, versus frequency. From 27.5 to 29.5 GHz, the saturated output

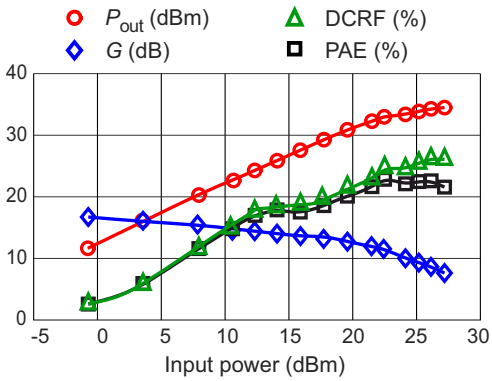

Fig. 4. Measured CW performance of the 3-way DPA at 27.5 GHz: output power (red), power gain (blue), efficiency (green), and PAE (black) versus input power.

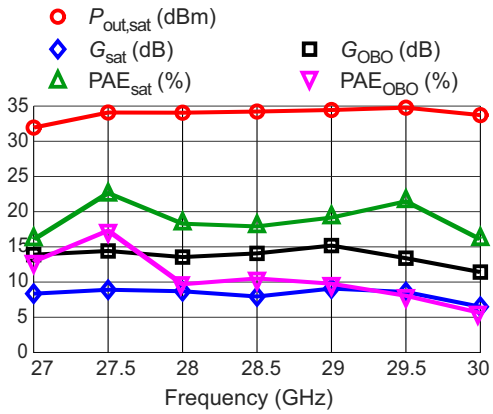

Fig. 5. Measured CW performance of the 3-way DPA versus frequency, from 27 GHz to 30 GHz: output power, power gain, and PAE at saturation and at 10 dB OBO.

power exceeds 34 dBm, with an associated power gain and PAE higher than 8 dB and 18%, respectively. At 10 dB OBO, the PAE is maintained above 8%, with better performance towards the lower end of the band, and the gain is always higher than 13.5 dB.

The CW performance of the designed amplifier is summarized and compared to the present state of the art (SOA) in Table 1. The achieved CW bandwidth and performance are competitive, especially in terms of back-off PAE, also considering the complexity of the architecture required to achieve a sufficient gain. In particular, [9] is the only work where comparable back-off PAE is maintained over a similar bandwidth while achieving high gain, but the power levels achievable by the adopted GaAs technology are significantly lower.

C. Modulated signal measurements

The 3-way DPA has been tested at the system level adopting a test bench composed of a Keysight E8267D PSG for signal generation and up-conversion and a Keysight N9021B MXA as a receiver. The signal excitation is a standard 5G 64-QAM NR downlink signal with 50 MHz instantaneous bandwidth, and 10 dB PAPR. Among the typical linearity

Table 1. Comparison with SOA Ka-band DPAs

Techn.	Freq. (GHz)	$P_{out,sat}$ (dBm)	PAE_{sat} (%)	$PAE^{\#}_{OBO}$ (%)	G_{sat} (dB)	Ref
Si	28	22.4	40*	18*	10*	[10]
Si	26	18.7	32*	8*	12.5*	[11]
GaAs	27.25–29.75	27	37	12*	18	[9]
GaAs	28	30	38	10*	15*	[12]
GaN	26–30	36.1	26.7	15*	7	[13]
GaN	24–28	34	23	-	18	[14]
GaN	28.5–29.5	29*	30*	18*	4*	[15]
GaN	28–29	34	20	12	8	[8]
GaN	**27.5–29.5**	**34**	**18–23**	**8–16**	**8–9**	**T. W.**

PAE at 10 dB OBO
* Value extrapolated from graphs

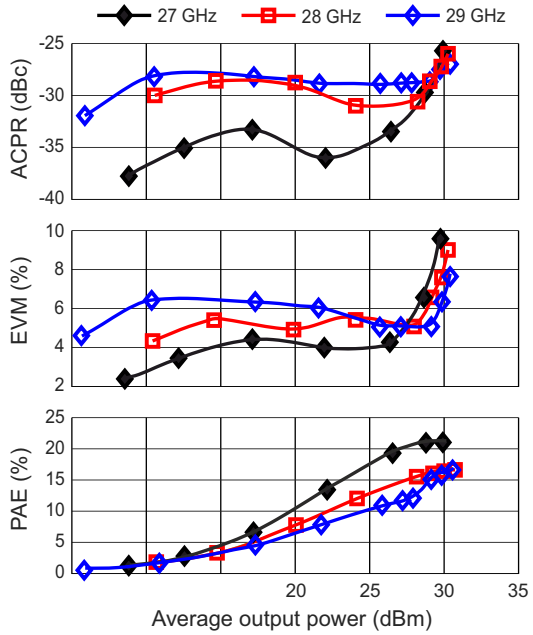

Fig. 6. Measured power sweeps under modulated signal excitation at 27 GHz (bleck), 28 GHz (red) and 29 GHz (blue): ACPR, EVM and PAE versus average output power.

figures of merit, such as Error Vector Magnitude (EVM), Adjacent Channel Power Ratio (ACPR), and Noise Power Ratio (NPR) [16], EVM and ACPR are typically adopted for ground applications and are therefore presented in this paper.

The characterization has been performed in the frequency range between 27 GHz and 29 GHz without digital pre-distortion. The setup has been pre-calibrated using an on-wafer thru in order to estimate the baseline distortion affecting the measurements, which results in EVM and ACPR of 0.8% and -48 dBc, respectively.

The 3GPP standard for the N259 band with 64-QAM 5G NR signals [6] requires a maximum EVM$<$ 8% and corresponding ACPR$<$-28 dBc.

Fig. 6 reports the measured ACPR, EVM, and PAE as a function of the average output power, at 27 GHz, 28 GHz, and 29 GHz. The amplifier is compliant with the 3GPP standard at all tested frequencies up to an average output power of about 28 dBm, without the need for any further linearization. The

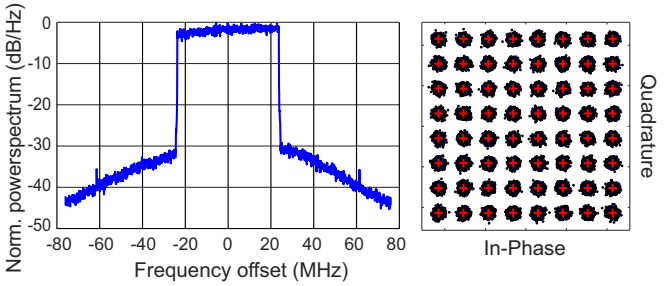

Fig. 7. Measured normalized power spectrum and corresponding 64-QAM constellation at 27 GHz, 26 dBm output power, with corresponding ACPR=-32 dBc, EVM=4% and PAE=20%.

corresponding average PAE results higher than 15 %. Towards the maximum tested power of 30 dBm which, according to the measured 34 dBm $P_{\mathrm{out,sat}}$ in CW and the 10 dB PAPR of the signal, corresponds to a strong signal clipping, the DPA maintains however ACPR<-25 dBc and EVM<10%.

The received output power spectrum and 64-QAM signal constellation at 27 GHz for an average output power of 26 dBm is reported in Fig. 7. The measured ACPR is -32 dBc with associated EVM=4% and PAE of 20%.

IV. Conclusion

This paper has presented the design, fabrication, and characterization of a 3-way Doherty power amplifier manufactured with the WIN Semiconductors' 150 nm gate-length GaN-SiC HEMT process, targeting efficient operation at deep back-off (around 10 dB) at 5G FR2 frequencies. Compared to the current state of the art at similar frequencies, the amplifier achieves competitive performance in terms of output power and PAE while showing very high intrinsic linearity, compatible with the 3GPP standard for 5G FR2 bands without the need for digital pre-distortion.

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References

[1] W. Hong, Z. H. Jiang, C. Yu, D. Hou, H. Wang, C. Guo, Y. Hu, L. Kuai, Y. Yu, Z. Jiang, Z. Chen, J. Chen, Z. Yu, J. Zhai, N. Zhang, L. Tian, F. Wu, G. Yang, Z.-C. Hao, and J. Y. Zhou, "The Role of Millimeter-Wave Technologies in 5G/6G Wireless Communications," *IEEE Journal of Microwaves*, vol. 1, no. 1, pp. 101–122, 2021.

[2] R. Quaglia and S. Cripps, "A Load Modulated Balanced Amplifier for Telecom Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 3, pp. 1328–1338, 2018.

[3] P. Saad, R. Hou, R. Hellberg, and B. Berglund, "A 1.8–3.8-GHz Power Amplifier With 40% Efficiency at 8-dB Power Back-Off," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 11, pp. 4870–4882, 2018.

[4] F. Wang, A. Yang, D. Kimball, L. Larson, and P. Asbeck, "Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 4, pp. 1244–1255, 2005.

[5] V. Camarchia, M. Pirola, R. Quaglia, S. Jee, Y. Cho, and B. Kim, "The Doherty power amplifier: Review of recent solutions and trends," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 559–571, Feb. 2015.

[6] "3rd Generation Partnership Project; Technical Specification Group Radio Access Network; NR; Base Station (BS) radio transmission and reception (release 15)," 3rd Generation Partnership Project-3GPP, TS 38.104, v.15.5.0, section 9, Standard, March 2019.

[7] L. Piazzon, R. Giofrè, R. Quaglia, V. Camarchia, M. Pirola, P. Colantonio, F. Giannini, and G. Ghione, "Effect of load modulation on phase distortion in doherty power amplifiers," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 7, pp. 505–507, 2014.

[8] A. Piacibello, V. Camarchia, P. Colantonio, and R. Giofrè, "3-Way Doherty Power Amplifiers: Design Guidelines and MMIC Implementation at 28 GHz," *IEEE Trans. Microw. Theory Techn.*, vol. 71, no. 5, pp. 2016–2028, 2022.

[9] A. Degirmenci and A. Aktug, "A High Gain Ka-Band Asymmetrical GaAs Doherty Power Amplifier MMIC for 5G Applications," in *2019 14th European Microwave Integrated Circuits Conference (EuMIC)*, 2019, pp. 116–119.

[10] N. Rostomyan, M. Özen, and P. Asbeck, "28 GHz Doherty Power Amplifier in CMOS SOI With 28% Back-Off PAE," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 5, pp. 446–448, 2018.

[11] G. Cho and S. Hong, "Ka-Band CMOS Power Amplifier Based on Transmission Line Transformers With Single-Ended Doherty Network," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 11, pp. 1223–1226, 2021.

[12] H. Xie, Y. J. Cheng, and Y. Fan, "A Ka-Band Watt-Level High-Efficiency Integrated Doherty Power Amplifier in GaAs Technology," in *2021 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*, 2021, pp. 287–289.

[13] Y. Yamaguchi, K. Nakatani, and S. Shinjo, "A Wideband and High Efficiency Ka-band GaN Doherty Power Amplifier for 5G Communications," in *2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2020, pp. 1–4.

[14] M. Bao, D. Gustafsson, R. Hou, Z. Ouarch, C. Chang, and K. Andersson, "A 24–28-GHz Doherty Power Amplifier With 4-W Output Power and 32% PAE at 6-dB OPBO in 150-nm GaN Technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 6, pp. 752–755, 2021.

[15] R. Ishikawa, T. Seshimo, Y. Takayama, and K. Honjo, "A 28-GHz-Band GaN HEMT MMIC Doherty Power Amplifier Designed by Load Resistance Division Adjustment," in *2021 16th European Microwave Integrated Circuits Conference (EuMIC)*, 2022, pp. 241–244.

[16] R. Figueiredo, N. Carvalho, A. Piacibello, and V. Camarchia, "Nonlinear Dynamic RF System Characterization: Envelope Intermodulation Distortion Profiles–A Noise Power Ratio-Based Approach," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 9, pp. 4256–4271, 2021.