Doctoral Dissertation
Doctoral Program in Electrical, Electronics
and Communications Engineering (35th cycle)

Ultra Low-Voltage and Ultra Low-Power Integrated Circuits targeting IoT and Next-Generation Biosensing

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Roberto Rubino
Turin, April, 2023

Summary

Digital electronics has led the development of finer silicon technology nodes improving performance, area, cost and computation efficiency in integrated circuits. The reduced dynamic range, degradation of the intrinsic transistor gain, physical limitations imposed by matching, have slowed down analogous advantages in analog and mixed-signals blocks, leading to increased design time and effort.

In the context of Internet of Things (IoT) and Biosensing applications this gap becomes more evident, since tiny ubiquitous nodes are required to sense and interact with the environment and the human body, power and area are heavily constrained, while design time and easy architecture reconfigurability and portability are a must to contain cost and being non-invasive.

Such applications usually require analog frontends with resolutions up to 12-14bits and moderate sample rates (up to MS/s), while required to operate over a wide, possibly unregulated, supply and achieving competitive energy and area figures of merit (FOM). This is the motivation to explore the design of novel digital-to-analog and analog-to-digital conversion techniques exploiting digitally intensive architecture to intrinsically benefit from scaled technology nodes and reduce design effort.

The Relaxation Digital-to-Analog Converter (ReDAC) has been extensively investigated in this thesis as a compact solution in IoT interfaces, starting from an analytical model of its operation, energy consumption, and intrinsic advantages with respect to known topologies. Integrated architectures featuring different calibration strategies based on clock frequency tuning have been developed in 40nm and 180nm CMOS technology and verified by post-layout simulations. Two ReDAC FPGA-based prototypes have been presented and a strategy to suppress parasitics-related nonlinearities has been studied and effectively demonstrated by measurements. A digital radix-based calibration strategy has been developed as a convenient alternative to the clock-tuning based calibrations, in a 180nm

simulated design.

A single-ended and a differential-output ReDAC implementation have been fabricated in a 180nm prototype featuring calibration and on-chip direct digital synthesis. The silicon verification validates the expected performance in terms of area and power dissipation of the ReDAC topology, proving to be a competitive solution compared to the state of the art in terms of area and power FOMs.

In the context of Biosensing interfaces, a Direct Digital Sensing Potentiostat (DDSP) has been presented aiming at non-enzymatic detection of glucose in Body-Dust particles. It replaces the conventional opamp-based architecture exploiting the concept of the digital-based operational transconductance amplifier to achieve order-of-magnitudes smaller area and power with respect to the state of the art while achieving good linearity in glucose detection. The design is verified based on post layout simulations developing an electrical model for the electrodes-solution interface.

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A mio padre

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Chapter 1

Introduction

This introductory chapter reports an overview of the Internet of Things ecosystem, which poses itself as one of the cutting-edge markets exploiting the More than Moore approach in profitable ways. Several challenges still need to be tackled in terms of integration, area, and power management in the edge nodes, therefore the main research directions and proposed design strategies are unfolded with a particular focus on digitally-intensive frontends and Digital-to-Analog Converters DAC. A review of the related fields of Internet of Wearable and Implantable Biosensors state-of-the-art is laid out, and reasons to explore digital-based amplifiers for the Next-Generation Biosensors are discussed. Finally, a review of the semiconductors trends in the last years as related to technological challenges faced in the decline of Moore's Law is presented.

1.1 The Internet of Things

The Internet of Things (IoT) concept can be traced back to 1985, from a speech given by Peter. T. Lewis at Congressional Black Caucus Foundation 15th Annual Legislative Weekend in Washington, D.C, while the Internet was still at his dawn [1], [2]:

> *"By connecting devices such as traffic signal control boxes, underground gas station tanks and home refrigerators to supervisory control systems, modems, auto-dialers and cellular phones, we can transmit status of these devices to cell sites, then pipe that data through the Internet and address it to people near and far that need that information. I predict that not only humans, but machines and other things will interactively communicate via the Internet. The Internet of Things, or IoT, is the integration of people, processes and technology with connectable devices and sensors to enable remote monitoring, status, manipulation and evaluation of trends of such devices. When all these technologies and voluminous amounts of Things are interfaced together – namely, devices/machines, supervisory controllers, cellular and the Internet, there is nothing we cannot connect to and communicate with. What I am calling the Internet of Things will be far reaching."*
>
> Peter Lewis, 25-28th Sep 1985

The IoT concept was later brought to a larger audience in 1999 by the MIT's Auto-ID Centre member Kevin Ashton, presented as a network of Radio-Frequency IDentified (RFID) devices [3].

From a more general perspective, the IoT has broadened its meaning over the decades as the technology-enabled interaction of people and smart objects capable of data gathering and processing, remote sensing, monitoring, and acting [4], as applied to infrastructures, home living, health, and environmental monitoring [5]. The pervasive sensing enabled by IoT can exempt humans from repetitive tasks and automatable labor exploiting data-driven decisions, allow to track objects in the global economy and manage them along distances, track human health and disease diffusion, enable geosocial networking, monitor the environment [4].

The IoT ecosystem (Fig. 1.1) operates at different levels: from the Trillion sensor nodes (leaf nodes) expected by 2025, interacting with the physical world, to the 10 Billion concentrators collecting information up to the 100 Million Cloud data elaborators (Fig. 1.2) storing and processing data [4].

The IoT trend has ever been fueled by the semiconductor industry (Fig. 1.3), the exponential improvement in efficiency and cost per unit transistor, resulting in rapidly enhanced computational power, wireless data transfer, and sensor interfaces up to a two orders of magnitude per decade [5].

Integrated Circuits (ICs) seem still to be the only viable technology able to target the scale and the sub 1$ cost per unit of such tiny devices [8], thanks to an economy of scale and the avoided overhead cost and

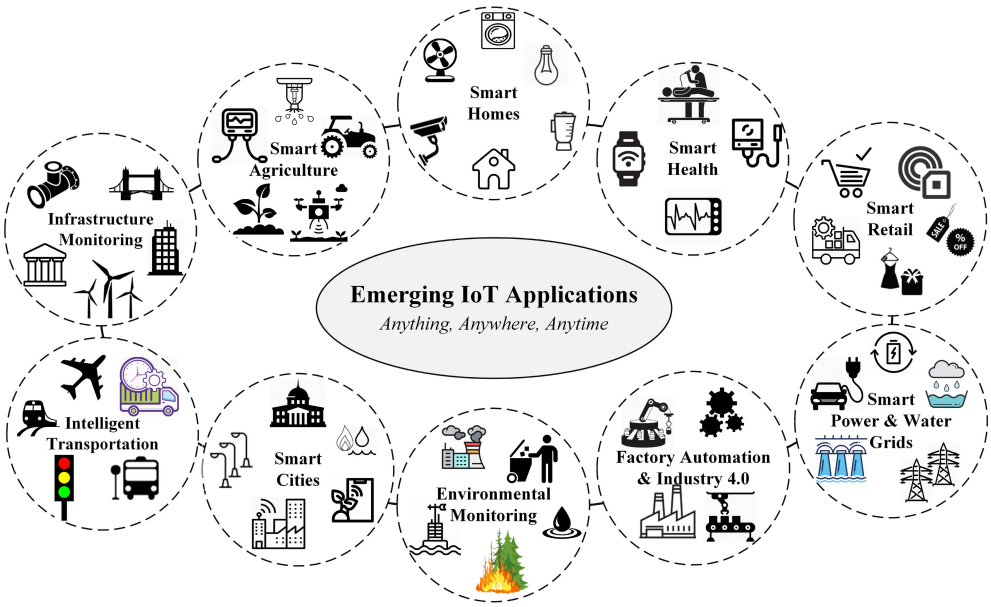


Figure 1.1: IoT applications. Source [6]

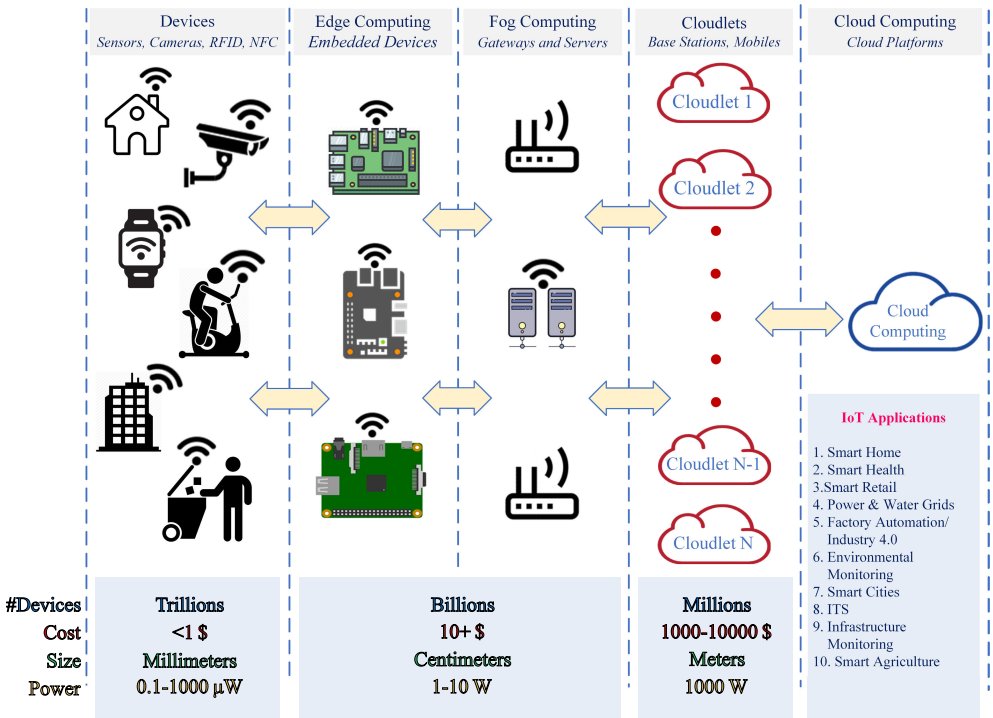


Figure 1.2: IoT ecosystem from the Device level to the Cloud: units, cost, size and power. Adapted from [6].

suboptimization of PCB-designed solutions (Fig. 1.4).

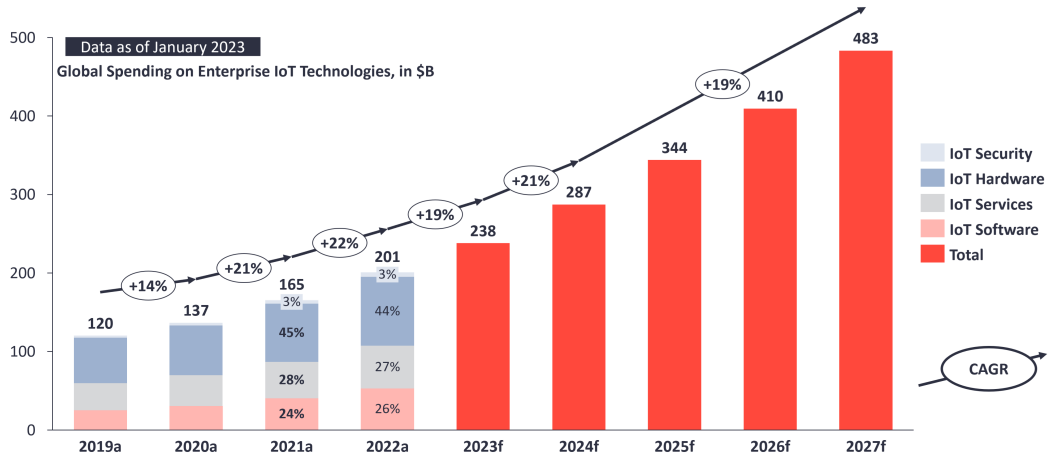


Figure 1.3: Global IoT market grows in 2023 despite economic downturn: IoT Hardware is leading. Adapted from [7].

The advances to tackle these challenges will come no more solely from bare CMOS scaling but enabled by the combination of different expertise and innovations at the system level, circuit level and design methodologies [9]. Several challenges need still to be tackled and a holistic approach is required.

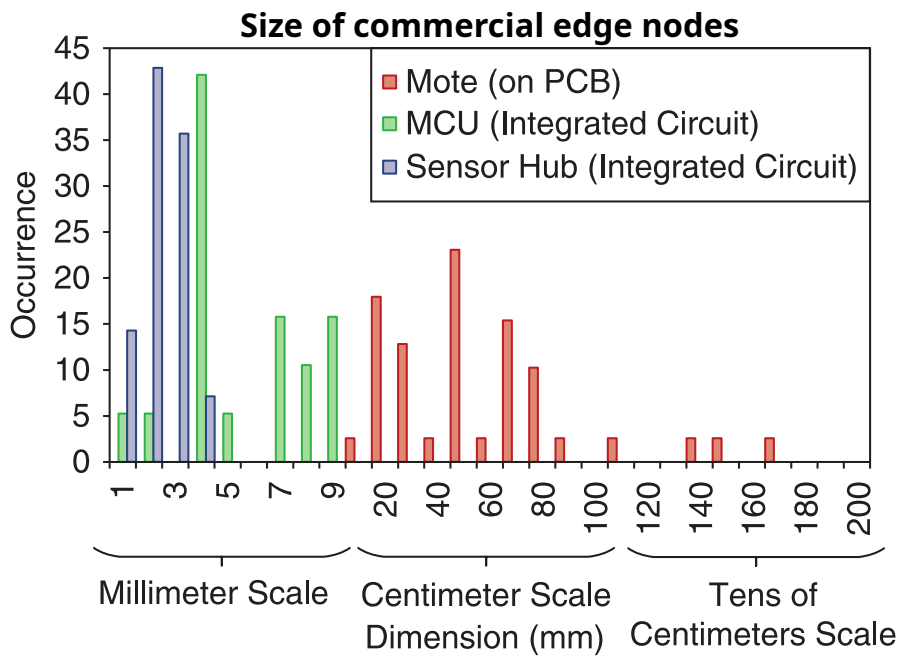
1.2 IoT Architectures and Challenges

The huge amount of expected leaf nodes in IoT need to satisfy certain criteria [5]:

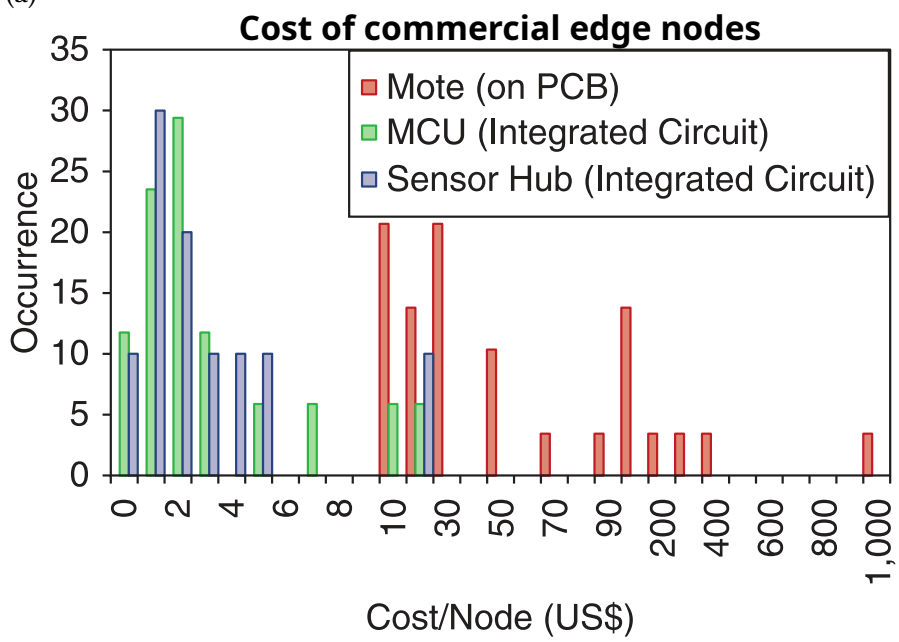
- non-intrusive (mm-scale size);
- reduced cost (sub 1$);
- non plugged, therefore self powered;
- long lifetime to avoid an unbearable maintenance cost.

Among the multiple possible architectures of edge nodes, several feature are recurrent [4] (see Fig. 1.5):

- a processing unit in the form of microprocessor (MPU) or microcontroller (MCU);
- communication-enabling unit, composed of a transmitter (TX) and receiver (RX);



(a)



(b)

Figure 1.4: (a) Size of IoT edge sensors divided by architecture and (b) cost of IoT edge sensors divided by architecture. Adapted from [8]

- energy storage in the form of batteries, capacitors, supercapacitors;
- energy harvesters (photovoltaic, vibration, thermoelectric, ultrasound);

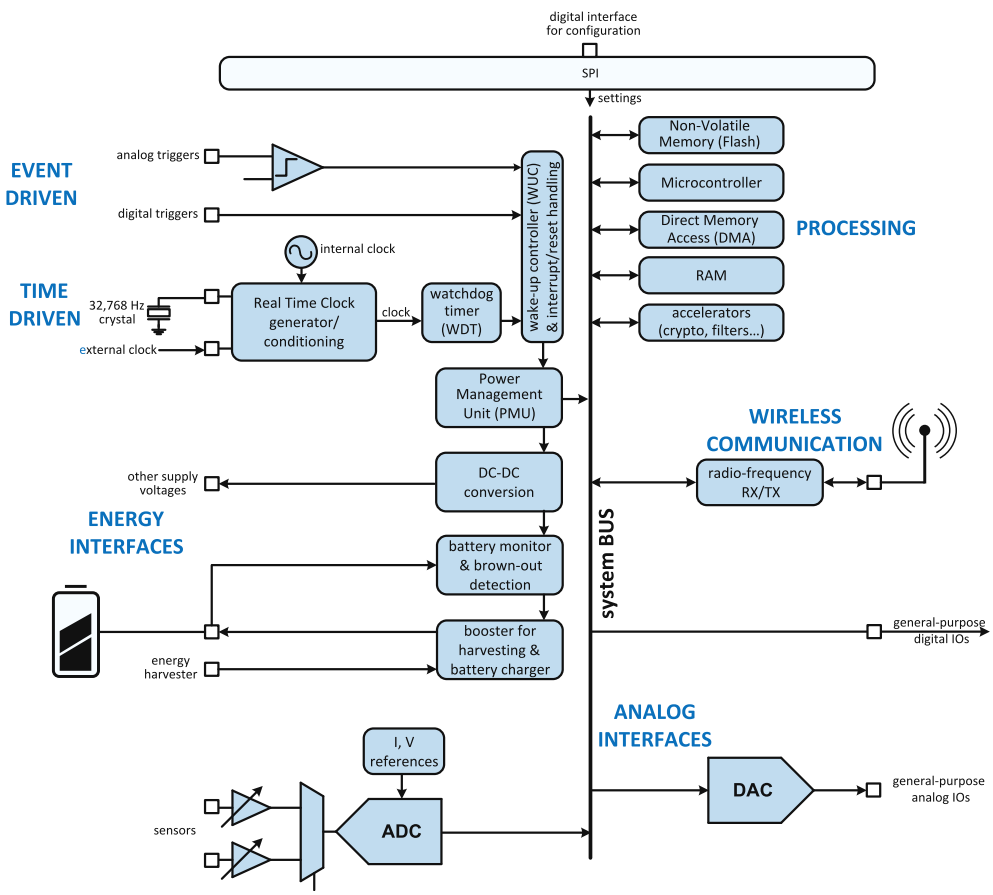


Figure 1.5: Generic structure of an IoT edge node. Adapted from source [4].

- time (clock) and voltage/current references;
- sensing/acting interfaces, such as Analog-to-Digital Converters (ADC), Digital-to-Analog Converters (DAC).

1.2.1 Battery-operated Nodes

The energy source plays a crucial role in the size and cost of IoT nodes, being their power heavily constrained, especially for wearable devices and environmental sensors [4], where unacceptable battery replacement rate and the consequent risk and maintenance costs must be avoided.

Up to present days batteries have been the dominant power source for IoT nodes, thanks to their precisely quantifiable electrical characteristics and a guaranteed energy flow. If the battery is the only energy source of the system, reducing the node average power certainly benefits its lifetime, which ultimately coincides with the battery lifetime itself [9].

Since battery technology is evolving at slower pace (doubled performance per decade) than electronics, to allow ubiquitous sensing with limited or no battery use demands a much lower power consumption than the state of the art [5]. As shown in Fig. 1.6 the total average node power required to provide weeks-to-year lifetime using tiny batteries should be below the microwatt level, and down to tens of nanowatts [9].

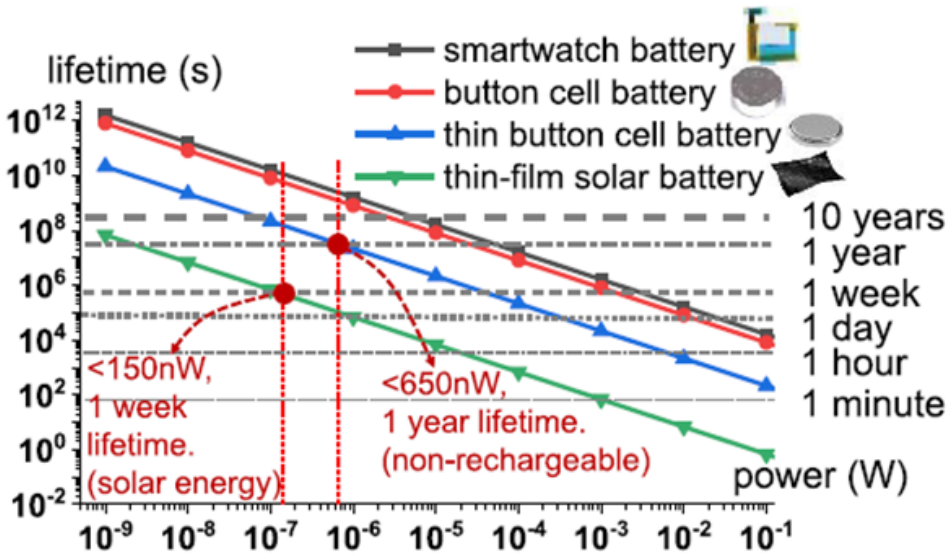


Figure 1.6: Power consumption required for IoT nodes to achieve long lifetime in relation to battery types. Source [4], [9]

1.2.2 Purely Harvested Nodes

As opposed to purely battery-powered systems, nodes which only rely on energy-harvested power are an option. This solution impairs the system operation every time the instantaneous harvested power falls below the minimum required by the application, while imposing extra area and cost demand due to the external transducer/antenna and possibly more complex power regulation [9]. It also imposes constraints on the architecture, since millimiter scale harvesters are not able to rake more than tens of nanowatts instantaneous power, making an exception for those found in industrial environments [5] (see Fig.1.7).

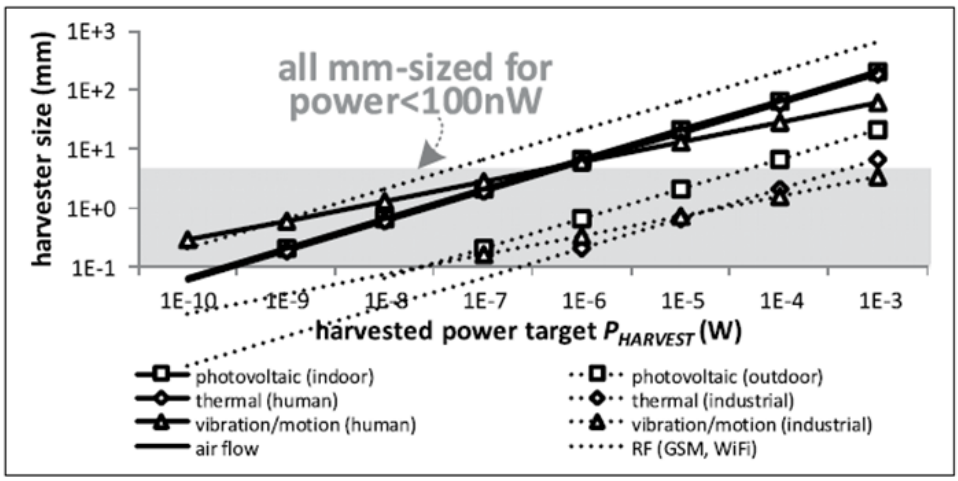


Figure 1.7: Harvester size related to required harvested power in presence of different ambient energy sources. Source [5].

1.2.3 Hybrid Nodes

As a tradeoff between the battery-only and harvested-only solutions, an hybrid solution employing a battery and harvester is viable. The node can continue to operate even if no power is currently being harvested, provided that enough residual energy is stored in the battery or enough energy is gathered from the environment, and the excess energy employed to recharge the energy tank.

Thanks to this compromise the battery and the harvester can both be reduced in size, and node lifetime extended [5].

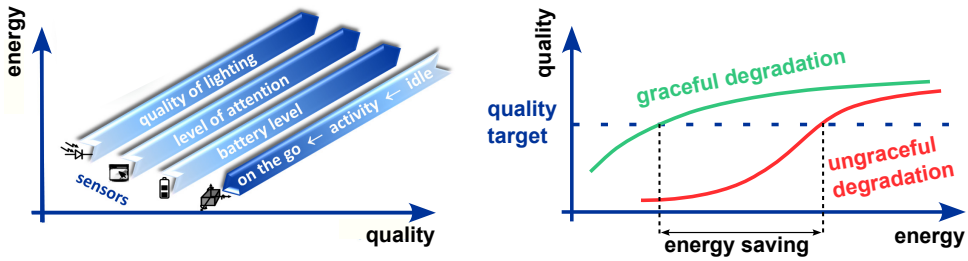
1.2.4 Battery Indifference and Energy-Quality Scaling

To reduce further the power requirements with respect to hybrid systems, battery indifferent nodes have been proposed, operating under direct harvesting and avoiding the need for power regulation, which saves both the area and power overhead.

To this purpose, the system must be designed to operate under a large range of supply conditions, trading power consumption and supply voltage with performance (quality), whenever the available energy allows it [10]. The ability to operate under wide energy availability conditions drastically reduces the chance of the node being completely off the grid, resulting in practically always-on nodes.

Such battery indifferent solutions are possible only by removing the power floor imposed by a power management unit (PMU) and the lower

limit dictated by analog and mixed signals (AMS) subsystems, developing circuit architectures and design techniques enabling graceful performance degradation in digital and analog blocks coordinately, when reduced-supply scenarios take place [5] (Fig. 1.8).



(a) (b)

Figure 1.8: (a) Conceptual diagram on how the sensor node performance can be scaled depending on the available energy and (b) possible energy saving for a given quality target if node performance gracefully degrade. Adapted from [10]

Once defined the "quality" for both digital and analog blocks as the accuracy of the task they need to perform, it has been shown that it consistently scales with the dissipated "energy" in several applications: digital logic, artificial intelligence algorithms, sound, image sensing are inherently robust examples in which energy-quality scaling can be successfully applied [8]. Moreover, the single-node quality requirement can be further relaxed in some cases, relying on statistical inference on the aggregate information from swarms of nodes.

1.2.5 Communication and Computation Efficiency

The wireless interface is covering a large part of the IoT node energy budget. Best transceivers consume tens of nanojoules to transfer a bit over a ten-meter range [8], and their performance is not expected to improve much in the next future, since they already operate close to the physical limit.

The strategy will then be to reduce the amount of transmitted data, not only by Compressed-Sensing techniques, exploiting smart data pre-processing, low power artificial intelligence, Neural Networks, and classification to extract the relevant features of signals [9]. The local energy saving will also reduce global power consumption at the system-level since the synthesized data benefit will ripple up to a reduced computational load at the Cloud.

All these targets need to be pursued along with improved standardization in communication, since largely diverse protocols are used nowadays in the IoT ecosystem [4].

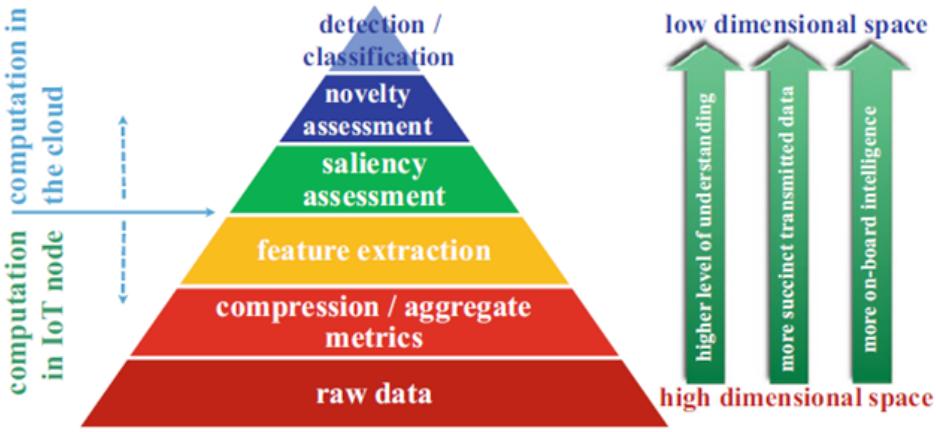


Figure 1.9: Data compression and feature extraction reduce the data dimensional space from the edge to the cloud. Source [4].

1.2.6 Wearable and Implantable Biosensing

Along with the Internet of Things, the Internet of Wearables (IoW) and Smart Health [6] are gaining attention in applications such as chronic health monitoring, safety in the workplace, sports, defence, and law enforcement, imposing design challenges both at the system and circuit level [11]. Intelligent remote health monitoring is of particular importance for the early diagnosis of diseases employing implantable, wearable sensors and body area networks (BAN) [6], which are ultimately connected to the IoT to help doctors in Point of Care (PoC) medicine. Real-time health monitoring is then moving from a clinic-centric towards a patient-centric service [6], especially useful for patients with chronic diseases and older people. In the area of sports and fitness activities, trackers like smartwatches, smartphones, smart glasses, mouth guards, hearables, jewels [12], and smart insoles [13] are more and more employed not only by professional athletes [14] but by ordinary people as well, concerning calories intake, sleep cycles, heart rate and steps taken during the day [6] to monitor sedentary lifestyle. Implantable biological sensors, alongside the wearable ones, are desirable and enabled by microelectronics miniaturization, advances in nanotechnologies and biocompatibility of materials. Flexible and skin-adhering electronics, partially or fully implantable devices, pacemakers, tattoos detecting glucose by bio-sensitive inks [12] are

being developed for in-vivo monitoring to minimize patient discomfort.

In-vivo monitoring of biomolecules through micro electrochemical [15] sensors is being desired for common diseases like diabetes, tumors, and neurological disorders [16] to reduce the time of traditional diagnosis in high-end medical laboratories and provide personalized therapy [15].

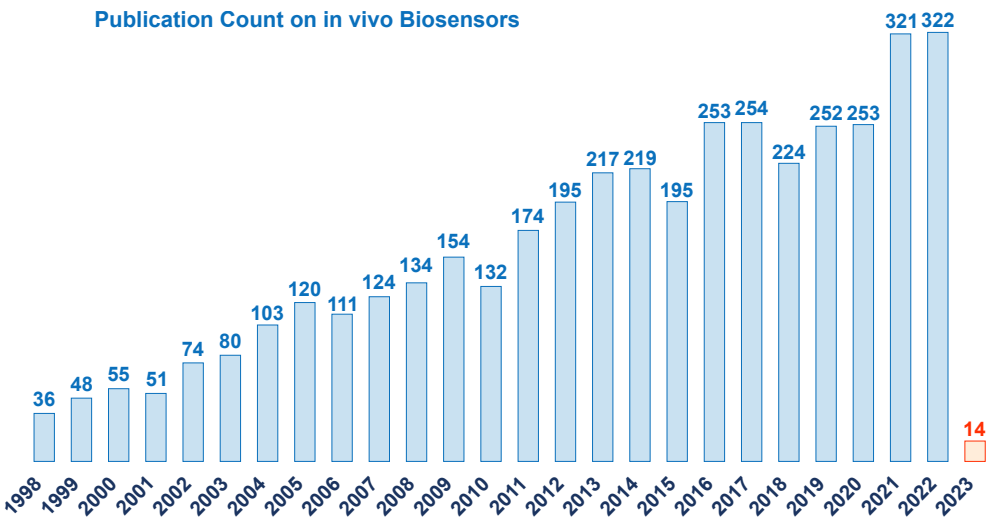


Figure 1.10: Number of publications on in-vivo biosensors over time. Adapted from [16].

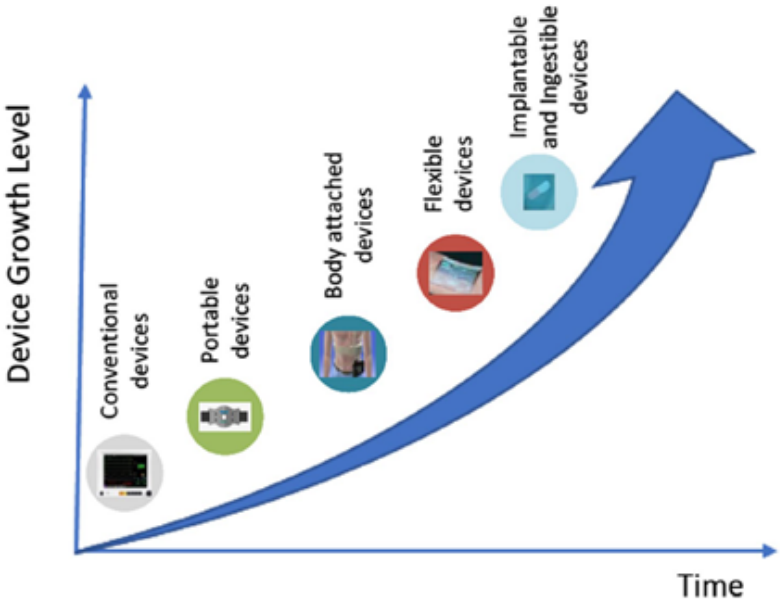
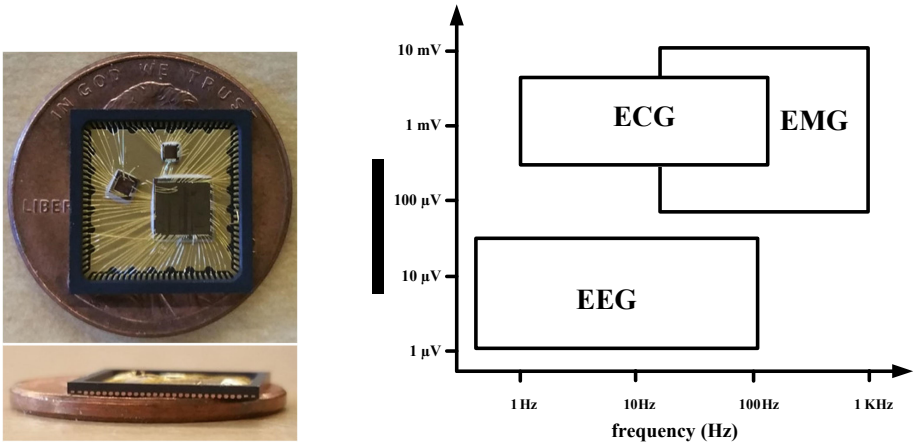


Figure 1.11: Evolution of biosensors from conventional to implantable devices. Source [12].

As per IoT nodes, IoW devices require ultra-low power consumption to achieve the desired continuous operation. Requirements become more stringent if the power source (e.g., battery) can not easily be replaced or recharged, eventually requiring sleep-mode capabilities [12] or energy harvesting [17]. electrocardiography (ECG), electromyography (EMG), photoplethysmography (PPG), electroencephalography (EEG) [12] are among the most common methods for in vivo monitoring, as well as electrochemical methods such as chronoamperometry (CA) cyclic voltammetry (CV) and electrochemical impedance spectroscopy (EIS) [15].

ECG (EMG) record electrical activities of the heart/muscles through electrodes, allowing the detection of wave patterns with amplitudes of few millivolts related to particular diseases or muscular activities in a frequency range of 0.05 Hz to 120 Hz (1 kHz)[12].



(a) (b)

Figure 1.12: A batteryless SiP for ECG monitoring [18] (a) and amplitudes and frequency bands of common electrical biosignals [19] (b).

A large family of biosensors is electrochemical, employing chronoamperometry (CA), cyclic voltammetry (CV), electrochemical impedance spectroscopy (EIS), exploiting the relation among electric current, potential or impedance to assess biological tissues parameters or concentration of analytes in bodily fluids [15]. Those sensors are required to apply determined fixed potentials, sinusoidal or swept potential/currents [20], or arbitrary stimuli patterns while measuring the electrical quantity of interest. Stimuli generation needs to be low-distortion [21], dissipating low powers in the microwatt range [22] having bandwidth ranging from few Hz to hundreds of kHz. At the same time, robust architecture and modularity enable multiple-stimuli generation in parallel channels [23].

1.3 Digital implementation of Analog and Mixed-Signal blocks

In previous sections the concept of battery-indifferent nodes and energy-quality scaling have been presented, and its requirement for coordinated performance scaling of analog and digital blocks at the same time. Since technology node development has been focused on improving performance of digital circuits, a possible strategy to get coordinated performance scaling at the system level is to exploit mostly-digital and digitally intensive techniques to implement traditionally-analog blocks, which trend has recently gained much popularity [24] (Fig. 1.13).

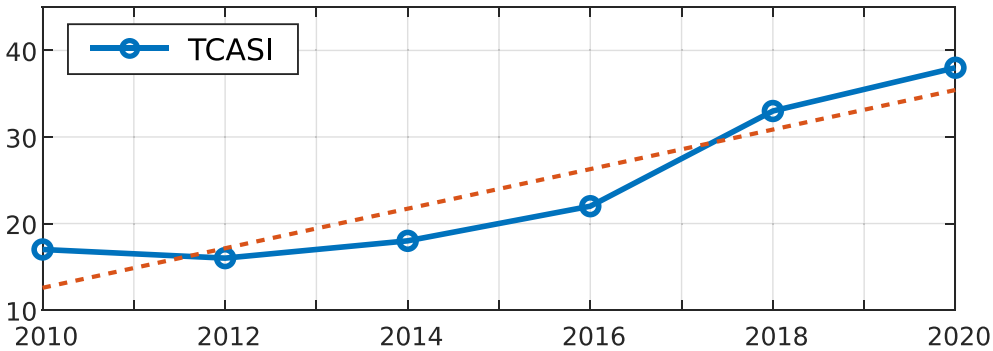


Figure 1.13: Digital intensive Analog/RF building blocks published onIEEE Transactions on Circuits and Systems I (TCASI) - Regular Papers, from 2010 to 2020. Source [24].

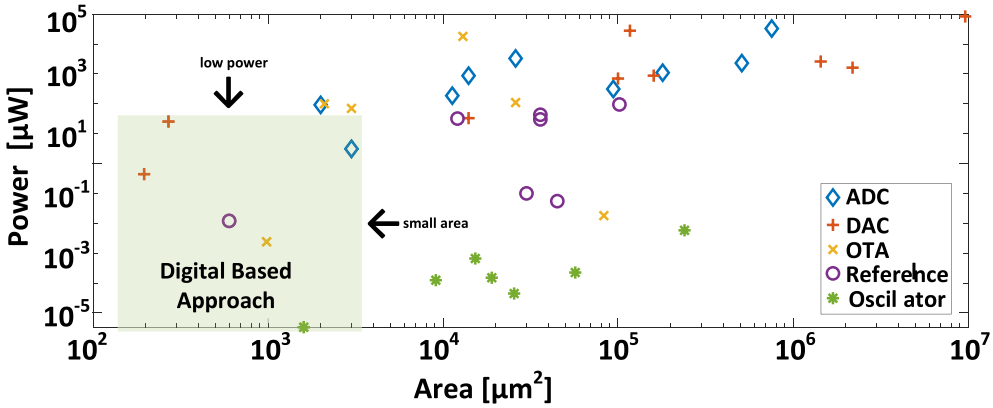


Figure 1.14: Comparison of digital-based AMS blocks in terms of area and power with respect to conventional approaches. Source [24].

The digital implementation of analog and mixed signals (AMS) blocks like operational amplifiers, data converters, references, oscillators, transceivers,

is intrinsically benefiting from the lower power consumption, smaller area footprint, and reduced supply voltage operation which has pushed the silicon technology development in advanced technology nodes aimed at improved digital computational power Fig. 1.14.

1.3.1 Energy-Efficient Frontends for the IoT

Internet of Things employs a variety of sensors, depending on the applications: from voltage-output sensors (sound, image, temperature) to current-domain sensors (DNA sequencing, photoelectric, blood saturation) to capacitive sensing (moisture, integrated motion units (IMU), contact detection) [9] (Fig. 1.15). To digitize such signals, or act on the environment, Digital to Analog Converters (DACs) and Analog-to-Digital Converters (ADCs) with ultra-low power operation and adequate resolution are required.

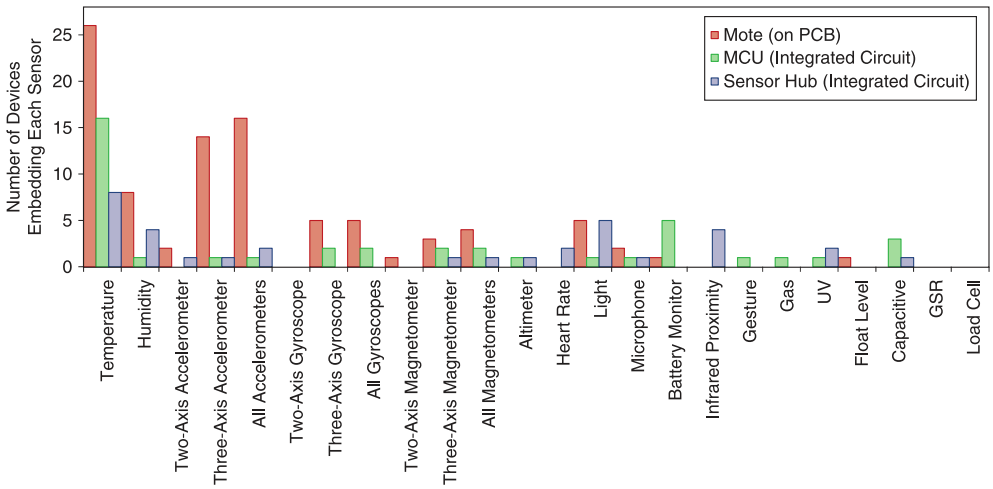


Figure 1.15: Histogram of the type of sensors used in edge IoT nodes. Source [8]

The most common interfaces employed in IoT are ambient-sensing ones: temperature, humidity, motion, magnetic field, and proximity, requiring ADC resolutions ranging, most of the times, from 6 to 16 bits [8], while DAC converters show a resolution range from 4 to 13 bits (Fig. 1.16).

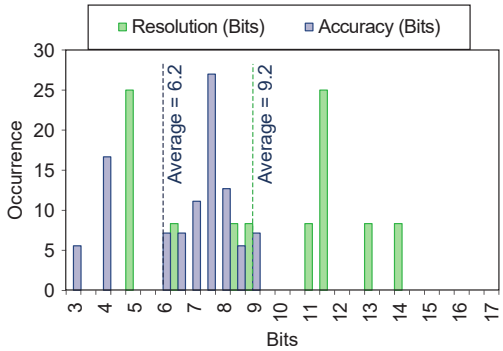
Most common ADC architecture are Successive Approximation Register (SAR) ADCs, for moderate sample rates (MS/s range) and resolution (up to 16-18 bits), and Sigma Delta architecture for lower sample rates (hundreds kS/s) and higher resolution (up to 20-24 bits) [9].

Since energy per conversion in data converters increases exponentially for every extra bit of accuracy, resorting to a circuit structure whose

Table : The ADC resolution range versus type of sensor.

	minimum	average	maximum
Temperature	4	9.2	13
Humidity	—	12	—
Accelerometer	10	11	13
Gyroscope	—	12	—
Magnetometer	—	12	—
Altimeter	—	6	—
Heart rate	—	14	—
Light	12	—	16
Microphone	—	16	—
Camera	8	—	12
Battery monitor	—	5	—
Infrared proximity	—	8	—
Gas	12	—	24
Ultraviolet	13	—	20
Capacitive	—	12	—

(a)



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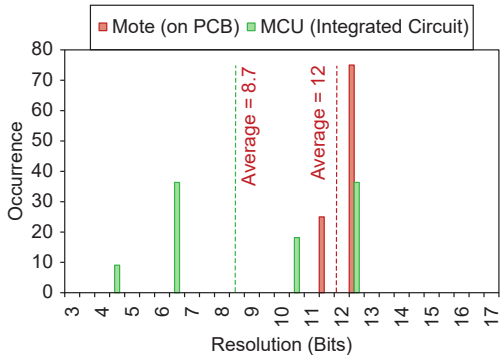


(c)

Figure 1.16: ADC resolutions for different sensors (a), DAC resolutions and accuracies in IoT nodes (b), ADC resolutions for temperature sensors (c). Adapted from [8].

resolution can be tailored to the application without complex architectural re-design and dynamically scaled with the available power is of strong relevance.

Asynchronous domain ADCs, like Level Crossing ADCs, avoid the need for synchronous sampling related to a fixed clock, storing only the information about the time instants the signal crosses pre-defined thresholds [9].

1.3.2 Why Bitstream Data Converters?

Integrated frontends employed in IoT applications demand new approaches to analog-to-digital (A/D) and digital-to-analog (D/A) conversion, aiming at significant power and area reduction, matching resilience and cost-effectiveness [25].

To highlight why new approaches are beneficial in such applications, a brief overview of conventional converter topologies is presented to show how bitstream, matching insensitive architectures are advantageous.

Most conventional Nyquist-rate converters rely on the matching of elementary unit elements such as capacitors, resistors, or current sources to perform the conversion. They often employ auxiliary blocks necessary to the converter operation: references/bias networks, operational amplifiers, and multiplexers/decoders [26].

A careful layout is necessary since mismatch among unit elements translates into static and dynamic converter errors.

Switched-capacitor architectures are ubiquitous in both DACs and ADCs because of the excellent linearity achievable in integrated capacitance [27]. Nevertheless, the number of unit elements required for weighted-capacitors converters increases exponentially with the number of bits, with a clear drawback in terms of area footprint. Split-capacitor arrays mitigate the area problem, unfortunately requiring an attenuation capacitor being a fraction of the unit one, imposing additional care in the layout [28].

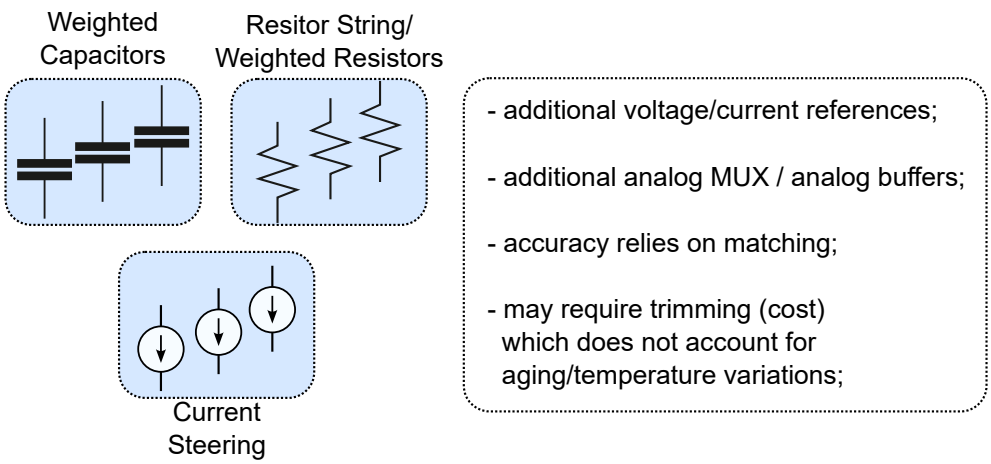


Figure 1.17: Considerations on data converters relying on weighted or matched elements.

Resistor-based converters like Resistor-String or R-2R converters demand similar design efforts regarding element matching. To achieve the desired accuracy, resistor geometries often need to be larger than the minimum the technology allows. A proper choice of resistor type is due to get an overall compact area even when several kilo-Ohms are desired for the unit resistor. Too-small absolute values can indeed easily impair efficiency [28]. Even if Resistor-String converters exhibit monotonic behavior, the number of switches increases exponentially with the number of bits, affecting the area, limiting the resolutions to less than 8 bits, and possibly the

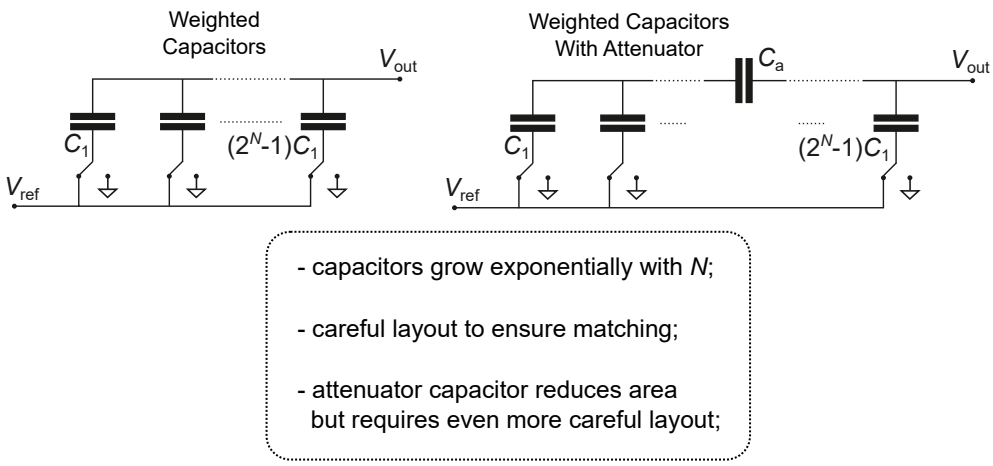


Figure 1.18: Considerations on data converters relying on weighted-capacitors.

bandwidth due to the parasitic capacitance of the off-switches. The problem can be attenuated by using segmented converters, which nonetheless require additional analog buffering with evident power and area overhead [28]. Voltage-mode R-2R converters require a voltage reference generator with good load regulation since it needs to keep its accuracy under a wide range of code-dependent load resistances.

For resistor and capacitor-based converters, the matching of unit-elements is never perfect, so the obtained accuracy may not be sufficient for the target application. In these cases, the solution is to add laser trimming or fuses/anti-fuses calibration in the fabrication process, which results in extra manufacturing costs. Moreover, the trimming/fuse procedure is permanent and does not account for aging or temperature variations [28].

Current-Steering architectures exploit transistors operated in the active region as constant current generators. Cascode structures or resistive source degeneration are often employed to achieve adequate output impedance, which inherently poses a lower bound to the minimum supply voltage of the converter, impairing voltage scaling. The current sources can not be turned off, making it hard to achieve high energy efficiency. Instead, their current is carefully steered to avoid dynamic errors and glitches [26].

Current Steering architectures may employ a unary or binary-weighted selection of current sources. While the first method is monotonic and glitch-free, its area rapidly grows with the number of bits. On the contrary, binary-weighted structures optimize the area, requiring design care to avoid glitches when a large number of bits switches [28].

Noise-shaped converters improve the in-band accuracy by pushing a

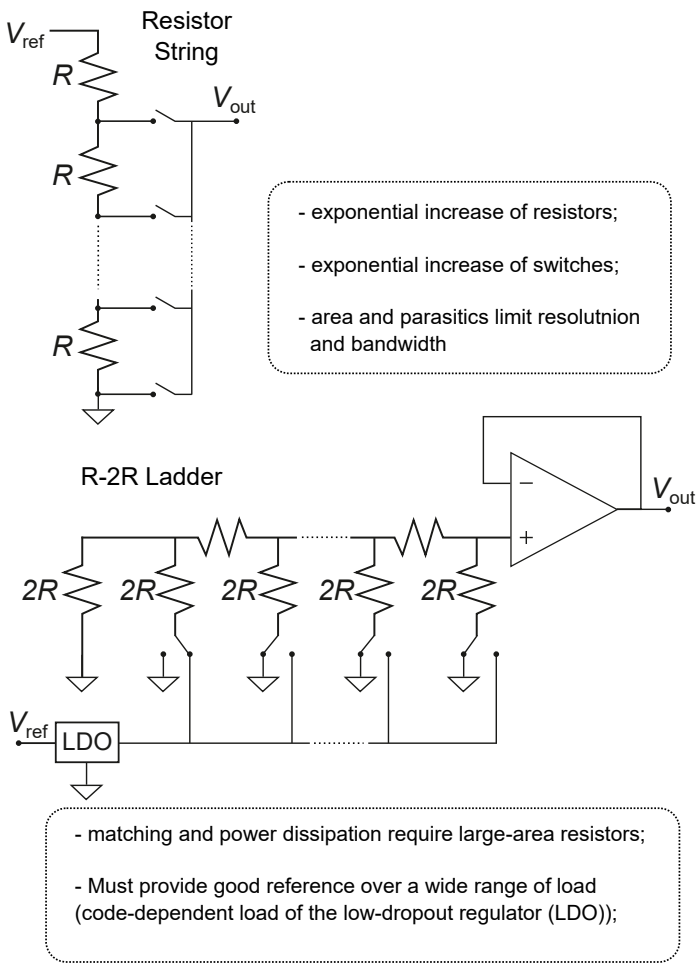


Figure 1.19: Considerations on data converters relying on weighted or matched resistors.

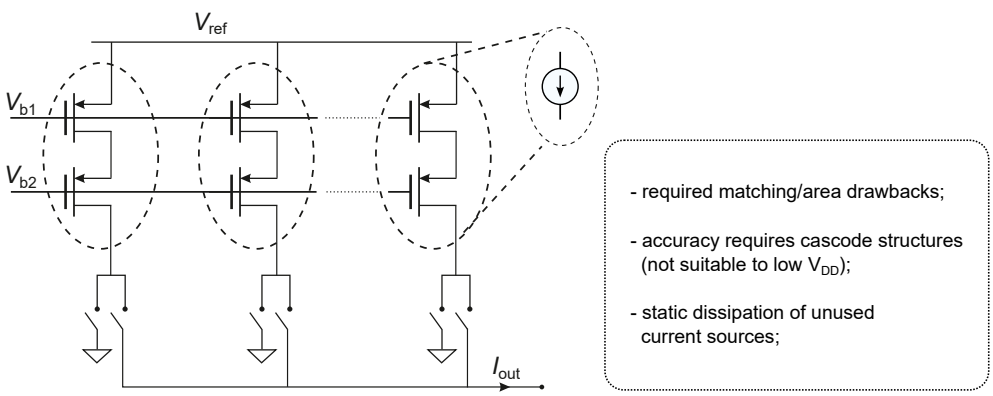


Figure 1.20: Considerations on current-steering data converters.

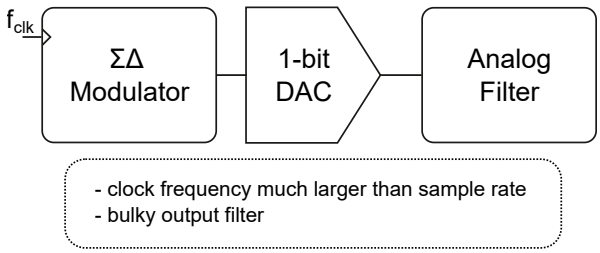


Figure 1.21: Considerations on oversampled data converters.

large portion of the quantization noise out-of-band. Unfortunately, they operate at a clock rate much higher than the signal bandwidth, which may be incompatible with the power budget of IoT nodes, in which digital information is processed at a much lower rate. Moreover, as previously noticed, resolutions required by most IoT applications are below 15 bits, which are achievable without resorting to noise shaping.

Integrated devices employed in IoT demand new approaches to analog-to-digital (A/D) and digital-to-analog (D/A) conversion, aiming at significant power and area reduction, matching resilience and cost-effectiveness [25].

Such achievements can be reached in nanoscale technologies exploiting the intrinsic advantage of digital circuits in relation to supply voltage scaling, area and power, re-thinking the frontends to be digitally synthesizable, possibly using a reduced number of passives, as in Fig 1.22 [29].

The novel ideas of the Relaxation Digital-to-Analog Converter, first presented in 2019 [30] and extensively covered in this work, and the Dyadic-Digital Pulse Modulator (DDPM) [31], are examples of bitstream, matching insensitive converters able to generate an analog output proportional to the digital input code with an all-digital circuit, except for an output RC network. The architectures exploit a digital stream of bits analogously to the well-known Digital Pulse-Width Modulation (DPWM) and single-bit sigma-delta strategies. Those strategies can aim at both D/A and A/D conversion since several ADC architectures employ DACs in feedback paths.

ReDAC: a bitstream-based data converter

As it will be analyzed in detail in the following chapters, the Relaxation Digital-to-Analog Converter (ReDAC) operationally requires quite simple hardware i.e. a single shift register with a number of bits N equal to the converter resolution and a first-order resistor-capacitor (RC) network, therefore suitable to digital-intensive implementation [30].

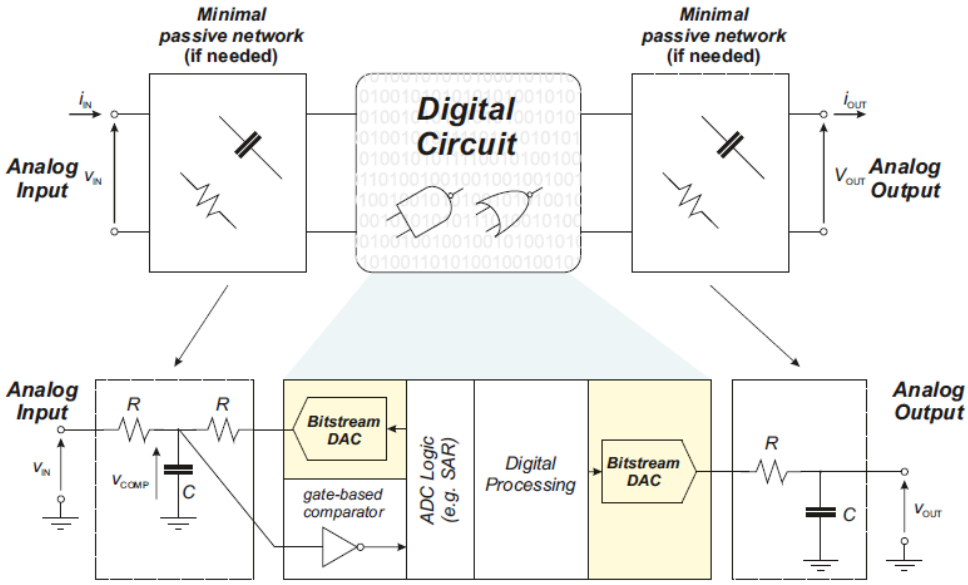


Figure 1.22: Digital-intensive processing architecture with bitstream-based data converters. Source [29]

Differently from converters exploiting unit-elements matching, the ReDAC resistor and capacitor do not require to be matched since linear operation is achieved by only satisfying a given ratio between the clock period and the RC time constant, achieved by calibration without any external absolute reference or bias.

Properly tuning the clock period enforces linearity under process-voltage-temperature (PVT) variations, and aging.

Avoiding the need for matching, the capacitor can be sized close to the $\kappa T/C$ noise limit, resulting in a highly compact and power-efficient solution. Unlike bitstream architectures exploiting pulse width modulation, the ReDAC only requires a minimum of $N + 1$ pulses for the single conversion, instead of 2^N, and keeps consistent accuracy up to the Nyquist frequency.

These advantages establish the ReDAC as an optimal solution in power and area-constrained, cost-effective, digital-based, low-voltage D/A converter suitable to nanoscale technologies and IoT needs.

1.3.3 Why Digital-Based Amplifiers in Next-Generation Biosensing?

From a system perspective, the generic biosensor requires acquiring the sensed signal, elaboration, and applying stimuli.

The sensing and stimulation, in particular, make extensive use of amplifiers and, in particular, operational amplifiers in acquisition front-ends [32], which find copious examples in neural recording/amplification [33]–[38], EEG [39]–[41] and ECG [42]–[44] acquisition, electrochemical impedance measurements [45]–[48], neural stimulation [49], [50], ultrasound imaging [51], brain-computer interfaces [52], [53], local body temperature [54] and on-skin pulse monitoring [55].

While traditional operational amplifiers (OA) and operational transconductance amplifiers (OTA) topologies can largely meet the dynamic range and bandwidth requirements of all bio-signals front-ends, their area, power, and minimum operating supply voltage may be too large to meet the needs of edge applications such as the ones required by the Body Dust (BD) concept [56]. Body Dust envisions the in-vivo distributed sensing of biological parameters enabled by electronic particles freely circulating in the human body and having size comparable to the human blood cells.

This is why to develop ultra-tiny, extremely low-power, digital-based OTAs operating at near-threshold supplies, for in-vivo energy autonomous sensing as proposed in the last chapters of this work.

1.4 Semiconductor trends supporting the IoT and IoW

Even though the names of technology nodes are no more related to the lithographic resolution, the half-metal pitch, which is still an actual indicator of the industry's technological advancement, is aligned with the IRDS forecasts up to 2023. The exponential miniaturization of electronics foreseen by Gordon Moore (unfortunately recently deceased) and made possible by improvements in silicon lithography is expected to flatten before 2030 as transistors approach the atomic scale and production expenses continue to increase (see Fig. 1.23).

Merely decreasing the gate length dimension (the so-called More Moore Strategy) is no longer the primary factor affecting logic circuit performance, as power and physical limitations have become increasingly stringent. In practice, since the last decade it became unfeasible to increase operational frequency beyond 10 GHz while also keeping power values within the 120-130W range (eliminating the need for wafer cooling, see Fig. 1.24). Consequently, semiconductor companies focused their transistor design efforts on reducing power consumption rather than maximizing transistor speed [57], paving the way for increased research interest in architectures

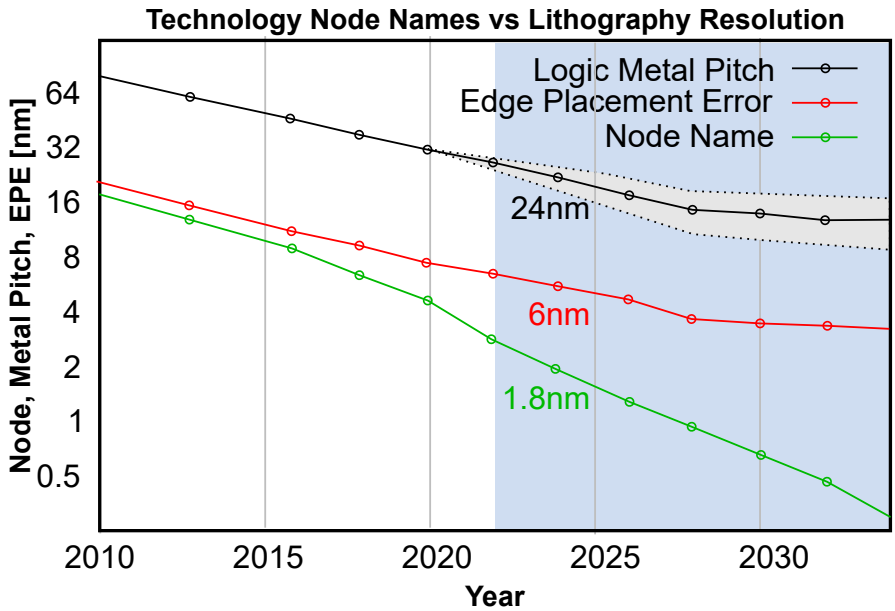


Figure 1.23: Technology node names are no more related to physical resolution. In the figure the node name, node metal pitch and edge placement error (EPE) are reported against year.X Adapted from [57].

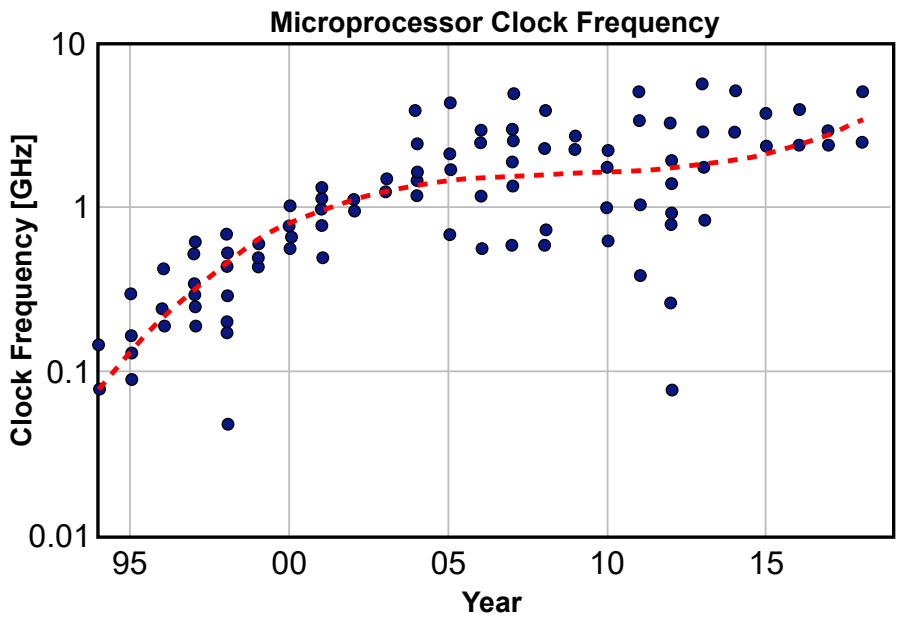


Figure 1.24: Microprocessor frequencies faced a power wall. Source [57].

addressing low power applications rather than pure increase in performance.

The roadmap for semiconductors has therefore been expanded in the

years to include not only the digital performance CMOS trend for memories and processors (led by miniaturization) but also the "Beyond Moore" and the "More than Moore" approach.

"Beyond Moore" is searching for completely novel devices and solutions (such as tunneling devices, molecular, magnetic, and quantum computing), while the "More than Moore" approach is devising heterogeneous integration of multi-functional analog and mixed-signal technologies for smart system applications. The "More than Moore" paradigm shifted the roadmap from a predominantly technology-driven to an increasingly application-driven perspective. It requires a highly multidisciplinary research environment coming from the understanding that progress in highly complex technology fields can only be achieved by cooperation along the complete innovation chain.

Functional diversification is promoted, while not necessarily following Moore's law, to offer added value to the end application [58]. Concerning the "More than Moore" approach, the Semiconductor Research Corporation foresees the next decade of semiconductors industry as characterized by five key breakthroughs [59]:

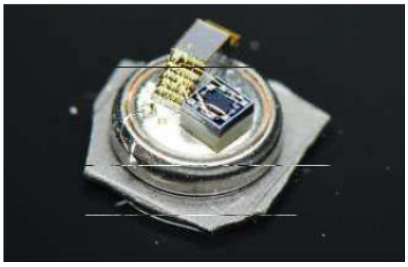
- develop smarter world-machine interfaces capable of sensing, perceiving, and reasoning with an analog-to-information compression ratio comparable to that of the human brain;
- devise memory solutions with significantly greater storage density capacity;
- resolve the imbalance between communication capacity and data-generation rates;
- deal with new security issues that arise in reliable, highly interconnected Artificial Intelligence (AI) systems;
- develop new computing paradigms achieving orders-of-magnitude energy improvements to meet the escalating energy demands of computing in relation to the global energy production.

Following the trend of the CMOS 100× per decade miniaturization, the upcoming decade is expected to be the one of millimeter and sub-millimeter scale computing, which will be the case for IoT edge nodes. Such dust-sized miniaturized systems will be able to be spread across objects for ubiquitous interactions.

The IoT is expected to be boosted by semiconductors economy and the More than Moore approach, integrating into a compact system MEMS,

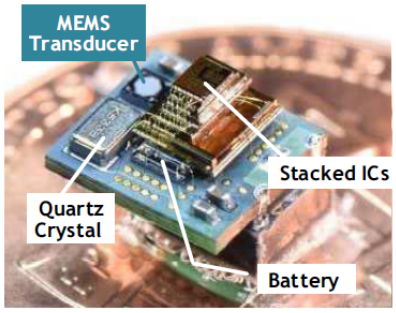
Application-Specific Integrated Circuits (ASICs), electrochemical interfaces, miniaturized actuators, printed semiconductors and flexible/organic supports [4]. The coexistence of diverse technologies will be boosted by System on Chip (SoC) and System in Package (SiP) integration, possibly exploiting 3D die-stacking of modular millimeter and sub-millimeter designs interacting with inter-layer bonding [60], self-assembed compliant structures and micro-origami batteries for higher energy densities [61]. The additional value for the consumer will come from additional services that the IoT provides, favoring smaller companies with specific expertise to enter the market [4] with Multiple Project Wafer (MPW) services, supported by the development of cheaper, maybe open source [62], user-friendly Electronic Design Automation (EDA) tools, as well as cloud-based design environments allowing modular and block-reusing IC design in well-established technology nodes.

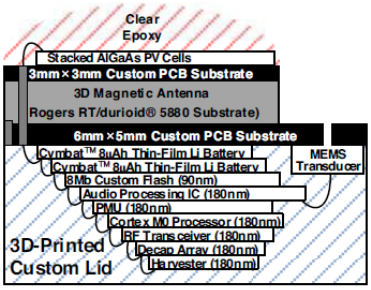
All these trends are indeed present in the framework of ubiquitous connected objects, the Internet of Things, and permeating more and more the biomedical, health, and wellness fields [63], as tackled by the Internet of Wearables (IoW) and the Next-Generation Biosensors, expanded in the following sections and addressed by the architectures in this thesis.



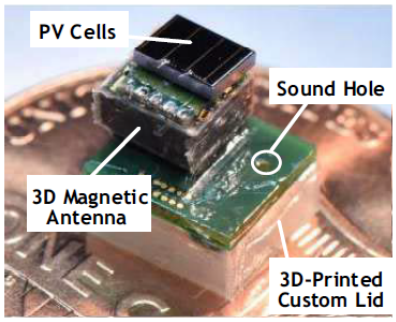
System Dimension	5.0×5.0×2.9 mm
Battery Capacity	1 mAh
Processor / Storage	Cortex M0 / 8KB SRAM
Active Power	27 µW
Sleep Power	24 nW
Processor Clock	80 kHz
Internal Supply	0.6, 1.2, 3.6 V
RF TX Energy	250 nJ/bit
Sensor SNR	49 dB
Sensor Conv. Energy	10.6 pJ/c.s @ 1 ms

(a)



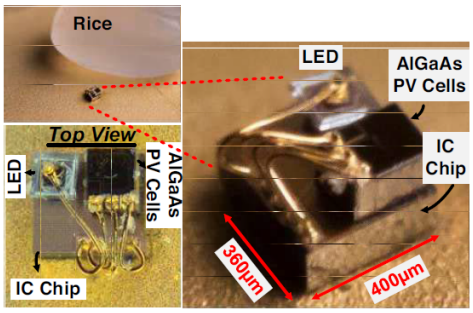


[Top side view]



Dimensions	6×5×4 mm³	
Storage	8Mb Flash / 24Kb SRAM	
Processor	ARM Cortex M0	
Battery	16µAh Thin-Film	
Energy Harvesting	Solar, 1.75µW @ 500lux	
RF TX Energy	3.67nJ/bit	
Overall System Power Consumption	Sleep	7.2nW
	Audio Processing	68µW
	RF TX	79µW

(b)



System Dimension	0.36×0.40 ×0.28 mm³
Technology	55nm
System Power	16nW
Processor	Cortex M0+, 4kb SRAM
Sensor	Temperature
Linearity Error	+0.38/-0.33C
Line Sensitivity	0.17C/V
RMS Resolution	0.034C
Communication	Optical
TX/RX Area	0.07 mm²
Transmit Distance	15.6 cm

(c)

Figure 1.25: Tiny nodes designed as SiP for pressure sensing (a) audio compressing (b) and cellular temperature sensing (c). Sources [60], [64]–[66].

1.5 Thesis organization

The thesis is structured as follows. In Chapter 2, a complete theoretical analysis of the Relaxation Digital-to-Analog Converter (ReDAC) is presented, highlighting the sources of non-idealities, expected conversion energy, parasitics contribution and general design guidelines.

In Chapter 3, the first self-calibrated ReDAC implementation based on voltage controlled oscillators is proposed and validated by simulations in 40 nm CMOS technology. This ReDAC occupies a tiny area of 677 μm^2, achieving a competitive 1.08 fJ/(c·s) energy FOM and a self-calibrated linearity of 9.06 ENOB under 0.6 V supply.

The need for a self calibrated hardware implementation leads to the ReDAC prototypes on FPGA presented in Chapter 4, reporting 10 bit 10.5 kS/s and 13 bit 514 S/s and exploiting clock-division based digital calibration. The implementation requires only 6 FPGA logic elements and the parasitics error suppression, which improves ReDAC linearity at minimum complexity overhead, is developed and validated by measurement for the first time.

The Radix-Based Digital Correction (RBDC) technique is presented in Chapter 5 as an alternative calibration strategy avoiding the need for clock tuning. A fully synthesizable architecture is developed and validated in 180 nm CMOS post-layout simulations, achieving comparable performance with respect to other calibration architectures of 9.4 ENOB at 1.45 MS/s. The required RBDC digital area (power) overhead is 5.6× (7.8×, FOM=9.21 fJ/(c.s.)) the one of the ReDAC core block in 180 nm technology, which tough becomes comparable in finer technology nodes thanks to area and power scaling, proving the aim of the digital-intensive approach.

Chapter 6 presents the first silicon implementation of ReDAC converters, fabricated in 180 nm CMOS technology, featuring a DCO-based calibration and embedded in a testing-oriented direct digital synthesizer system. Besides the Single-Ended ReDAC (SE-ReDAC) operating at 10 bit, 880 kS/s, a first differential version (Diff-ReDAC) on 13 bit, 100 kS/s is proposed. The multi-dice characterization of both ReDACs reveals calibration robustness and linearity consistency up to the Nyquist rate, while reporting very good energy Figure of Merit (FOM) and area-normalised Figure of Merit (FOM_A) compared to other silicon-verified DACs. The ability to keep linearity on a wide supply range and operate at the lowest reported supply of 0.45 V (featuring energy-quality scaling) prove the digitally-intensive ReDAC strategy in the framework of ultra-compact, reconfigurable, low-power architectures targeting IoT and IoW interfaces.

In the context of digital-based frontends for the next-generation biosensing targeting Body Dust, a fully-digital Direct Digital Sensing Potentiostat (DDSP) for electrochemical, non-enzymatic, glucose sensing is presented in Chapter 7 and verified by 180 nm post-layout simulations. The architecture reports high linearity under process-mismatch-voltage variations with a power consumption of 4.7 nW (3,400× less then the minimum reported) at the smallest area (150× less than the minimum reported) and the lowest supply of 0.4 V, by effectively exploiting the Digital-Based Operational Transconductance Amplifier (DB-OTA) concept to merge the potentiostat and the A/D conversion functions, conventionally separately implemented in state-of-the-art architectures.

Chapter 2

The Relaxation Digital-to-Analog Converter

This chapter introduces the operating principle of the Relaxation Digital-to-Analog Converter (ReDAC), unfolding the relation between errors on the optimal clock period and the converter linearity, and exposes an architecture-independent calibration principle. Guidelines are provided to design ReDAC converters operating close to the thermal noise limit. The expected energy per conversion is analytically derived, and the effect of components parasitics on the converter linearity is discussed, developing an effective strategy to suppress them. Finally, the ReDAC topology is compared to weighted capacitor DACs in terms of energy per conversion and physical implementation constraints.

As introduced in Chapter 1, digital circuit architectures have led the development of integrated CMOS technology in highly scaled nodes to increase their performance, compactness, power consumption, and cost-effectiveness. At the same time, designing analog and mixed signals (AMS) blocks is increasingly expensive in terms of design time and effort.

Rethinking analog blocks and data converters in their natively digital and time-based implementations is therefore extensively being investigated [4], [24], [25], [31], [67]–[77].

The Relaxation Digital-to-Analog Converter (ReDAC) principle, presented in 2019 for the first time [30], exploits these concepts.

2.1 Relaxation DAC Operating Principle

The Relaxation Digital-to-Analog Converter (ReDAC) bases its operation on the exponential response of a first-order RC network in order to produce 2^N quantiseed voltages which are binary weighted with respect to the bits of the digital input word n on N bits, expressed as in (2.1).

$$n = \sum_{i=0}^{N-1} b_i 2^i, \tag{2.1}$$

To achieve this, the RC is driven for a period $t \in [0, NT]$ by a stream of N voltage pulses of equal duration T in time and amplitude equal to zero Volt or the supply voltage V_{DD} depending on the value of the the ith bit b_i, $(i = 0 \ldots N-1)$ of the digital word to be converted, as shown in Fig. 2.1.

The bits are presented to the buffer starting from the least significant bit (LSB) b_0 to the most significant bit (MSB) b_{N-1} .

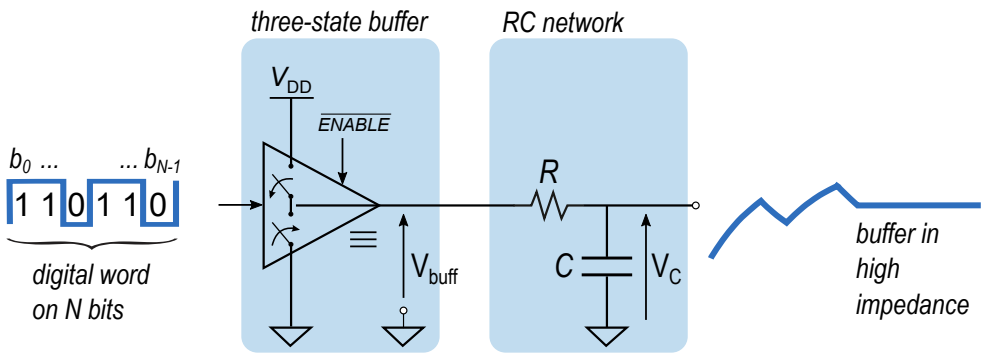


Figure 2.1: Basic Relaxation DAC principle.

The mentioned operation can be obtained by simple digital hardware, e.g. a parallel-in serial-out shift register driving the RC network with the bits of the digital word to be converted, LSB first, at constant clock frequency $f_{\mathrm{clk}} = 1/T$ through the three-state buffer as in Fig. 2.2(a).

The ReDAC operation follows the timing diagram in Fig. 2.2(b), loading the register at the first clock cycle and shifting each bit in the following

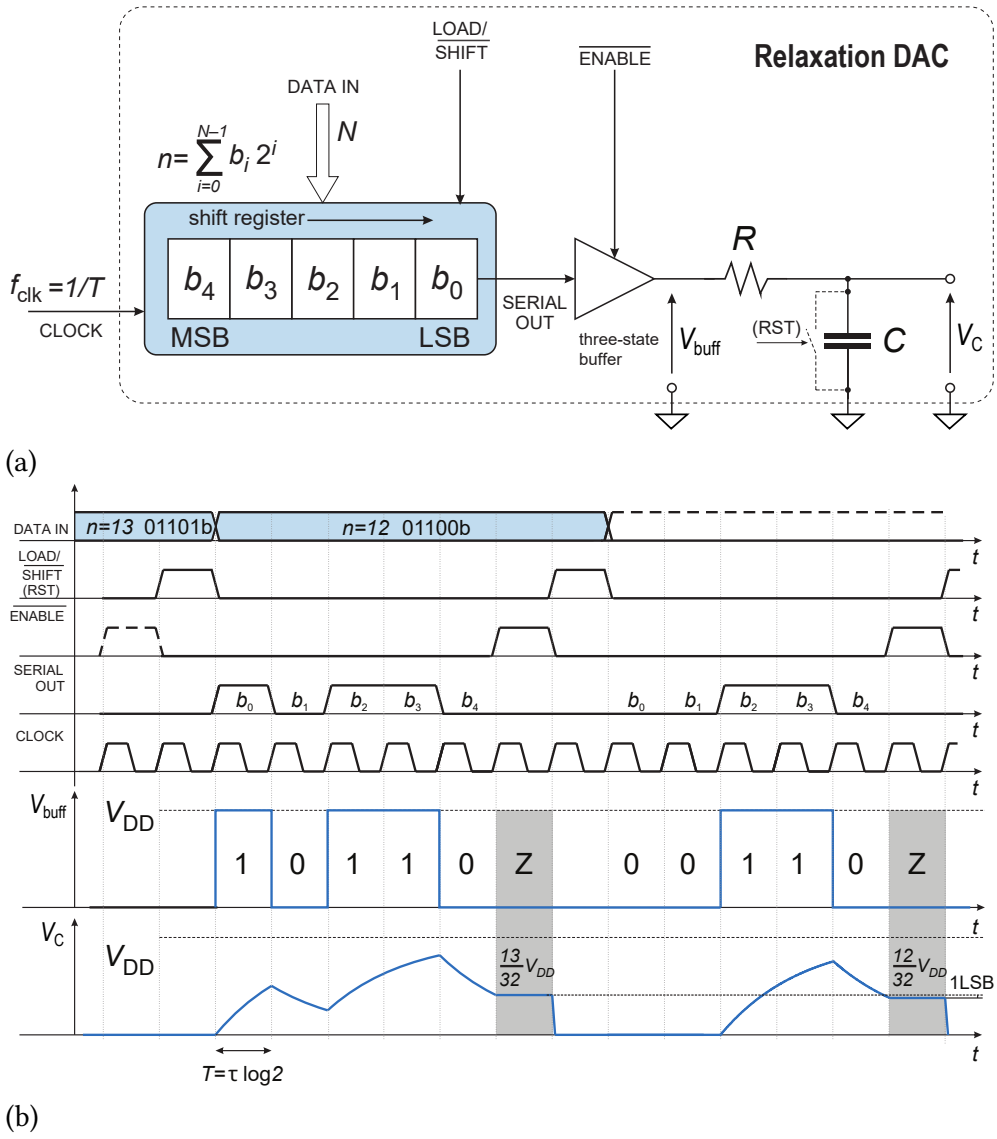


Figure 2.2: Hardware implementation of a ReDAC by means of a shift-register (a) ReDAC control timing diagram (b).

ones; the three-state buffer is put in high impedance (hold phase) by the $\overline{ENABLE}$ signal after the last bit (MSB) is shifted.

In the conversion time $t \in [0, NT]$, the RC network is driven by the unitary voltage pulse stream of v_{buff}:

$$v_{\text{buff}}(t) = V_{\text{DD}} \sum_{i=0}^{N-1} b_i \Pi\left(\frac{t}{T} - i - \frac{1}{2}\right)$$

where $\Pi(x)$

$$\Pi(x) = \begin{cases} 1 & |x| < \frac{1}{2} \\ \frac{1}{2} & |x| = \frac{1}{2} \\ 0 & |x| > \frac{1}{2}, \end{cases}$$

is the unitary pulse function. The capacitor voltage in each clock cycle $[iT, (i+1)T]$ is therefore fully described knowing the time constant $\tau = RC$, the initial voltage in each period $v_{C,i} = v_C(iT)$ on the capacitor and the steady-state voltage $v_{C,i}(\infty) = V_{\mathrm{DD}} b_i$, corresponding to 0V or V_{DD} depending on the value of the bit b_i of the ith clock cycle:

$$v_C(t) = v_{C,i}(\infty)\left[1 - e^{-\frac{t-iT}{\tau}}\right] + v_{C,i} e^{-\frac{t-iT}{\tau}}. \tag{2.2}$$

If we assume the capacitor voltage to be zero in the beginning of conversion, i.e.:

$$v_C(0) = v_{C,0} = 0 \tag{2.3}$$

by iterating (2.2) in each cycle $i = 0 \ldots N-1$, at the time $t = NT$ the capacitor voltage is

$$v_C(NT) = V_{\mathrm{DD}}\left(1 - e^{-\frac{T}{\tau}}\right) \sum_{i=0}^{N-1} b_i e^{-\frac{(N-1-i)T}{\tau}}.$$

Note that, choosing the clock period T in relation to the time constant τ such that[1]

$$e^{-\frac{T}{\tau}} = \frac{1}{2} \quad \Rightarrow \quad T = \tau \log 2 = T^* \tag{2.4}$$

the capacitor voltage at $t = NT$ is

$$v_C(NT^*) = \frac{V_{\mathrm{DD}}}{2^N} \sum_{i=0}^{N-1} b_i 2^i = \frac{n}{2^N} V_{\mathrm{DD}} = V_{\mathrm{DAC}}(n) \tag{2.5}$$

resulting in a linear relation between the digital code (2.1) and the converted voltage V_{DAC}, implementing therefore the functionality of a DAC.

The result in (2.5) is obtained under the assumption of null initial conditions. In practice it is not necessary to reset the capacitor voltage

[1]After the publication of the ReDAC idea [30] the authors found that a condition equivalent to (2.4) had been exploited by Claude E. Shannon in a 1948 Pulse Code Modulation (PCM) Decoder (see [78]).

at the beginning of each conversion since, even if (2.3) is not met, it is always valid that $v_{C,0} < V_{DD}$ and, being the contribution of $v_{C,0}$ damped by a factor $e^{-NT/\tau} = 2^{-N}$ at the end of conversion, its contribution to the final voltage falls always below 1 LSB of the target resolution:

$$\frac{v_{C,0}}{2^N} < \frac{V_{DD}}{2^N} = 1\,\text{LSB}.$$

Numerically simulating all the possible codes of a 5 bit ReDAC, according to (2.2), Fig. 2.3 is obtained.

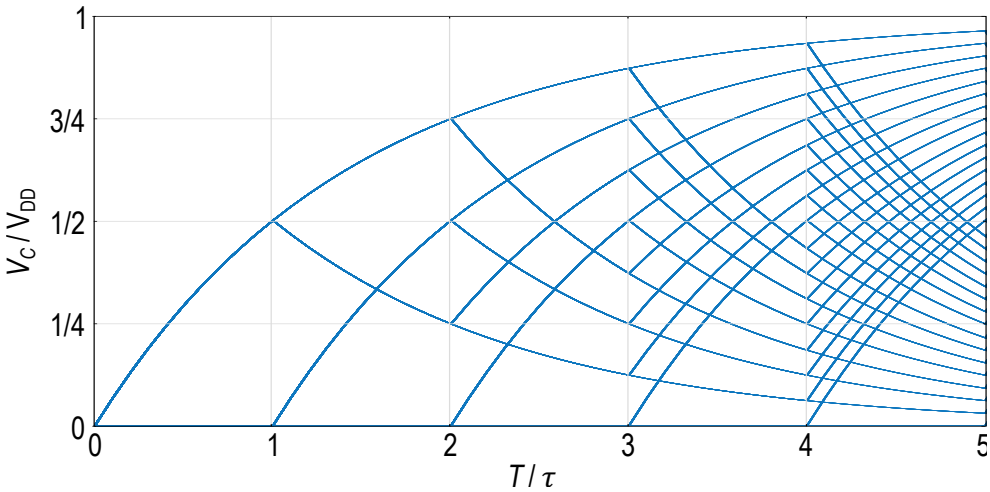


Figure 2.3: All the possible waveforms of a 5 bit ReDAC converter superimposed.

2.2 Clock and Calibration Principle

2.2.1 Clock-related Nonlinearity

It is worth noting that, according to (2.4), the ReDAC linear operation is depending solely on the ratio between T and τ so that, tuning the clock period to enforce $T = T^*$, results in a process-voltage-temperature (PVT) and mismatch insensitive architecture, highly desirable in scaled technology nodes.

Conversely, if (2.4) is not met, the error $\Delta T = T - T^*$ between the actual clock period and the ideal one translates into a ReDAC nonlinearity error which is code-dependent.

In particular, the effect of a positive (negative) clock error ΔT on the ReDAC swing, integral nonlinearity (INL), and diferential nonlinearity (DNL), is shown in Fig. 2.4(a) (Fig. 2.4(b)).

The nonlinearity error is expressed in LSB as:

$$\varepsilon(n) = V_{\mathrm{DAC}}(n)|_{T^*+\Delta T} \frac{2^N}{V_{\mathrm{DD}}} - n \tag{2.6}$$

and its expression can be expanded by Taylor series in the neighbourhood of $t = NT^*$ as

$$\begin{aligned}\varepsilon(n) &= 2\left(1 - \frac{1}{2}e^{-\frac{\Delta T}{\tau}}\right)\sum_{i=0}^{N-1} b_i 2^i e^{-\frac{(N-1-i)\Delta T}{\tau}} - n \\ &\simeq \left(1 + \frac{\Delta T}{\tau}\right)\sum_{i=0}^{N-1} b_i 2^i \left[1 - (N-1-i)\frac{\Delta T}{\tau}\right] \\ &= \frac{\Delta T}{T^*} \cdot \log 2 \cdot \left[n(2-N) + \sum_{i=0}^{N-1} 2^i i b_i\right].\end{aligned} \tag{2.7}$$

The error is maximum at half swing, in correspondence to the digital codes $2^{N-1} - 1$ and 2^{N-1}, where the INL assume the values

$$\varepsilon(2^{N-1} - 1) = \left(-2^{N-1} + N\right)\log 2 \cdot \frac{\Delta T}{T^*} \tag{2.8}$$

and

$$\varepsilon(2^{N-1}) = 2^{N-1}\log 2 \cdot \frac{\Delta T}{T^*}, \tag{2.9}$$

which translate into a maximum DNL error of

$$\delta = \mathrm{DNL}_{\mathrm{max}} = (2^N - N)\log 2 \cdot \frac{\Delta T}{T^*} \approx 2^N \log 2 \cdot \frac{\Delta T}{T^*} \tag{2.10}$$

which highlights the monotonic relation between δ and ΔT. The value of δ is also related to the difference ΔV_{DAC} between the two half-swing codes:

$$\Delta V_{\mathrm{DAC}} = V_{\mathrm{DAC}}(2^{N-1}) - V_{\mathrm{DAC}}(2^{N-1} - 1) \tag{2.11}$$

expressed in LSB as

$$\Delta V_{\mathrm{DAC}} = 1\mathrm{LSB} \cdot \left(1 + 2^N \log 2 \cdot \frac{\Delta T}{T^*}\right) = (1 + \delta)\mathrm{LSB} \tag{2.12}$$

2.2.2 Calibration Principle

Equation (2.12) can be exploited to search the optimal clock period to get linear ReDAC operation by detecting the sign of ΔV_{DAC} and increasing

(decreasing) the clock period if the sign is negative (positive), according to the flowchart in Fig. 2.5 until condition

$$\Delta V_{\mathrm{DAC}} = 0 \tag{2.13}$$

is reached.

Different hardware calibrations can be deployed accordingly, as reported in ReDAC architectures presented in the following chapters.

Based on (2.12) and (2.13) the calibration completion corresponds to

$$\Delta V_{\mathrm{DAC}} = 0 \rightarrow \delta = -1\mathrm{LSB} \tag{2.14}$$

i.e. a maximum DNL error of 1 LSB on N bits on all codes $n \in [0,2^N - 1]$. If a residual error of less than 1 LSB is required, (2.13) can be enforced on $N + E$ bits, resulting in $2^{N-E}\,LSB$ maximum DNL, and $\delta \approx 0$.

From (2.7), it can be observed that the calibration condition could be enforced between any couple of progressive digital input codes 2^{N-I-1}, $2^{N-I-1} - 1$, which mean on

$$\begin{aligned} \Delta V_{DAC,I} &= V_{DAC}(2^{N-I-1}) - V_{DAC}(2^{N-I-1} - 1) \\ &= 1\mathrm{LSB} \cdot \left(1 + 2^{N-I} \log 2 \cdot \frac{\Delta T}{T^*}\right) \end{aligned} \tag{2.15}$$

by imposing $\Delta V_{\mathrm{DAC},I} = 0$ for any $I \in [0, N-1]$. In practice, $I = 0$ is the optimal calibration point since, for higher I values, the residual error is obtained with less accuracy due to reduced sensitivity between $\Delta V_{\mathrm{DAC},I}$ and ΔT decreasing exponentially with I.

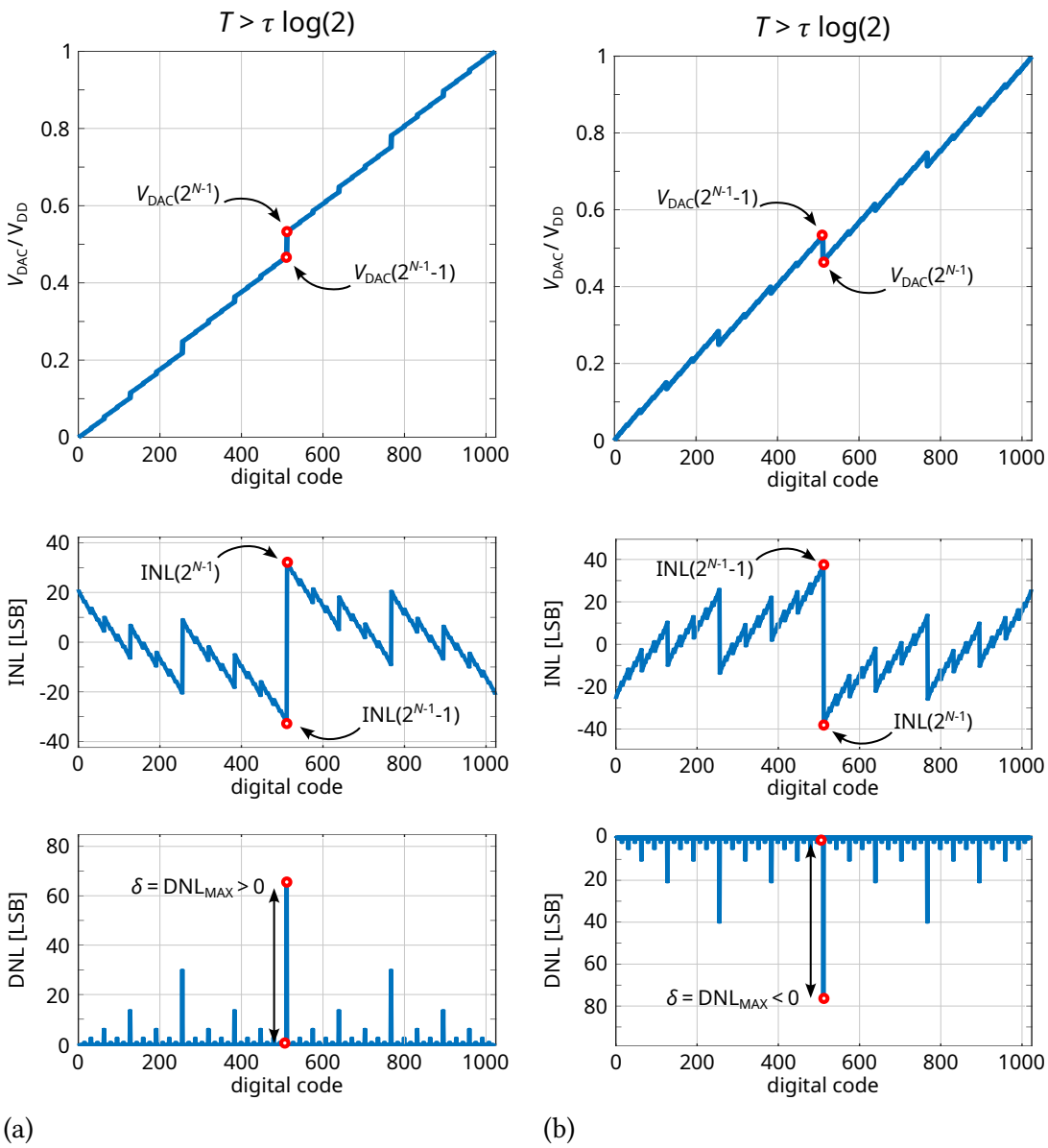


Figure 2.4: Effect on ReDAC swing, INL, and DNL in presence of a positive (a) and negative (b) error on the clock period.

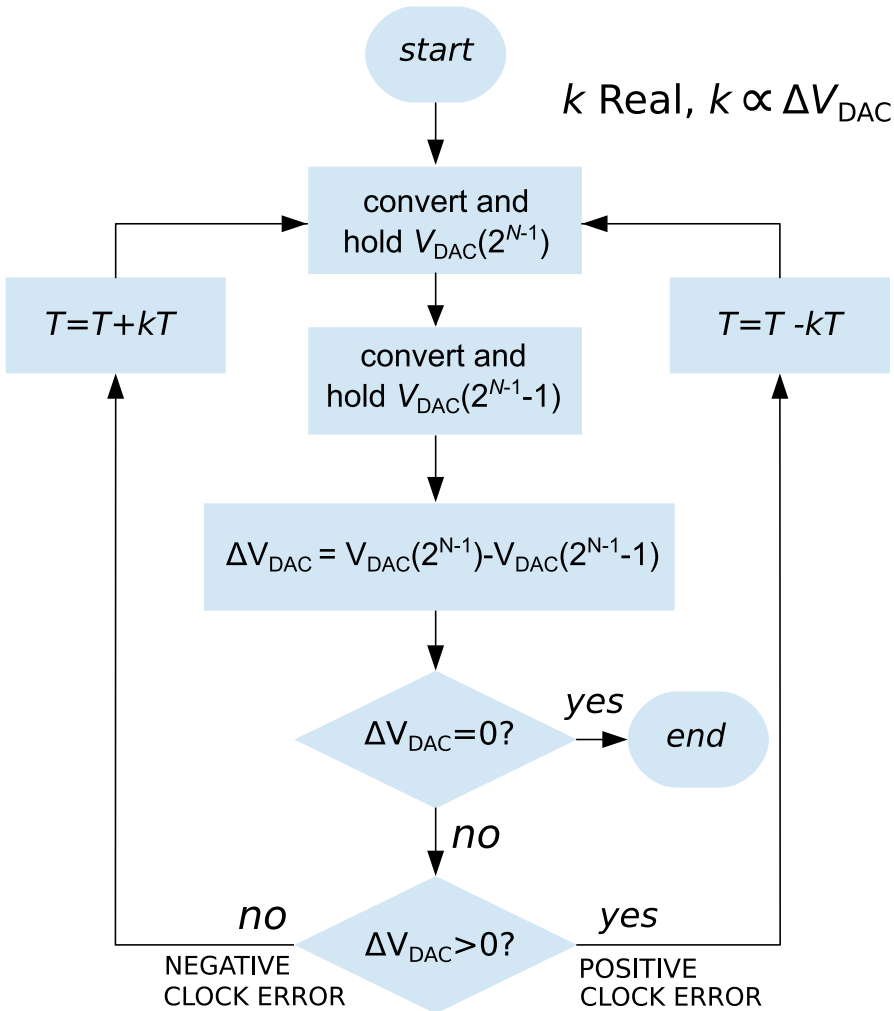


Figure 2.5: Clock-tuning calibration principle.

2.3 ReDAC Design, Tradeoffs, and Nonidealities

Different non-idealities affect the ReDAC operation in practical hardware implementations: the finite resolution achievable with the clock tuning, non-zero transition times of the digital pulses, random clock jitter σ_T, supply noise, nonzero output resistance and nonlinear loading of the three-state buffer, clock feedthrough, leakage impinging on the output capacitor, and the RC network parasitics. All these factors may result in additional noise or nonlinearities even when calibration condition (2.4) is met.

2.3.1 Capacitor Design based on the Thermal Noise Limit

Being ReDAC accuracy not dependent on matching, the capacitor C can be sized close to the $\kappa T/C$ thermal noise limit, differently from what is commonly required in weighted capacitors DACs, as introduced in Sec. 1.3.2. Given the thermal noise power

$$\overline{v_{nC}^2} = \frac{\kappa T}{C} \tag{2.16}$$

its equivalent rms voltage noise must be less than a fraction of LSB:

$$\gamma\sqrt{\frac{\kappa T}{C}} < \frac{V_{\mathrm{DD}}}{2^{N+\theta}} \tag{2.17}$$

where γ and θ are chosen depending on how many noise standard deviations are considered and the amount of LSB fraction allocated to the thermal noise. Considering three standard deviations and half LSB ($\gamma = 3$, $\theta = 1$) the minimum capacitance is

$$C_{\mathrm{min}} = 9 \cdot 2^{2N+2} \cdot \frac{\kappa T}{V_{\mathrm{DD}}^2}. \tag{2.18}$$

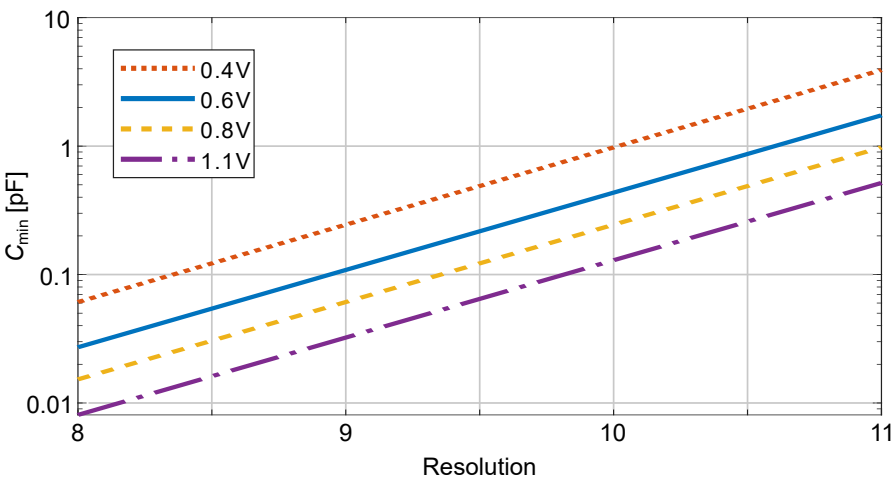


Figure 2.6: Minimum ReDAC capacitance, as per thermal noise constraint in (2.18), for different supplies.

2.3.2 General ReDAC Design

Being the ReDAC accuracy dependent on the clock period T, the transition times t_{tr} of the three-state buffer must be a negligible portion of T, which

means

$$\frac{t_{\text{tr}}}{T} < \frac{1}{2^{N+1}} \quad \rightarrow \quad T > 2^{N+1} t_{\text{tr}} \tag{2.19}$$

requiring proper sizing of the threestate buffer output transistors and limiting, in practice, the minimum conversion time:

$$T_{\text{conv}} > (N + \beta)T = (N + \beta)2^{N+1} t_{\text{tr}} \tag{2.20}$$

where βT is the duration of the hold phase at the end of conversion ($\beta \geq 1$). Considering $N = 10$ bit resolution, (2.20) is compatible with sample rates in the order of MS/s for integrated designs (t_{tr} about tens of picoseconds) and kS/s for discrete components designs (t_{tr} in the nanoseconds range).

Further limitations to the ReDAC linearity arise from the resolution ΔT_{res} at which the calibration condition (2.4) is enforced. If the period T is obtained by clock division of a higher-frequency clock having period $T_{\text{clk}} = \Delta T_{\text{res}}$ then, from (2.10), it must be:

$$\frac{T_{\text{clk}}}{T} \leq \frac{1}{2^N \log 2}. \tag{2.21}$$

Condition (2.21) can be relaxed in integrated implementations by using a voltage controlled oscillator (VCO) or a digitally controlled oscillator (DCO) or, in FPGA implementations, with fractional-N PLLs.

Apart from calibration resolution, random Gaussian clock jitter affects the converted value accuracy and, based on (2.9) and [79], results into code-depending error normally distributed and having standard deviation (in LSB) of

$$\sigma_\varepsilon(n) = \frac{\sigma_T}{T} \cdot \log 2 \cdot \left[n(2 - N) + \sum_{i=0}^{N-1} 2^i i b_i \right]. \tag{2.22}$$

which is maximum for digital code $n = 2^{N-1}$ and corresponds to a maximum rms INL of

$$\text{INL}_{\text{rms}} = 2^{N-1} \log 2 \cdot \frac{\sigma_T}{T}. \tag{2.23}$$

If the clock is referenced to crystal oscillators, σ_T of some picoseconds is achievable with clocks of several MHz and resolutions beyond 13 bits.

If T is obtained, as previously mentioned, by counting M periods of a higher-frequency reference having period T_{clk} ($T = M \cdot T_{\text{clk}}$), even better resolutions can be achieved due to the reduced jitter

$$\frac{\sigma_T}{T} = \frac{\sigma_{T_{\text{clk}}}}{T_{\text{clk}}} \frac{1}{\sqrt{M}}. \tag{2.24}$$

In the absence of a crystal reference clock, 10 bits ReDAC converters up to the MS/s sample rate are nonetheless achievable.

Due to the absence of matching requirements, C can be dimensioned close to the minimum dictated by thermal noise according to (2.18), which translates in less than 1 pF for 10 bit resolution and related power and area saving.

Once T and C are fixed, the resistance R can be finally sized to meet (2.4):

$$R = \frac{\tau}{C} = \frac{T}{C \log 2}. \tag{2.25}$$

From (2.25) it results that the resistance is in the order of 100 kΩ in integrated ReDAC for a 10 bit converter, and in the MΩ range for discrete designs under the same resolution.

The output buffer resistance and nonlinear loading is easily be made negligible with this value of R in both integrated and discrete ReDAC implementations by choosing the three-state output resistance R_{buff} in the tens-of-Ohms range. Nevertheless, the effect of the distributed parasitic capacitance of R can easily be large enough not to be negligible, impairing the first-order response of the RC network.

2.3.3 RC Network Parasitics

To evaluate the effect of the ReDAC parasitics in its output stage the resistor R and its distributed capacitance C_{par} towards the substrate are considered, along with the non null output resistance of the three-state buffer.

In practice, the RC parasitics dominate over the buffer nonlinear loading, which is validated by simulations ona 10 bit, 2 MS/s ReDAC in 40 nm, simulated at transistor level with an ideal RC network, and all other parasitics (see Fig. 2.7(a)) and with realistic RC network and ideal buffer (see Fig. 2.7(b)). The two figures clearly show how the effect of the buffer nonidealities are negligible with respect to the RC parasitics; a strategy to suppress the latter is then investigated.

The ReDAC is modelled by a resistance R loaded by the capacitor C driven by a voltage source having as series resistance R_{buff}, i.e. the best linear approximation of the output buffer impedance, as in Fig. 2.8(a) . The transfer function of the RC network results to be no more a fist order one but it can be expressed by the distributed-model transfer function

$$H(s) = \frac{1}{(1 + sCR_{\text{buff}}) \cosh \gamma + \left(\frac{R_{\text{buff}}}{Z_0} + sCZ_0 \right) \sinh \gamma} \tag{2.26}$$

having $\gamma = \sqrt{RC_{\text{par}}s}$ and $Z_0 = \sqrt{\frac{R}{sC}}$.

The transfer function (2.26) is compactly approximated by the low-pass transfer function of Qth order:

$$H(s) = \prod_{k=0}^{Q} \frac{1}{s\tau_k + 1} = \sum_{k=0}^{Q} \frac{a_k}{s\tau_k + 1} \tag{2.27}$$

where

$$a_k = \prod_{h \neq k} \frac{1}{1 - \frac{\tau_k}{\tau_h}} \tag{2.28}$$

are the residues of the singularities in $H(s)$.

By Taylor series expansion of the denominator of (2.26), the dominant time constant τ_0 can be derived by evaluating the first order moment of the transfer function, as in [80]:

$$\tau_0 = (R + R_{\text{buff}})\left(C + \frac{C_{\text{par}}}{2}\right) + \frac{1}{2}C_{\text{par}}R_{\text{buff}} \tag{2.29}$$

while the first non-dominant time constant is

$$\tau_1 = \frac{1}{6}(3R_{\text{buff}} + R)\,C_{\text{par}} \simeq \frac{1}{6}\frac{C_{\text{par}}}{C}\tau_0 \tag{2.30}$$

considering valid the approximation $R_{\text{buff}} \ll R$ and $C_{\text{par}} \ll C$.

The impulse response related to the transfer function (2.27) is normalised with respect to the dominant time constant residue and expressed as

$$\begin{aligned} h(t) &= \mathrm{e}^{-\frac{t}{\tau_0}} + \sum_{k=1}^{Q} \frac{a_k}{a_0}\mathrm{e}^{-\frac{t}{\tau_k}} \\ &= h_0(t) + h_\varepsilon(t) \end{aligned} \tag{2.31}$$

where $h_0(t)$ is equivalent to the impulse response of an ideal RC network as required by a ReDAC, being $\tau = \tau_0$, while $h_\varepsilon(t)$ can be regarded as an error term contribution related to the parasitic resistor capacitance.

The ReDAC capacitor voltage can therefore be expressed as the convolution product of the buffer output stream of bits (2.2) with the multiple time constant impulse response h in (2.31) as:

$$v_{\text{C}}(t) = (v_{\text{buff}} * h)(t) = \underbrace{(v_{\text{buff}} * h_0)(t)}_{v_{\text{C,id}}(t)} + \underbrace{(v_{\text{buff}} * h_\varepsilon)(t)}_{v_{\text{C,}}(t)}. \tag{2.32}$$

The term $v_{\mathrm{C,id}}(t)$ is analogous to (2.2) and it is the capacitor voltage during conversion of a ReDAC having an ideal first-order RC network of time constant $\tau = \tau_0$; $v_{\mathrm{C,}}(t)$ is the error contribution due to the parasitic high-order terms in the impulse response, as depicted in Fig. 2.8(b) (red dashed curve), resulting in a ReDAC nonlinearity error expressed in LSBs as

$$\varepsilon_{\mathrm{par}}(n) = v_{\mathrm{C},\varepsilon}(NT)\frac{2^N}{V_{\mathrm{DD}}}. \tag{2.33}$$

The multiple-time-constants model is verified by considering a 10 bit ReDAC in 40 nm CMOS technology having components of nominal value $R = 144\,\mathrm{k\Omega}$ and $C = 444\,\mathrm{fF}$ (as considered in [81]) and their parasitics $C_{\mathrm{R}} = 36\,\mathrm{fF}$, $R_{\mathrm{buff}} = 4.2\mathrm{k\Omega}$. Limiting the expansion to the first two time constants ($Q = 2$), then

$$\tau_0 = 68.5\,\mathrm{ns}, \quad \tau_1 = 0.94\,\mathrm{ns}, \quad \frac{a_1}{a_0} = 0.014 \tag{2.34}$$

and the worst half-swing DNL ReDAC error δ_0 related only to the RC network parasitics, and fixing the clock period to $\tau_0 \log 2$ to meet (2.4) for $\tau = \tau_0$, is:

$$\begin{aligned} \delta_0 &= \varepsilon_{\mathrm{par}}(2^{N-1}) - \varepsilon_{\mathrm{par}}(2^{N-1} - 1) \\ &\simeq -2^N\frac{a_1}{a_0} - 1 \simeq -15\,\mathrm{LSB} \end{aligned} \tag{2.35}$$

which is close to the ReDAC transistor-level simulated prediction of $-16.33\,LSB$ worst-case DNL shown in Fig. , validating the analytical model, which is also confirmed by the simulated results of Fig. , in which a comparison between the transistor-level simulated result for maximum δ_0 and the analytically predicted by (2.35) is performed for the same nominal R and C at different normalised resistor widths $k_{\mathrm{W}} = W/W_{\mathrm{min}}$, resulting in different parasitic capacitances towards the substrate.

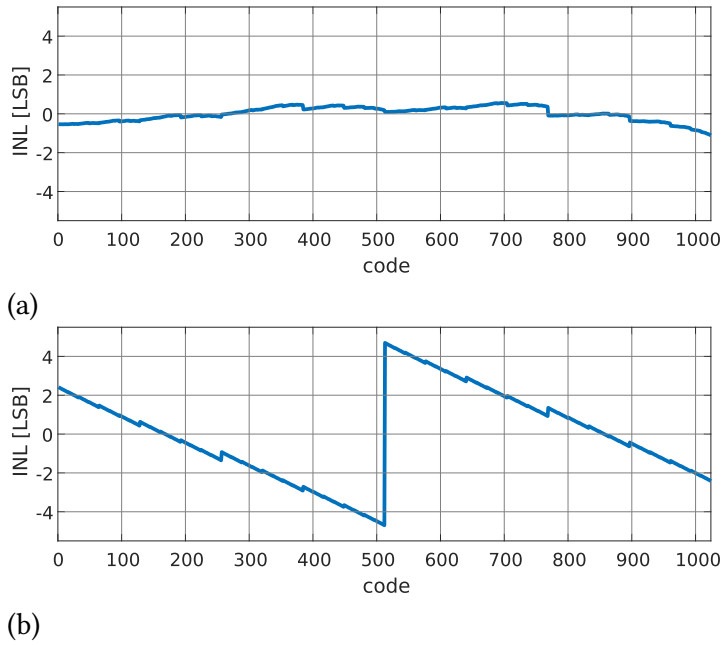


Figure 2.7: Simulated nonlinearity for a calibrated 10 bit, 2 MS/s ReDAC in 40 nm CMOS having $R = 144\,\mathrm{k}$ and $C = 444\,\mathrm{fF}$ for: (a) ideal RC network driven by transistor-level model of the buffer and (b) a realistic model of the RC driven by an ideal voltage source. The larger INL in (b) reveals that the main contribution to nonlinearity are the RC-network parasitics.

2.3.4 Parasitics Suppression Strategy

Once a model is derived for the ReDAC parasitics as in Section 2.3.3, a strategy to suppress the dominant parasitics effect on nonlinearity is devised.

Considering (2.32), if the ReDAC output buffer is not put in high impedance at $t = NT$ but driven low for $t > NT$, the first-order term of the ReDAC output voltage for $t > NT$ is given by the convolution

$$\begin{aligned}(v_{\mathrm{buff}} * h_0)(NT + t) &= \\ &= \int_{-\infty}^{\infty} v_{\mathrm{buff}}(\lambda) e^{-\frac{NT+t-\lambda}{\tau_0}} d\lambda \\ &= e^{-\frac{t}{\tau_0}} \int_{-\infty}^{\infty} v_{\mathrm{buff}}(\lambda) e^{-\frac{NT-\lambda}{\tau_0}} d\lambda \\ &= v_{\mathrm{C,id}} \cdot e^{-\frac{t}{\tau_0}} \end{aligned} \tag{2.36}$$

while the contribution of the higher-order error terms is

$$\begin{aligned} v_{\mathrm{C},\varepsilon}(NT+t) &= (v_{\mathrm{buff}} * h_\varepsilon)(NT+t) \\ &= \int_{-\infty}^{\infty} v_{\mathrm{buff}}(\lambda) \sum_{k=1}^{Q} \frac{a_k}{a_0} e^{-\frac{NT+t-\lambda}{\tau_k}} \mathrm{d}\lambda \\ &= \sum_{k=1}^{Q} e^{-\frac{t}{\tau_k}} \underbrace{\frac{a_k}{a_0} \int_{-\infty}^{\infty} v_{\mathrm{buff}}(\lambda) e^{\frac{-NT+\lambda}{\tau_k}} \mathrm{d}\lambda}_{v_{C,\varepsilon,k}} \\ &= \sum_{k=1}^{Q} v_{\mathrm{C},\varepsilon,k} \cdot \mathrm{e}^{-\frac{t}{\tau_k}} \end{aligned} \tag{2.37}$$

i.e. the sum of the voltage errors $v_{C,\varepsilon,k}$ associated to the undesired time constants τ_k are damped exponentially in time by e^{-t/τ_k}.

Based on (2.36) and (2.37), considering the magnitude of the first non-dominant time constant τ_1 in (2.30) being in practice orders of magnitude smaller than τ_0, if the threestate buffer is driven low at $t = NT$ up to $t = NT + T_{\mathrm{del}}$, and having

$$3\tau_1 \simeq T_{\mathrm{del}} \ll \tau_0, \tag{2.38}$$

it ensues

$$\begin{aligned} v_{\mathrm{C}}(NT+T_{\mathrm{del}}) &= v_{\mathrm{C,id}} \cdot e^{-\frac{T_{\mathrm{del}}}{\tau_0}} + \sum_{k=1}^{Q} v_{\mathrm{C},\varepsilon,k} \cdot e^{-\frac{T_{\mathrm{del}}}{\tau_k}} \\ &\simeq v_{\mathrm{C,id}} \cdot e^{-\frac{T_{\mathrm{del}}}{\tau_0}} \end{aligned} \tag{2.39}$$

where the capacitor voltage is practically equal to the ideal one attenuated by a small factor

$$e^{-\frac{T_{\mathrm{del}}}{\tau_0}} \simeq e^{-\frac{3\tau_1}{\tau_0}} \simeq 1,$$

and the errors are damped by a factor which is at least $\mathrm{e}^{-3} \simeq 0.05$, becoming negligible. The effectiveness of this strategy is validated by transistor level simulations as reported in Fig. 2.11, where the maximum DNL error δ decays in agreement with the predicted behaviour in (2.39) with a negligible swing attenuation.

Based on numerical values in (2.34), choosing $T_{\mathrm{del}} = 3\tau_1 = 2.82\,\mathrm{ns}$, the parasitics contribution is attenuated by 0.05 times its original value, i.e. from 16 LSB to 0.7 LSB on 10 bit ($7.3 \cdot 10^{-4}$ of the ReDAC swing), while the ideal component is attenuated to just 0.959 its original value.

Moreover, it is worth noting that, as long as $\tau_0 \gg \tau_1$, there is no need to precisely control T_{del}: a 10% larger T_{del} translates into an attenuation of the parasitics error to 0.04 (opposed to 0.05) and in a 0.956 (instead of a 0.959) damping of the nominal signal, which does not affect ReDAC linearity and results in a gain error of just 0.03 dB (maximum absolute error at full swing of 4 LSBs).

The error suppression strategy is therefore robust to process-related and temperature-related variations of parasitics affecting the RC network, as validated by the results in Fig. 2.12(a), and Fig. 2.12(b), showing the simulated distribution of the ReDAC swing attenuation related to process and temperature variations respectively for a minimum width Hi-res polysilicon resistor and a MiM capacitor.

The parasitics error suppression strategy presented herein, is easily implemented in both integrated and FPGA implementations of the ReDAC by driving low the output buffer for a fraction T_{del} of the clock period before it is put in high impedance, in normal operation as well as calibration.

The minimum value of T_{del} can be derived by imposing the parasitics error to be less than half LSB on the target resolution enforcing

$$\delta_0 \cdot \mathrm{e}^{-\frac{T_{\text{del}}}{\tau_1}} \leq \frac{1}{2}\mathrm{e}^{-\frac{T_{\text{del}}}{\tau_0}}$$

which results in

$$T_{\text{del}} > \frac{\tau_0 \tau_1}{\tau_0 - \tau_1} \log(2\delta_0) \tag{2.40}$$

corresponding to $T_{\text{del}} > T_{\text{del,min}} = 3.13\,\text{ns}$ for the 40 nm ReDAC design considered so far. The ReDAC nonlinearity obtained for such $T_{\text{del}} = T_{\text{del,min}}$ by simulations and by the model (2.39) is compared in Fig. 2.13 revealing the strength of the proposed method.

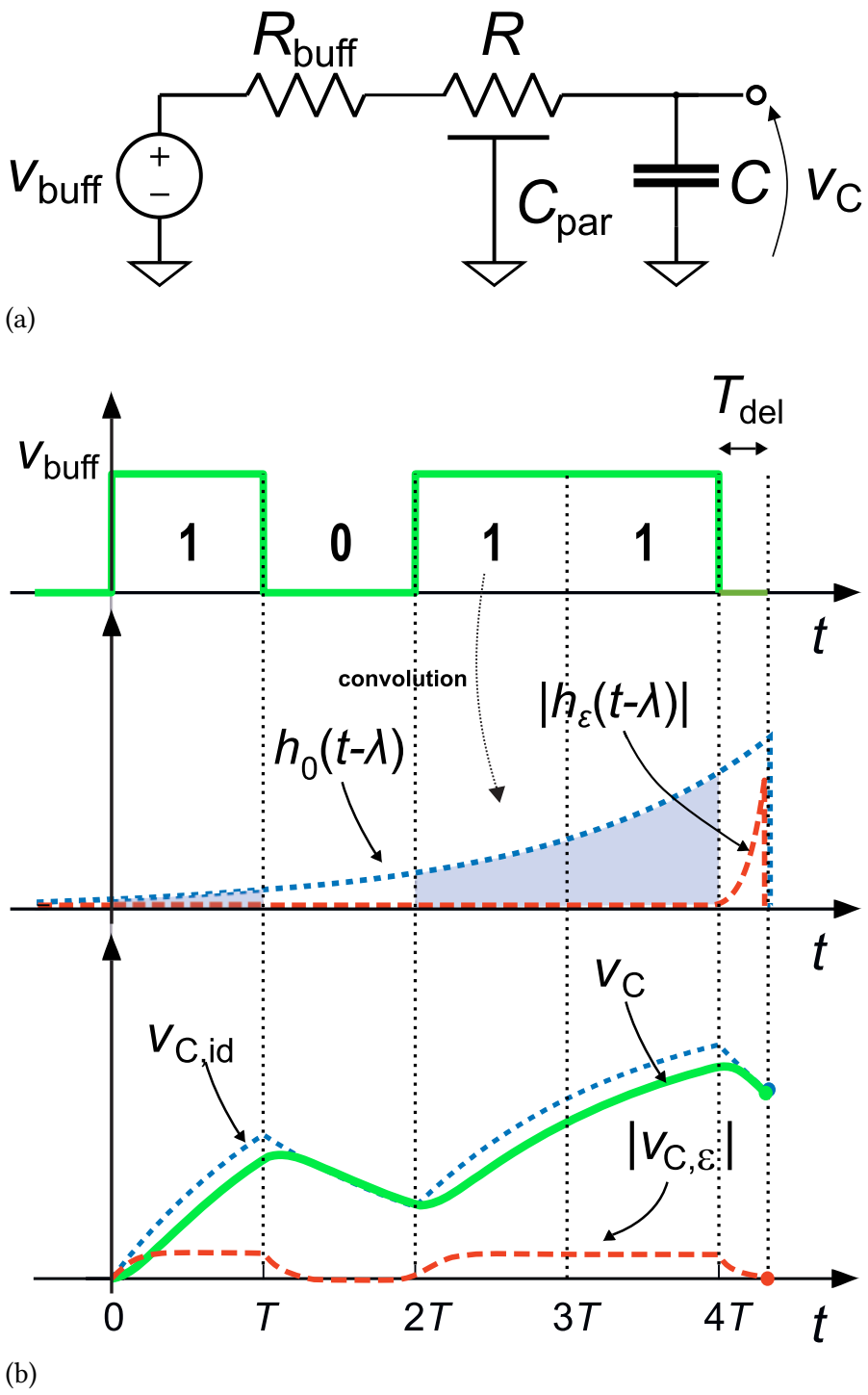


Figure 2.8: RC network distributed model driven by an ideal voltage source, corresponding to the linearised Thevenin equivalent of the three-state buffer (a). Convolution of the digital word 1101 with the first and second order term of the impulse response expansion (b).

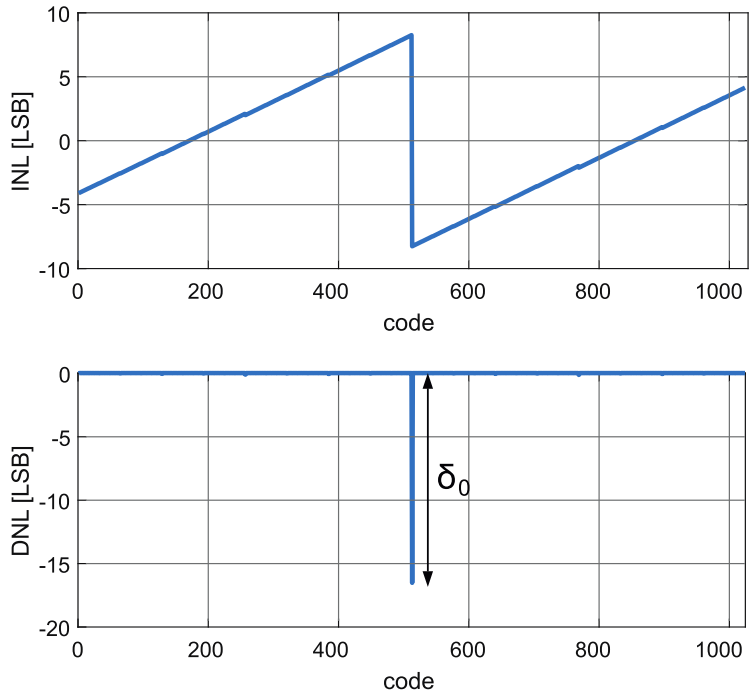


Figure 2.9: INL and DNL related to the RC network parasitics as simulated in a 40 nm ReDAC having High-res poly resistor ($R = 144\,\mathrm{k}$) with total parasitic capacitance $C_{\mathrm{par}} = 36\,\mathrm{fF}$ and a MiM capacitor $C = 444\,\mathrm{fF}$. The operating condition (2.4) is satisfied for the dominant time constant i.e. $T = \tau_0 \log 2$.

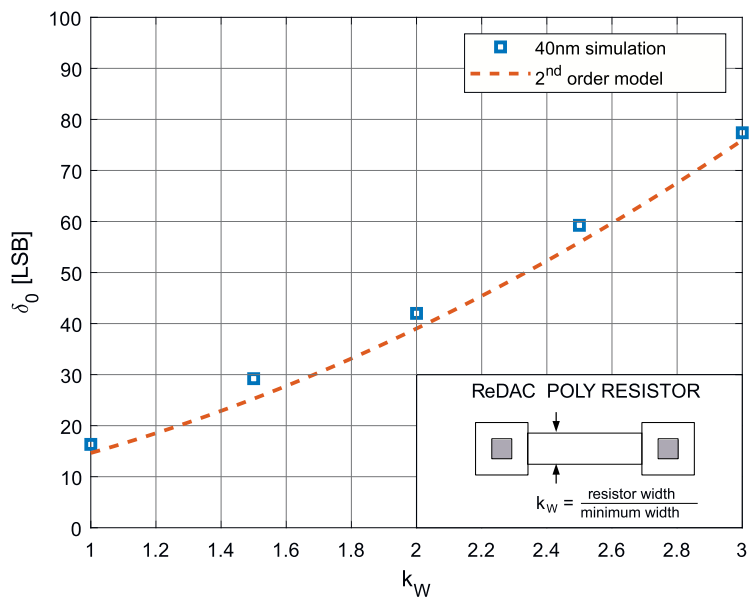


Figure 2.10: Maximum DNL δ_0 evaluated by simulations under the same conditions as in Fig.2.9 for different resistor widths parametrised with respect to the minimum technology width. The model-based results are in accordance with simulations.

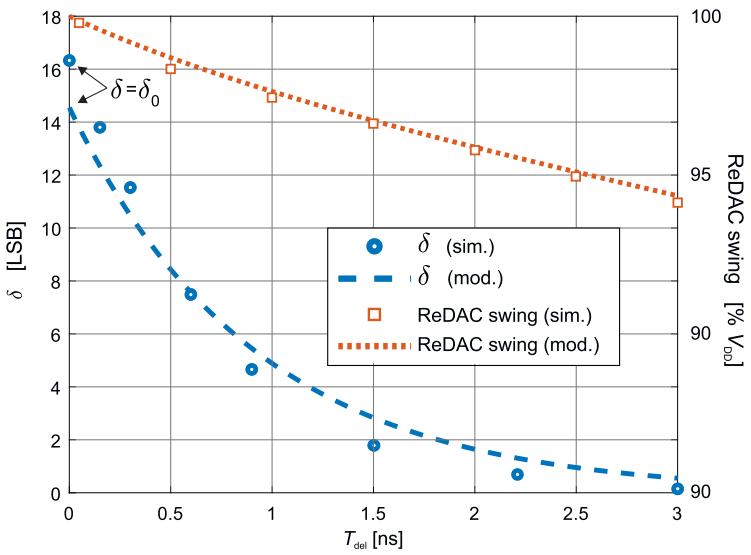


Figure 2.11: Comparison between the analytically-predicted and the simulated ReDAC swing (maximum DNL) attenuation with T_{del}.

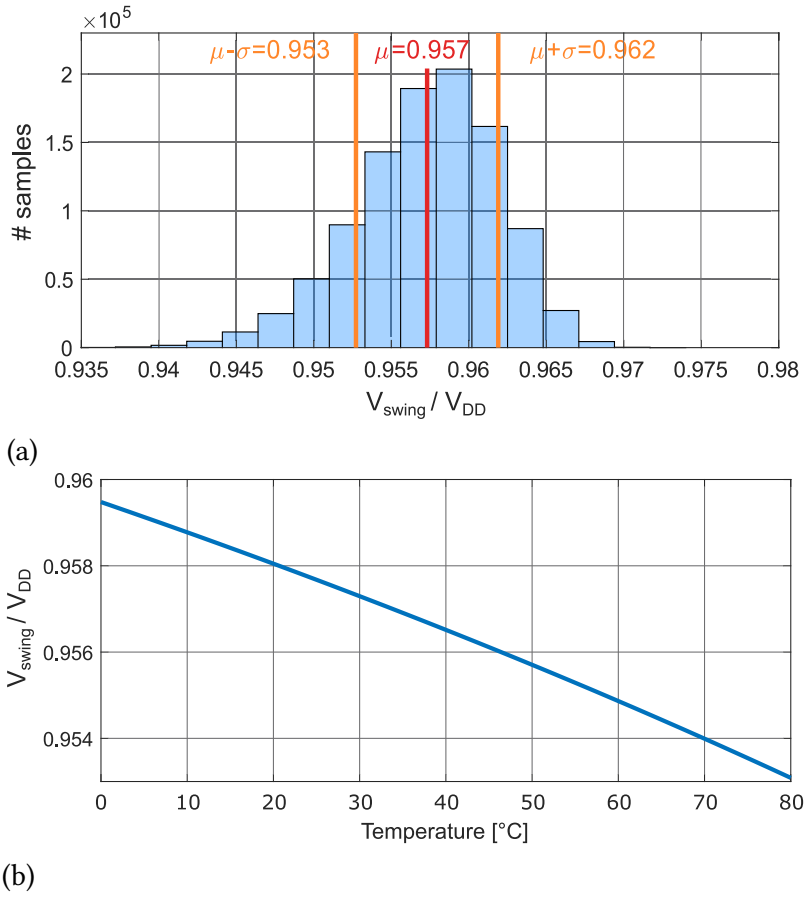


Figure 2.12: ReDAC swing attenuation simulated variations with process (a) and temperature (b).

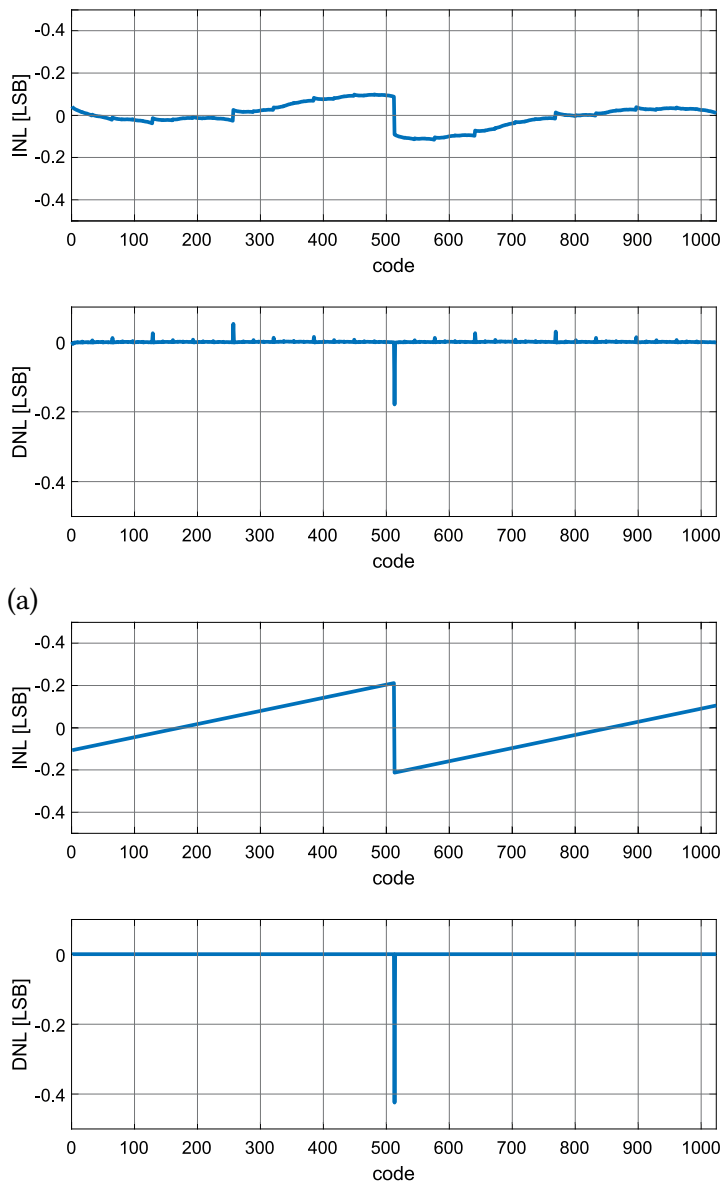


Figure 2.13: INL and DNL obtained by applying the minimum predicted T_{del} to get nonlinearity below half LSB, accoding to simulations (a) and the proposed multiple time constants model (b).

2.3.5 Energy per Conversion

The ReDAC energy per conversion E is depending on the digital input n and can be evaluated from (2.2) considering the sum of the energies required to charge the capacitor bits b_i are equal to one.

The energy per conversion normalised with respect to CV_{DD}^2 is

$$E(n) = CV_{\mathrm{DD}}^2 \sum_{i=0}^{N-1} b_i \sum_{j=0}^{i} 2^{j-i}(b_j - b_{j-1}) \qquad b_{-1} \triangleq 0 \tag{2.41}$$

and it is plotted for a $N = 10$ bit converter in Fig. 2.14, in which the average energy is $1.5CV_{\mathrm{DD}}^2$.

Evaluating the average energy per conversion of the ReDAC as a function of resolution, it can conveniently be numerically fit by the linear expression

$$\overline{E} \simeq CV_{\mathrm{DD}}^2(0.13N + 0.2). \tag{2.42}$$

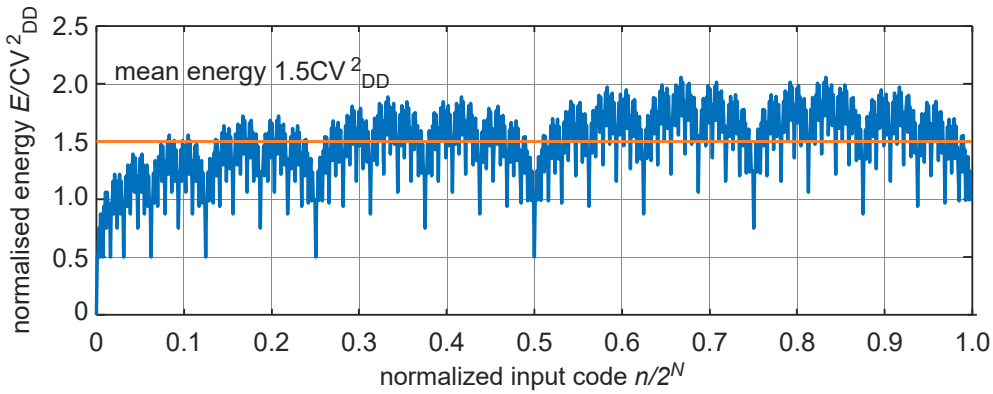


Figure 2.14: Energy per conversion, normalised with respect to CV_{DD}^2, versus digital code for $N = 10$ bits.

2.3.6 Comparison to Weighted Capacitors DACs

Table 2.1 shows a comparison of the ReDAC to conventional binary weighted capacitors (CBW) and binary weighted capacitors DAC with attenuation capacitor (BWA) [30], [79] as related to parameters already presented in this chapter for the ReDAC: minimum total capacitance, INL, DNL, and mean conversion energy.

The ReDAC is based on a single capacitor and its linearity is not constrained by the capacitor matching variation (standard deviation σ_0), being related to the residual error $\Delta T/T$ after the clock calibration.

At the same time, the total ReDAC capacitance is not limited by the minimum unit capacitor C_0 dictated by technology or matching constraint, and can therefore be close to the thermal noise limit C_{TH} required by Nbit resolution.

Given the total capacitance C, the ReDAC energy per conversion is $(0.13N+0.2)CV_{\mathrm{DD}}^2$, compared to $1/6CV_{\mathrm{DD}}^2$ of the weighted capacitor DACs, making the ReDAC energy easily smaller due to the reduced total capacitance.

Table 2.1: Comparison of ReDAC with binary-weighted capacitor DACs.

DAC	CBW	BWA[a]	Relaxation
# of capacitors	N	$N+1$	1
minimum total cap. C	$\max\{2^N C_0, C_{\mathrm{TH}}\}$	$\max\left\{2^{\frac{N}{2}+1} C_0, C_{\mathrm{TH}}\right\}$	$C_{\mathrm{TH}} \simeq 9 \cdot 2^{2N+2}\kappa T/V_{\mathrm{DD}}^2$ [b]
INL max	$3 \cdot 2^{\frac{N}{2}-1}\left(\frac{\sigma_{C_0}}{C_0}\right)$	$3 \cdot 2^{\frac{3N}{4}-1}\left(\frac{\sigma_{C_0}}{C_0}\right)$	$2^{N-1}\log 2 \cdot \frac{\Delta T}{T}$
DNL max	$3 \cdot 2^{\frac{N}{2}}\left(\frac{\sigma_{C_0}}{C_0}\right)$	$3 \cdot 2^{\frac{3N}{4}}\left(\frac{\sigma_{C_0}}{C_0}\right)$	$2^{N}\log 2 \cdot \frac{\Delta T}{T}$
mean energy	$\frac{1}{6}CV_{\mathrm{DD}}^2$	$\frac{1}{6}CV_{\mathrm{DD}}^2$ [c]	$(0.13N+0.2)CV_{\mathrm{DD}}^2$ [d]
floating caps.	no	yes	no

[a]With two equal sub-arrays ($N/2$ capacitors each).
[b]Thermal noise limited value.
[c]Under monotonic switching, being C the total capacitance of the DAC.
[d]Based on linear interpolation of simulation results, valid for $N > 2$.

Chapter 3

40nm CMOS ReDAC with VCO-based Foreground Calibration

The present chapter presents the design of a first self-calibrated ReDAC architecture. The calibration is based on VCO-based clock tuning and VCO-based A/D conversion, to provide a matching insensitive, reference-free ReDAC linearity enforcement. The converter design in 40 CMOS is presented, the calibration procedure developed and performance evaluated by simulations, validating the effectiveness of the proposed approach.

3.1 Motivation

As introduced in Chapter 1, the ReDAC idea rises in the context of digital-intensive bitstream data converters. Based on considerations unfolded in Chapter 2, the ReDAC can be designed to achieve ultra-compact area and low power operation, proposed as an alternative to weighted capacitors D/A converters [82], [83], sigma-delta ($\Sigma\Delta$) [84], and pulse-width modulation DACs [31], [85], [86], provided that the characteristic relation $T^* = \tau \log 2$ ((2.4) in Chapter 2) between the clock period and the RC time

constant is enforced.

Once published the original ReDAC concept [30], [81], the need for automatic clock calibration arose, and the first digital automatic calibration was proposed [87] and discussed in the present chapter.

While the possibility to digitally tune the ReDAC clock by division of an high-frequency clock was initially suggested [30], in integrated implementations it is more convenient to operate the ReDAC at the minimum required clock to keep power dissipation at the minimum required, devising a reference-free, supply independent calibration compatible to low-cost CMOS integration and digital design flow.

3.2 VCO-based calibration

The ReDAC linearity does not rely on unitary elements matching like current steering, weighted resistor and weighted capacitor DACs [82]–[84] and it is related on the sole process-depending ratio T/τ, which feature enables to achieve linearity on the full swing by single-point calibration, which means imposing the correct output voltage for a single digital code.

The proposed calibration enforces the relation (2.4) between the time constant $\tau = RC$ and the clock period T based on the proportionality between the error on clock period $\Delta T = T - T^*$ and the difference in output voltage between the codes $2^{N-1} - 1$ and 2^{N-1} as recalled from (2.12) of Chapter 2:

$$\Delta V_{\mathrm{DAC}} = 1\,\mathrm{LSB} \cdot \left(1 + 2^N \log 2 \frac{\Delta T}{T}\right)$$

and represented in Fig. 3.1. Enforcing $\Delta V_{\mathrm{DAC}} = 0$ results in a maximum error of 1 LSB across the whole swing.

3.2.1 Self Calibration Architecture

The architecture in Fig. 3.2 is proposed to enforce the calibration condition (2.4) on N bits. The voltage controlled oscillator VCO1 is providing the reference clock for the architecture.

The VCO1 input is connected to the capacitor $C_{\mathrm{VCO},1}$, storing the control voltage $V_{\mathrm{VCO},1}$, which value can be updated by connecting it to the ReDAC output capacitor C trough a pass gate PG1. A different VCO named VCO2, which is analogously controlled by the voltage $V_{\mathrm{VCO},2}$ across its input capacitor $C_{\mathrm{VCO},2}$ can also be updated by the ReDAC output trough a pass gate PG2. Using binary counter the second oscillator VCO2 is used as a VCO-based analog-to-digital converter [88], [89].

The architecture of the two VCOs is shown in Fig. 3.3 adopted broadly in latest low power relaxation oscillators [90]–[92], which period is

$$T = 2\frac{CV_{\mathrm{TRIP}}}{I}$$

being C the capacitance at the input of the Set-Reset latch in Fig. 3.3, V_{TRIP} the threshold of the logic gates, and I the current in transistor MP, modulated by its gate voltage which coincides with the input of the VCO. The VCO operates according to the timing in Fig. 3.4.

The calibration is controlled by a digital state machine, implementing a negative feedback to reach condition (2.4), exposed in what follows.

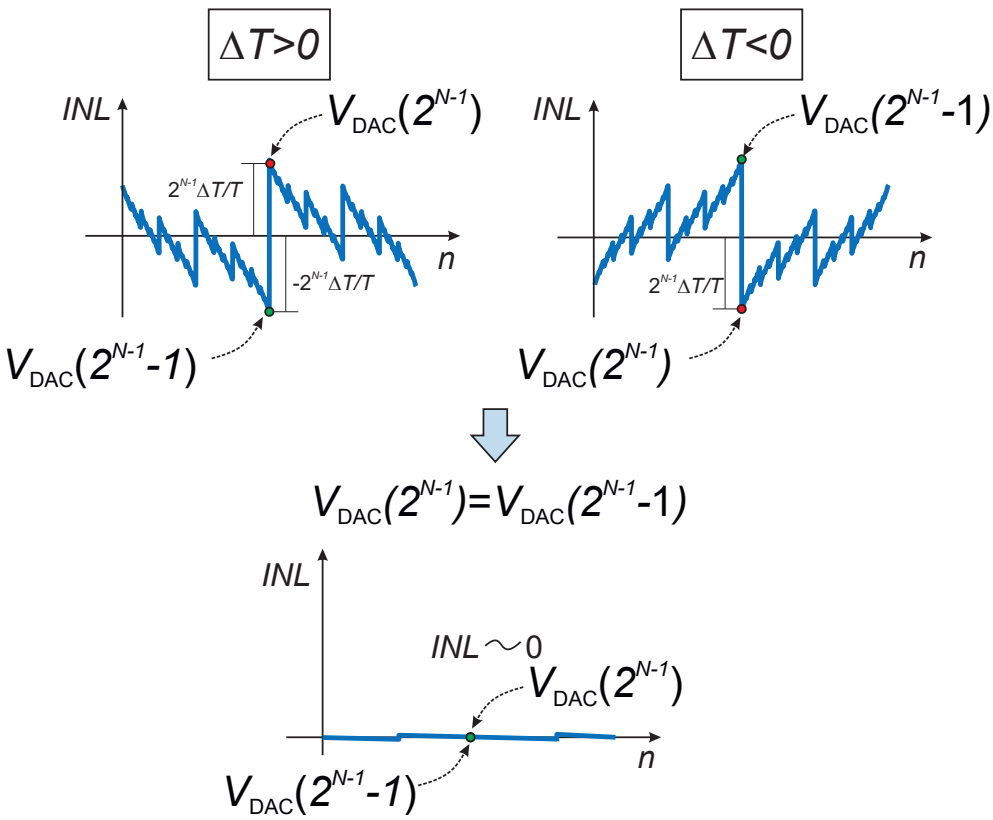


Figure 3.1: Relation between ReDAC nonlinearity and clock period exploited in calibration.

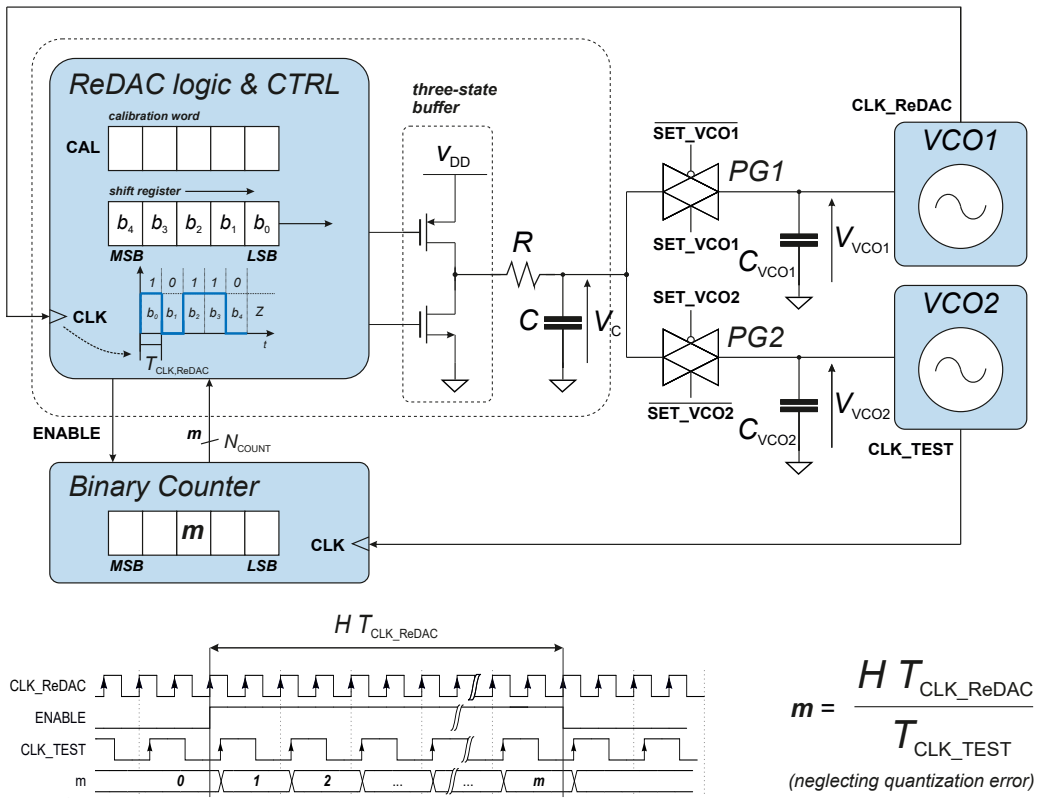


Figure 3.2: ReDAC with foreground calibration architecture.

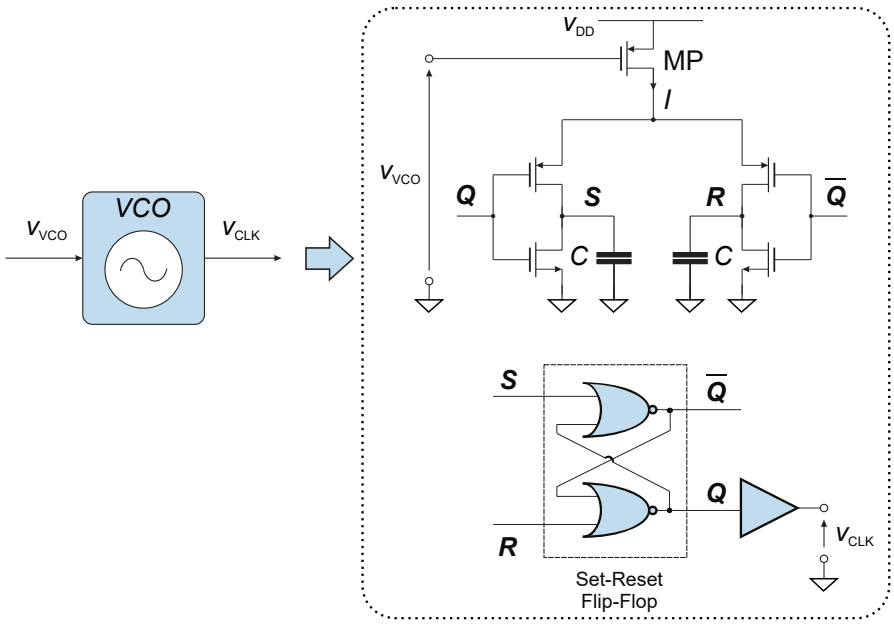


Figure 3.3: Relaxation VCO topology.

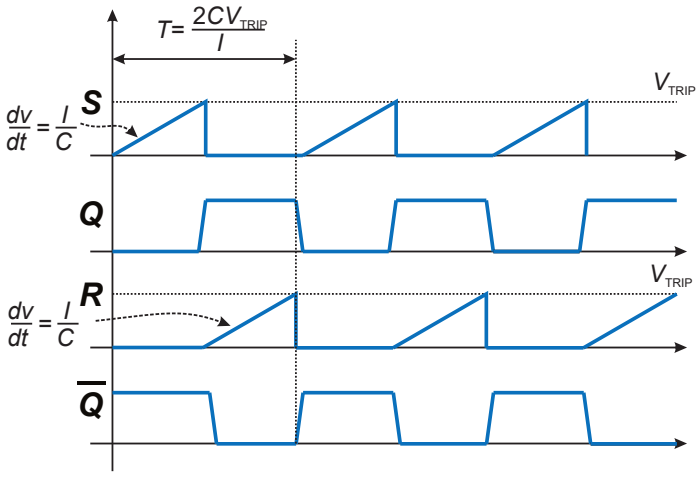


Figure 3.4: Relaxation VCO timing diagram.

3.2.2 Self Calibration Procedure

The calibration procedure follows the flowchart in Fig. 3.5. In the first step of the single calibration cycle the input of $V_{\mathrm{VCO},1}$ is held at the last voltage value set by the previous calibration cycle (at startup $C_{\mathrm{VCO},1}$ is discharged so the oscillator starts at its maximum frequency) then converts the internally stored digital calibration word CAL on N bits into its corresponding voltage $V_{\mathrm{cal}} = V_{\mathrm{DAC}}(\mathrm{CAL})$ which is applied to the capacitor $C_{\mathrm{VCO},1}$ by means of the pass gate PG1, therefore updating the oscillating frequency of the ReDAC clock $f_{\mathrm{CLK\_ReDAC}}$ depending on the CAL value.

The second step involves the conversion of the code 2^{N-1} into its corresponding voltage $V_{\mathrm{DAC}}(2^{N-1})$, which is then applied to the input of $V_{\mathrm{VCO},2}$ by enabling the switch PG2. The binary counter is reset and it is enabled to count, for a fixed time dictated by an integer number of VCO1 periods $H \cdot T_{\mathrm{CLK\_ReDAC}}$, the number of edges of the VCO2 output $f_{\mathrm{CLK\_TEST}}$ which will be related to the value $V_{\mathrm{VCO},2} = V_{\mathrm{DAC}}(2^{N-1})$. When the enabling window ends the counter stores a value m expressed as

$$m(2^{N-1}) = \frac{2H\, f_{\mathrm{CLK\_TEST}}(2^{N-1})}{f_{\mathrm{CLK\_ReDAC}}} \simeq \alpha \cdot V_{\mathrm{DAC}}(2^{N-1}) \tag{3.1}$$

which is proportional to $V_{\mathrm{DAC}}(2^{N-1})$ (neglecting the quantization error) by the term

$$\alpha = \frac{2H \cdot k_{\mathrm{VCO},2}}{f_{\mathrm{CLK\_ReDAC}}} \tag{3.2}$$

where $k_{\mathrm{VCO},2}$ indicates the VCO gain. In practice, the counter final value $m(2^{N-1})$ can be considered as the analog-to-digital re-conversion of the voltage $V_{\mathrm{DAC}}(2^{N-1})$ by means of the VCO-based ADC implemented with the counter and the VCO2 oscillator.

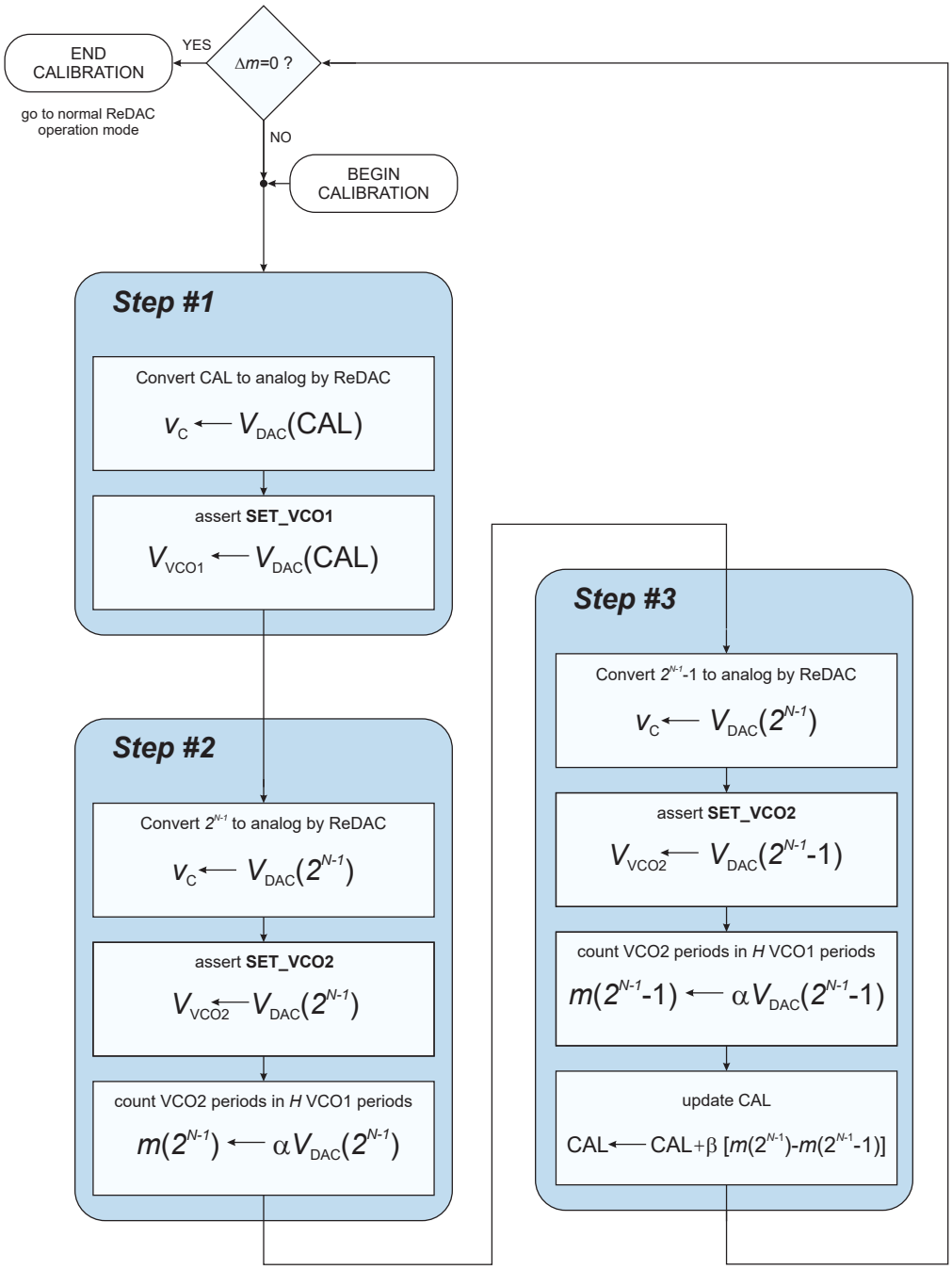


Figure 3.5: VCO-based calibration flowchart.

In the third calibration step the code $2^{N-1} - 1$ is converted by the ReDAC under the same clock frequency $f_{\text{CLK\_ReDAC}}$ of the second step, and repeating the same operations as before: sampling of $V_{\text{DAC}}(2^{N-1} - 1)$ on $C_{\text{VCO},2}$, resetting the counter and enabling it for the same time period $H \cdot T_{\text{CLK\_ReDAC}}$. At the end of the third step the counter content will be the digital representation of $V_{\text{DAC}}(2^{N-1} - 1)$ analogously to (3.1):

$$m(2^{N-1} - 1) \simeq \alpha V_{\text{DAC}}(2^{N-1} - 1). \tag{3.3}$$

The difference Δm of the two digital values stored in the counter at the end of steps second and third is related to the maximum nonlinearity voltage step ΔV_{DAC}, which in turn is proportional to the clock error ΔT according to (2.12) in Chapter 2. This difference is not affected by mismatch or, more generally, errors added by VCO2 or the sampling switch PG2 since the two ReDAC voltages are compared using the same hardware path.

The value of Δm can therefore be regarded as the error signal of the feedback loop to correct the ReDAC clock period by updating the calibration word CAL according to:

$$\text{CAL}^{\text{new}} = \text{CAL}^{\text{old}} - \beta_{\text{FB}} \cdot \Delta m \tag{3.4}$$

being β_{FB} an opportune gain coefficient in the negative feedback loop, resulting in a reduction of the error ΔV_{DAC} in time and approaching $\Delta V_{\text{DAC}} = 0$ ($\Delta m = 0$) to finally enforce $\Delta T \simeq 0$ as in Fig. 3.1.

It is worth noting that, approaching the end of calibration, when ΔV_{DAC} approaches zero, VCO2 operates at nearly the same input voltage in Step #2 and Step #3, making the difference Δm tolerant to the voltage-frequency nonlinearity of the VCO.

The calibration cycle is repeated until when $\Delta m = 0$, resulting in $\Delta V_{\text{DAC}} = 0$ within the calibration quantization error, and the calibration is terminated letting the ReDAC operate at nominal resolution under the clock provided by the tuned VCO1, which corresponds to the last CAL word.

3.3 Design and Validation by Simulations

3.3.1 Design

The ReDAC is designed in 40 nm CMOS technology to achieve 2 MS/s and 10 bit resolution under 0.6 V supply, as first presented in [81].

The ReDAC is designed according to the guidelines presented in Chapter (2), i.e.:

- due to the absence of matching constraints the size of the MiM capacitor is chosen to be close to the thermal noise limit (2.18), resulting in $C = 450\,\text{fF}$;
- the clock period T is designed according to the target sample rate, considering $N = 10$ bits and two more periods for the hold phase, i.e. $T_{\text{conv}} = (2\,\text{MS/s})^{-1} = (N+2)T$, leading to $T = 40\,\text{ns}$;
- the Hi-res polysilicon resistor is designed based on the target time constant, linked to the clock period by (2.4), resulting in $R = 128\,\text{k}\Omega$, and uses minimum physical width to keep at minimum the parasitic capacitance towards the substrate;
- the three-state buffer output transistors are designed to avoid non-linear loading effect in driving the RC network, resulting in aspect ratios of 1.6 µm/40 nm and 0.8 µm/40 nm for the pMOS and nMOS transistors in Fig.3.2 , respectively.

The layout of the ReDAC core (excluding calibration) is visible in Fig. 3.6

3.3.2 Simulation Results

The blocks in Fig. 3.2 are simulated at different abstraction levels: the ReDAC core, pass gates and VCOs are modelled at transistor level, while the binary counter and the self-calibration logic are described in Verilog-A.

The self-calibration trend of the VCOs simulated input are reported in Fig. 3.7(a). The control voltage of VCO1 converges to a voltage of 147.8 mV, corresponding to an optimal clock period $T = 40.8\,\text{ns}$. The VCO2 input oscillates between two voltage level which difference is related to ΔV_{DAC}, until it reaches 200 μV at the end of calibration.

In Fig. 3.7(b) a zoom-in of the ReDAC capacitor voltage at the beginning and at the end of the process is highlighted, showing the three calibration steps as well as the convergence to the same value of the output voltages $V_{\text{DAC}}(2^{N-1})$ and $V_{\text{DAC}}(2^{N-1}-1)$ in the second and third steps.

The post-calibration ReDAC performance has been characterized and compared to the non-calibrated ReDAC having 3.2% error on the clock period. The static nonlinearity is evaluated as 0.98 (0.40) LSB of maximum (rms) INL and 1.00 (0.06) LSB of DNL for the calibrated ReDAC which is improved compared to the 8.67 (3.3) LSB of maximum (rms) INL and 17.2 (0.8) LSB of DNL in the uncalibrated ReDAC.

Dynamic characterization of the calibrated ReDAC performed under 90 % swing sine wave input at 20.42 kHz (equivalent to $1/100T_{\text{conv}}$) reveals 62.9 dB SFDR, 60.16 dB THD and 56.13 dB SNDR corresponding to

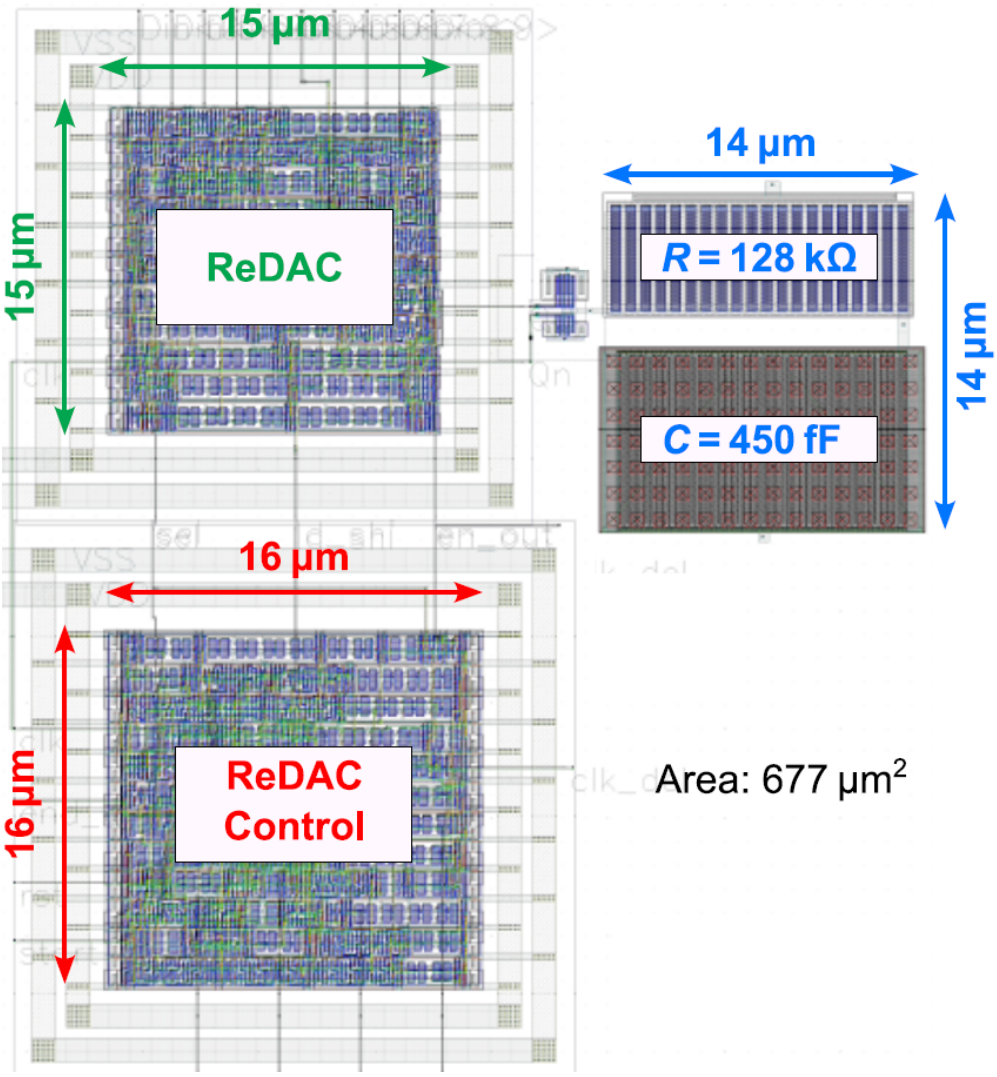
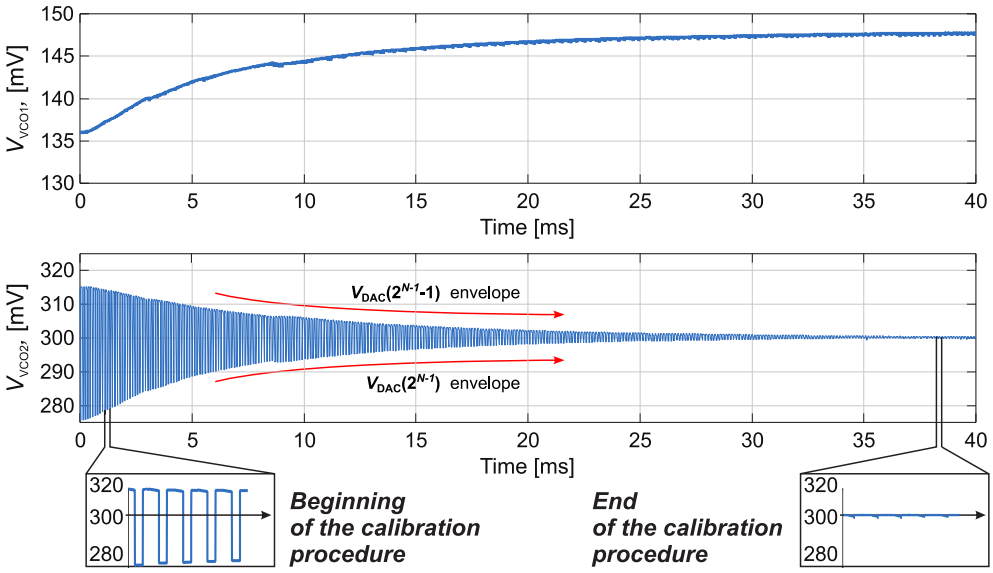
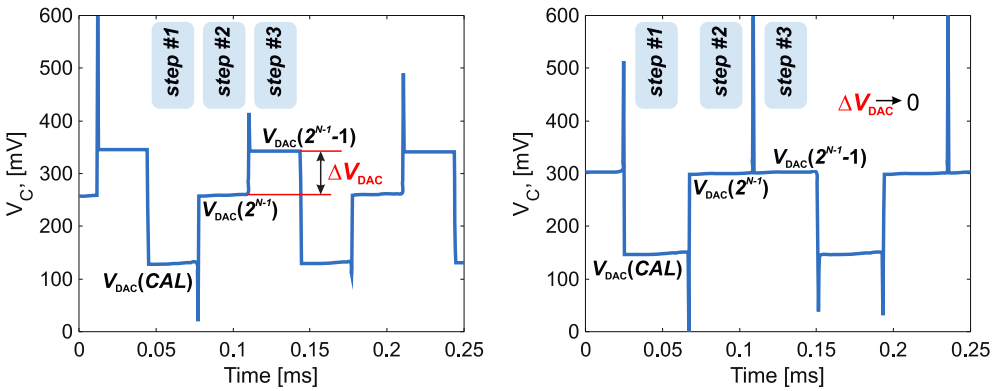


Figure 3.6: ReDAC core layout in 40 nm CMOS.

9.06 ENOB. Compared to the uncalibrated Relaxation Digital-to-Analog Converter (ReDAC) the calibration allows for 18 dB higher SFDR, 16 δ higher THD, 15 dB higher SNDR, resulting in 2.5 more ENOB, validating the effectiveness of the calibration strategy. The ReDAC implementation proves to be extremely competitive in terms of efficiency, having a total energy per conversion (energy FOM) of 0.73 pJ (1.08 fJ/(c·s)).

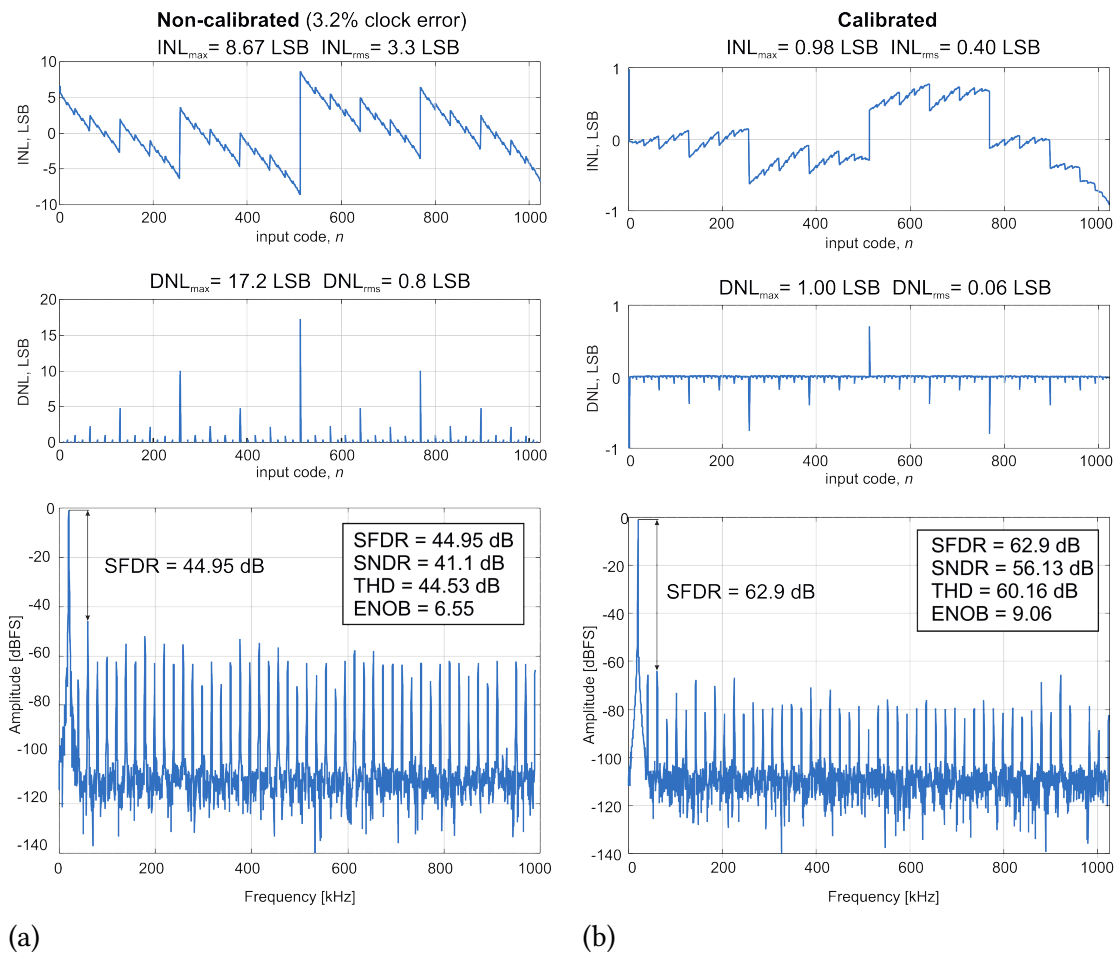


(a)



(b)

Figure 3.7: Simulated VCO1 and VCO2 calibration voltages (a) and zoom-in of the ReDAC capacitor voltage, highlighting the three calibration steps (b).



(a) (b)

Figure 3.8: ReDAC static and dynamic characterization under 20.42 kHz, 90 % swing sine wave for the uncalibrated ReDAC (a) and after calibration (b).

Chapter 4

FPGA-based ReDAC converters featuring parasitics supression and digital calibration

Fourth chapter presents the first physical implementation of self-calibrated ReDAC prototypes, on 10 and 13 bits respectively. The presented designs exploit a clock-division based calibration and an effective voltage-to-time to digital conversion to enforce the converter linearity. The parasitics error suppression strategy is here implemented in hardware for the first time and validated by measurements trough a complete performance characterization.

4.1 Motivation

As discussed in the introductory chapter, developing Integrated Circuits (ICs) of increasing complexity is demanding effective design strategies to reduce effort, development time, cost, and time-to-market [93].

Reconfigurable hardware such as Field Programmable Gate Arrays

(FPGAs) are particularly effective for prototyping and production at small/ medium scale of digital circuits, while analog circuits do not benefit of equally attractive solutions since reconfigurable analog platforms [94]–[96] can target only specific circuit topologies such as analog filters or amplifiers which often cannot compete with the performance of custom analog hardware.

From this perspective, the digital-intensive implementation of analog and mixed signals (AMS) blocks, introduced in Chapter 1 [24], [25] as a strategy to take advantage of silicon integration in newer technology nodes for reduced supply voltages operation, small area and power, is here proposed as a strategy of coping with rapid prototyping of AMS blocks in conventional FPGA architectures, and the consequent possibility of scaling consistently their performance to Application-Specific Integrated Circuits (ASICs) on the base of the same Hardware Description Language (HDL) design.

Example architectures exploiting such strategy have recently been applied to Digital-to-Analog Converters (DACs) [31], [97]–[100], Analog-to-Digital Converters (ADCs) [101], Digital-to-Time Converters (DTCs) [102] and Time-to-Digital Converters (TDCs) [103].

Concerning the DACs, the Relaxation Digital-to-Analog Converter has been explored as an alternative to Digital Pulse-Width Modulation (DPWM) [98], sigma-delta ($\Sigma\Delta$) modulation [99], [100], [104] and Dyadic-Digital Pulse Modulator (DDPM).

The first FPGA prototype [30] required impractical external calibration, and its accuracy (7 ENOB) and sample rate (400 S/s) was strongly limited by the parasitics of the discrete RC network.

A complete self-calibrated ReDAC hardware implementation on FPGA was therefore developed [105] and it is discussed in the present chapter. Unlike the integrated implementation of Chapter 3, the FPGA prototype could not take advantage of VCOs for self-calibration, requiring a different strategy. In order to get rid of the parasitics, the parasitics error suppression presented in Chapter 2 was implemented in hardware for the first time [105] validating its effectiveness by experimental results.

4.2 FPGA-based ReDAC

4.2.1 Architecture

Two FPGA prototypes featuring self calibration are discussed, operating at 514 S/s (10.5 kS/s) and 13 bit (11 bit) resolutions. The two ReDACs are based on the architecture shown in Fig. 4.1. The ReDAC Control Block (ReDAC

core) is in charge of converting the digital input DATA, which is provided by an external digital synthesizer or, alternatively, by the Calibration Control block, in normal operation or during calibration respectively.

The D/A conversion starts synchronously with the first edge of the clock $f_{\mathrm{clk,ReDAC}}$, after the signal *Convert* is asserted, as reported in the timing diagram of Fig. 4.2.

The clock signal $f_{\mathrm{clk,ReDAC}}$ drives the ReDAC and the Calibration Control as well, and it is obtained by clock division of the system FPGA clock f_{clk} by a divide-by-$2m$ frequency divider, consisting ina free-running counter toggling the $f_{\mathrm{clk,ReDAC}}$ signal when reaching the terminal count m, as in Fig. 4.3.

The value of m is initialized at reset at the value $m = m_0 = \lceil f_{\mathrm{clk}} T^* / 2 \rfloor$ to satisfy (2.4) of Chapter 2 for the nominal values of FPGA system clock, R and C, than it is tuned by the self calibration proposed in the following to compensate for component tolerance and drifts.

The same free-running counter has a second terminal count m_{del} generating a clock clk,ReDAC,del at the same frequency of $f_{\mathrm{clk,ReDAC}}$ and delayed by $T_{\mathrm{del}} = m_{\mathrm{del}} T_{\mathrm{clk}}$, which is required by the parasitics suppression strategy as presented in Section 2.3.4 of Chapter 2.

The self calibration includes the capacitor discharge network consisting in an open-drain buffer connected to the ReDAC capacitor by a resistor R_{disch}, a comparator and an up/down counter operated at the system clock. This calibration harness is working as single slope ADC and employed to compare voltages converted by the ReDAC, according to the calibration principle presented in Section 2.2.2.

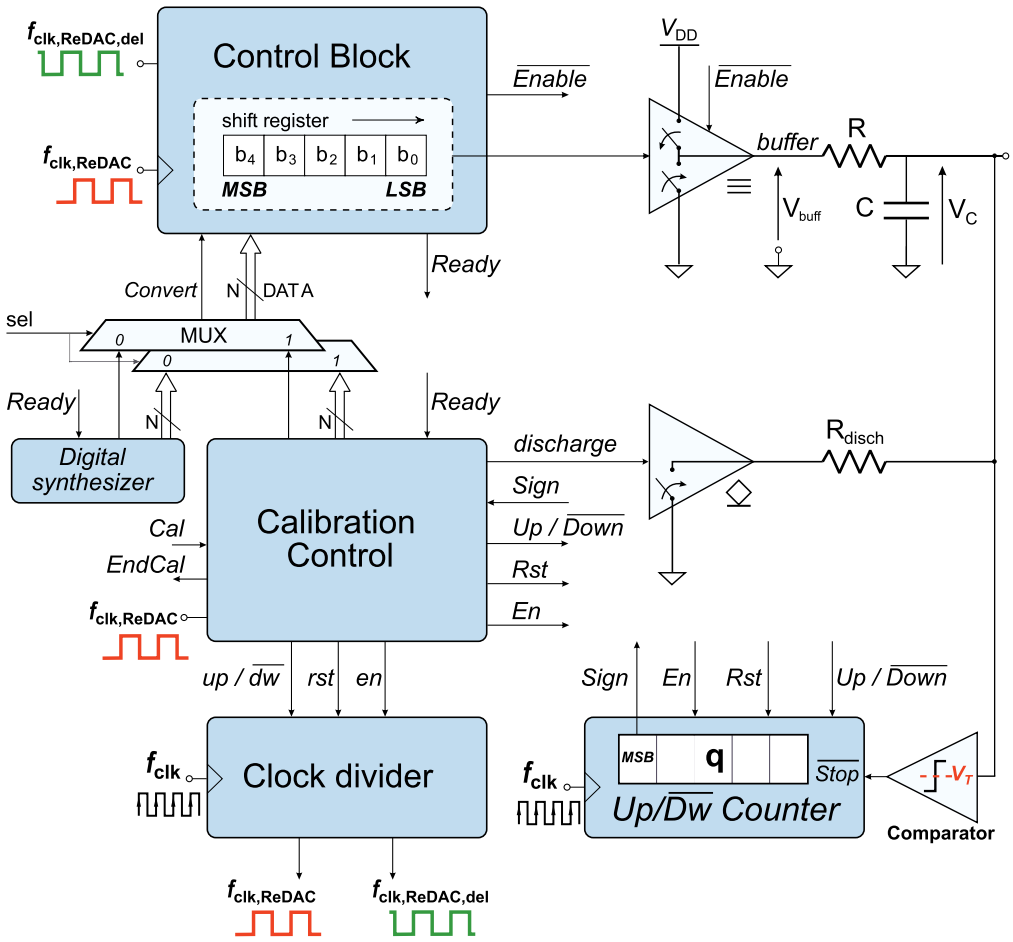


Figure 4.1: FPGA ReDAC architecture.

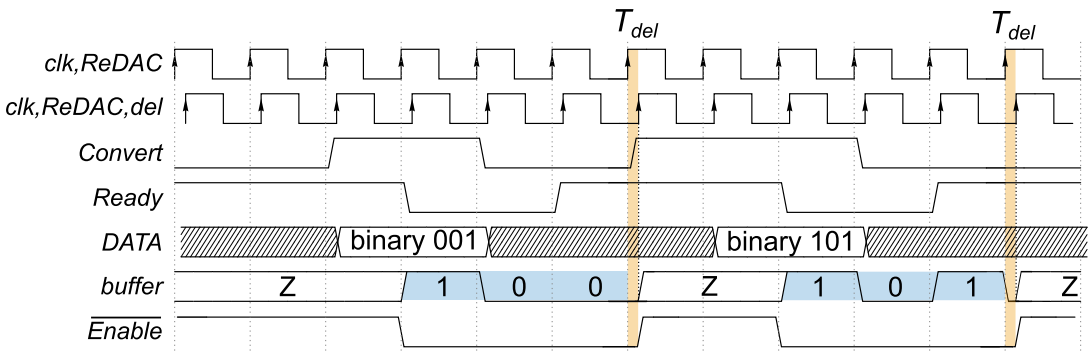


Figure 4.2: FPGA ReDAC timing diagram.

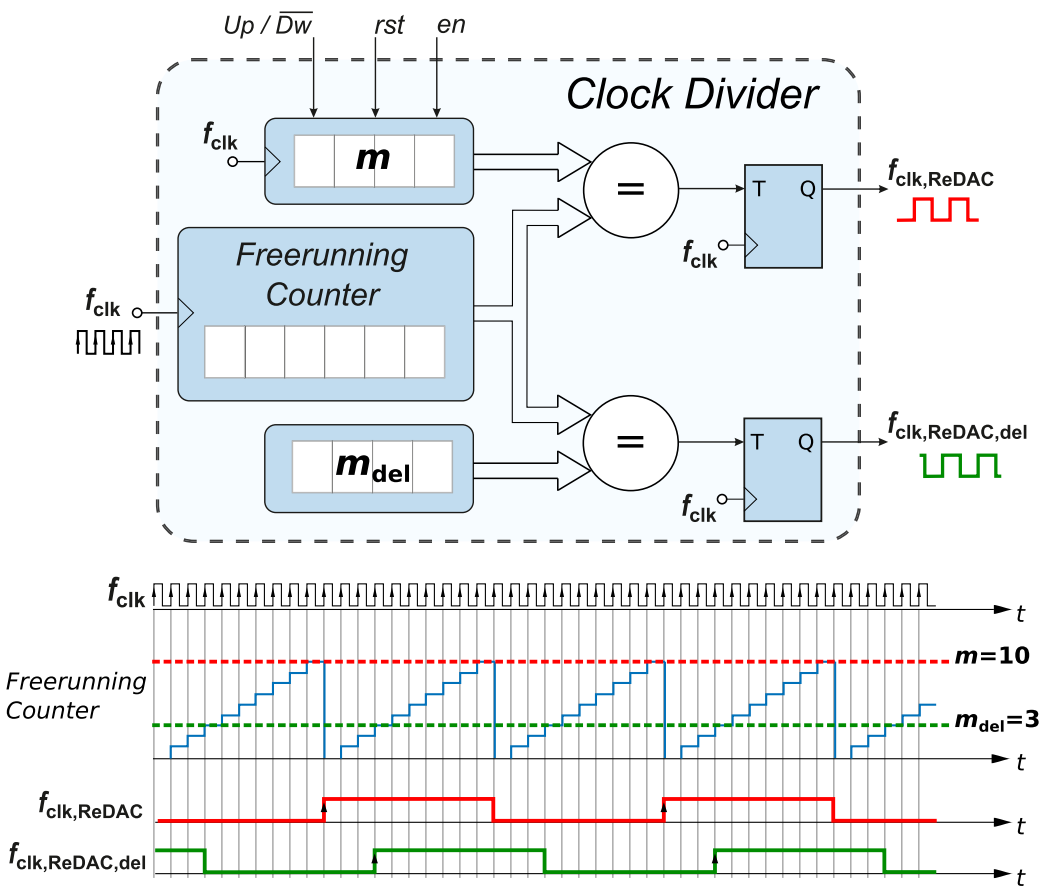


Figure 4.3: Clock divider and its timing diagram.

4.2.2 Self calibration procedure

The self calibration operates according to the flowchart in Fig. 4.4, while the timing diagram of the four steps is reported in Fig. 4.5.

At the beginning of the calibration, the ReDAC is operated at the close-to-optimum frequency $f_{\mathrm{clk,ReDAC}} = f_{\mathrm{clk}}/2m_0$ and converts the digital code $2^{N-1} - 1$. The three-state buffer is driven low for a period T_{del} after conversion then put in high impedance on the rising edge of $f_{\mathrm{clk,ReDAC,del}}$.

The up/down counter is enabled together with the discharge network (connecting R_{disch} in parallel to C). As a result, the capacitor is exponentially discharged with a time constant $\tau_{\mathrm{disch}} = R_{\mathrm{disch}}C$ and its voltage, initially equal to $V_{\mathrm{DAC}}(2^{N-1} - 1)$, decreases until it crosses the threshold $V_{\mathrm{T}} < V_{\mathrm{DAC}}(2^{N-1})$ of the comparator, disabling the counter. The value q stored in the counter at the end of Step #2 is

$$q(2^{N-1} - 1) = \lfloor T_{\mathrm{disch}}(2^{N-1} - 1) f_{\mathrm{clk}} \rfloor$$

and related to the discharge time (neglecting calibration)

$$T_{\text{disch}}(2^{N-1}-1) = \tau_{\text{disch}} \cdot \log\left[\frac{V_{\text{DAC}}(2^{N-1}-1)}{V_{\text{T}}}\right], \tag{4.1}$$

which is itself a monotonic nonlinear function of $V_{\text{DAC}}(2^{N-1})$.

Step #3 is equivalent to Step #1, this time converting the digital code 2^{N-1} instead of $2^{N-1}-1$; Step #4 repeats the discharge operation of Step #2 with the difference that the up/down counter is now set to down count, until V_{T} is crossed after a time

$$T_{\text{disch}}(2^{N-1}) = \tau_{\text{disch}} \cdot \log\left[\frac{V_{\text{DAC}}(2^{N-1})}{V_{\text{T}}}\right]. \tag{4.2}$$

The value q stored in the counter at the end of the four calibration steps is therefore proportional to the signed difference of the quantised discharge times in Step #2 and #4:

$$\begin{aligned} \Delta q &= q(2^{N-1}-1) - q(2^{N-1}) \\ &= f_{\text{clk}}\lfloor T_{\text{disch}}(2^{N-1}-1) - T_{\text{disch}}(2^{N-1})\rfloor \\ &\simeq -f_{\text{clk}}\tau_{\text{disch}} \cdot \log\left[\frac{V_{\text{DAC}}(2^{N-1})}{V_{\text{DAC}}(2^{N-1}-1)}\right], \end{aligned} \tag{4.3}$$

and it is zero if

$$\Delta V_{\text{DAC}} = V_{\text{DAC}}(2^{N-1}) - V_{\text{DAC}}(2^{N-1}-1) = 0, \tag{4.4}$$

otherwise it is $q > 0$ ($q < 0$) if $\Delta V_{\text{DAC}} < 0$ ($\Delta V_{\text{DAC}} > 0$).

The difference ΔV_{DAC} is in turn proportional to the ReDAC clock error ΔT according to (2.12) in Chapter 2, so that $\Delta q = 0$ implies the calibration condition (2.4), within 1 LSB of ReDAC nonlinearity, and the calibration ends-

On the contrary, if $\Delta q > 0$ ($\Delta q < 0$) the terminal count m is decreased (increased). The four calibration steps are repeated until (2.4) is met ($\Delta q = 0$).

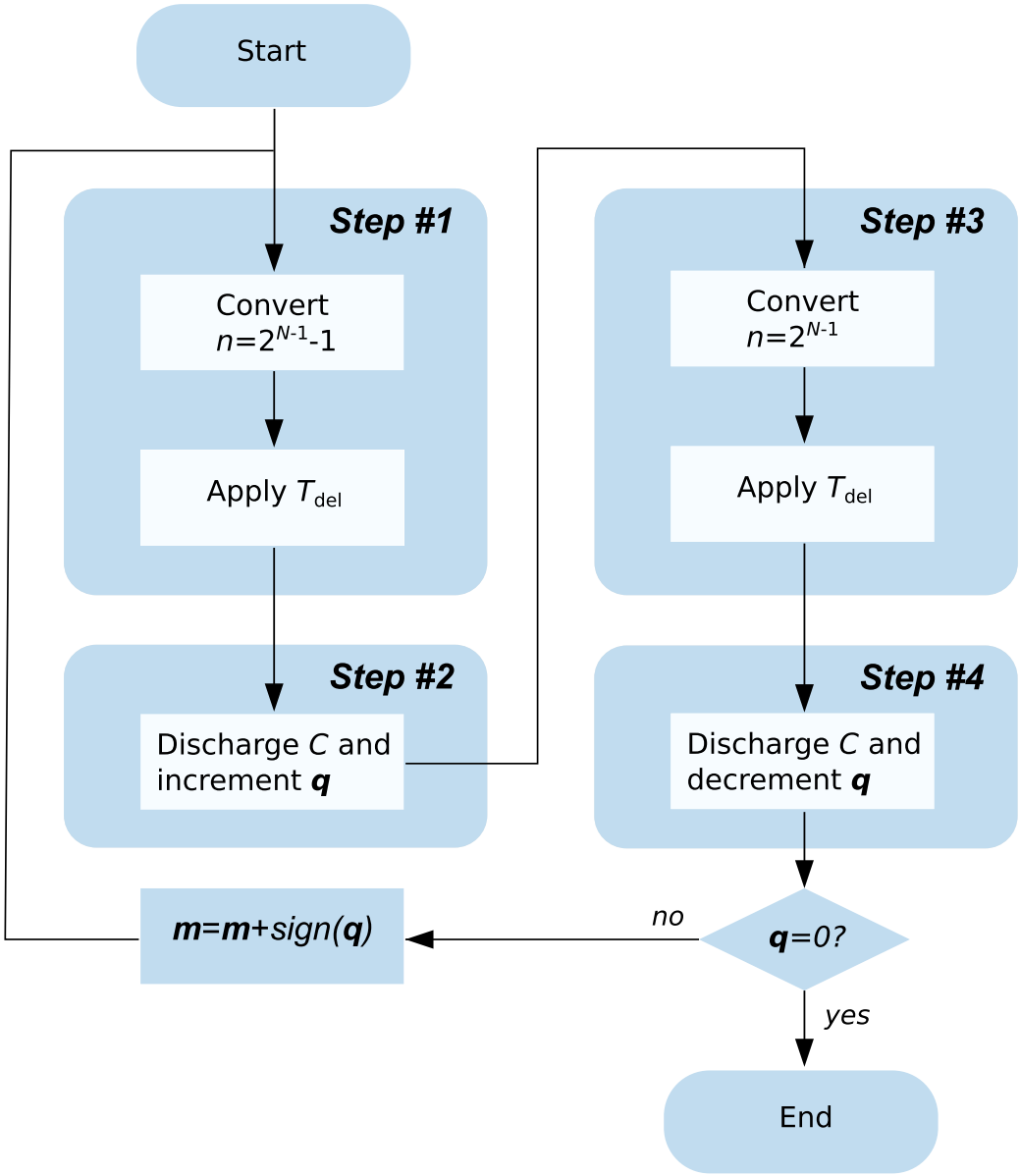


Figure 4.4: FPGA Self Calibration flowchart.

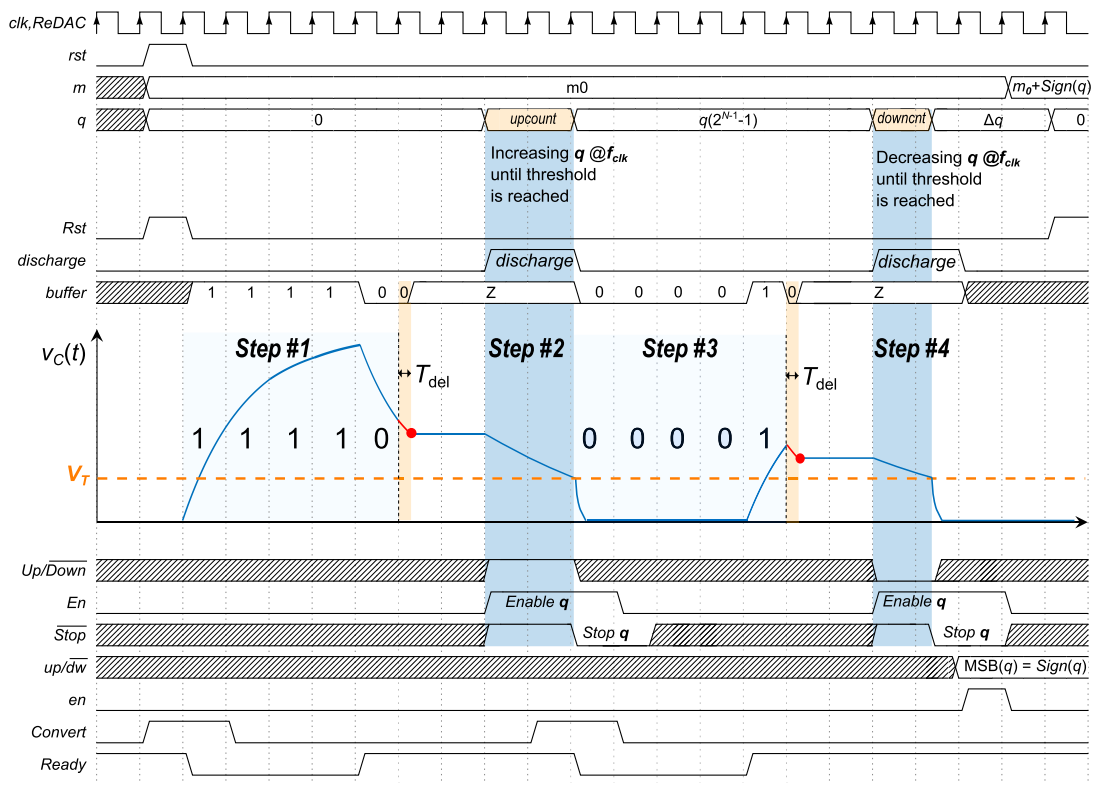


Figure 4.5: FPGA Self Calibration timing diagram.

Considerations on the Self-Calibration

The duration of each calibration step, including two conversions and two discharge periods, is expressed using the same notation in (2.20) as

$$T_{\text{cs}} \simeq 2 \cdot [(N + \beta)T^* + T_{\text{disch}}(2^{N-1})]. \tag{4.5}$$

Being the value of m updated by one unit in each calibration cycle, the amount of steps $\#cs$ needed to complete the calibration is expressed by the difference $\#cs = |m_0 - m^*|$ between the initial value of the terminal count m_0 and the optimal one m^* satisfying (2.4).

After the first calibration is complete, few calibration steps are needed to compensate for drift and temperature variations in R and C, supposing slow changes in temperature and the possibility of scheduling timeslots for few re-calibration steps.

Temperature-related errors associated with the RC time constant variations can also be limited by employing intrinsically-low thermal drift discrete components at a slightly higher cost or using a frequency reference able to track the time constant variations (for example, by using an

oscillator which frequency is set by resistors and capacitors with the same thermal drift of the ReDAC R and C).

4.2.3 Self calibration design

The discharge network implementing the nonlinear single-slope A/D conversion is dimensioned considering that the difference

$$\begin{aligned}\Delta T_{\text{disch}} &= T_{\text{disch}}(2^{N-1}) - T_{\text{disch}}(2^{N-1}-1) \\ &= \tau_{\text{disch}} \log \frac{V_{\text{DAC}}(2^{N-1})}{V_{\text{DAC}}(2^{N-1}-1)} \simeq \tau_{\text{disch}} 2^{-N+1}\end{aligned}$$

needs to be larger than the time resolution provided by the system clock period T_{clk} in measuring the discharge times of Step #2 and #4 of the calibration, so it must hold

$$\tau_{\text{disch}} = R_{\text{disch}} C > T_{\text{clk}} 2^{N-1}. \tag{4.6}$$

The only requirement for the comparator threshold voltage V_{T} is not to vary during calibration, and its value does not need to be precisely set, provided that both voltages $V_{\text{DAC}}(2^{N-1}-1)$ and $V_{\text{DAC}}(2^{N-1})$ are above the threshold when the initial ReDAC clock division factor m_0 is set, i.e. in presence of reasonably large initial errors ΔT on the ReDAC period.

Consequently, the bit width of the up/down counter q is designed based on the comparator threshold to avoid counter overflow given the discharge times:

$$q > f_{\text{clk}} T_{\text{disch}}(2^{N-1}) \simeq f_{\text{clk}} T_{\text{disch}}(2^{N-1}-1).$$

4.3 Experimental results

4.3.1 Hardware implementation

Two ReDAC designs, ReDAC1 and ReDAC2, have been implemented on a an Altera DE1-SoC FPGA board, featuring a Cyclone V (5CSEMA5F31C6) FPGA IC, operated at 50 MHz clock generated by a on-board crystal oscillator, under 3.3 V supply. The two ReDACs are operated at 13 bit resoolution, 514 S/s and 11 bit resolution, 10.5 kS/s respectively.

Both prototypes implement the parasitics error suppression, which theory has been introduced in Section 2.3.4 of Chapter 2 (employing the architecture described in 4.2.1 of this chapter), and the digital self calibration as described in Section 4.2.2.

The ReDAC design follows the guidelines exposed in Section 2.3.2 of Chapter 2, leading to $C = 1\,\text{nF}$ and $R = 180\,\text{k}\Omega$ for the ReDAC1 and $C = 2.2\,\text{nF}$, $R = 4.7\,\text{k}\Omega$ in the ReDAC2.

Since the two prototypes operate under the same system clock, the discharge network of the two employs the same discharge resistor $R_{\text{disch}} = 820\,\text{k}\Omega$ meeting the requirements in (4.6) with a sufficient margin for both the implementations, and a threshold voltage $V_{\text{T}} = V_{\text{DD}}/4$ obtained by a resistive voltage divider. The few passives required for ReDAC operation are discrete Surface Mounted (SMT) devices soldered on one prototyping board (PB) for each DAC, connected by a header to the FPGA board General Purpose Input Output (GPIO) socket.

The comparator needed for calibration and the three-state FPGA buffer are also soldered on the PB board to reduce at minimum the interconnect parasitics between them ant the ReDAC RC network, given that the PCB traces from the FPGA to the GPIO socket are in the order of 10 cm length.

In a custom PCB implementation of the ReDAC, a built-in three-state buffer of the FPGA I/O pins can directly be used, and the external comparator avoided by exploiting a low-voltage differential signaling (LVDS) input of the FPGA, therefore avoiding the drawback of external components.

To probe the ReDAC output and decouple it from the testing equipment a voltage-following operational amplifier is soldered on the same PB. The experimental setup employed for ReDAC testing is reported in the photograph of Fig. 4.6, along with a sample conversion waveform of the ReDAC.

The ReDAC and Calibration block are synthesized on the FPGA from their HDL description and occupy only 6 and 105 logic elements respectively of the FPGA resources.

The parasitic suppression strategy is synthesized according to the digital clock division described in Section 4.2.1, and a clock delay of $T_{\text{del}} = 2.4\mu\text{s}$ and $T_{\text{del}} = 0.6\mu\text{s}$ is enough to fully damp the parasitics-related nonlinearity of ReDAC1 and ReDAC2 respectively. A configurable direct digital synthesizer is mapped on the same FPGA to generate digital ramps and sinusoids needed for ReDAC static and dynamic performance testing.

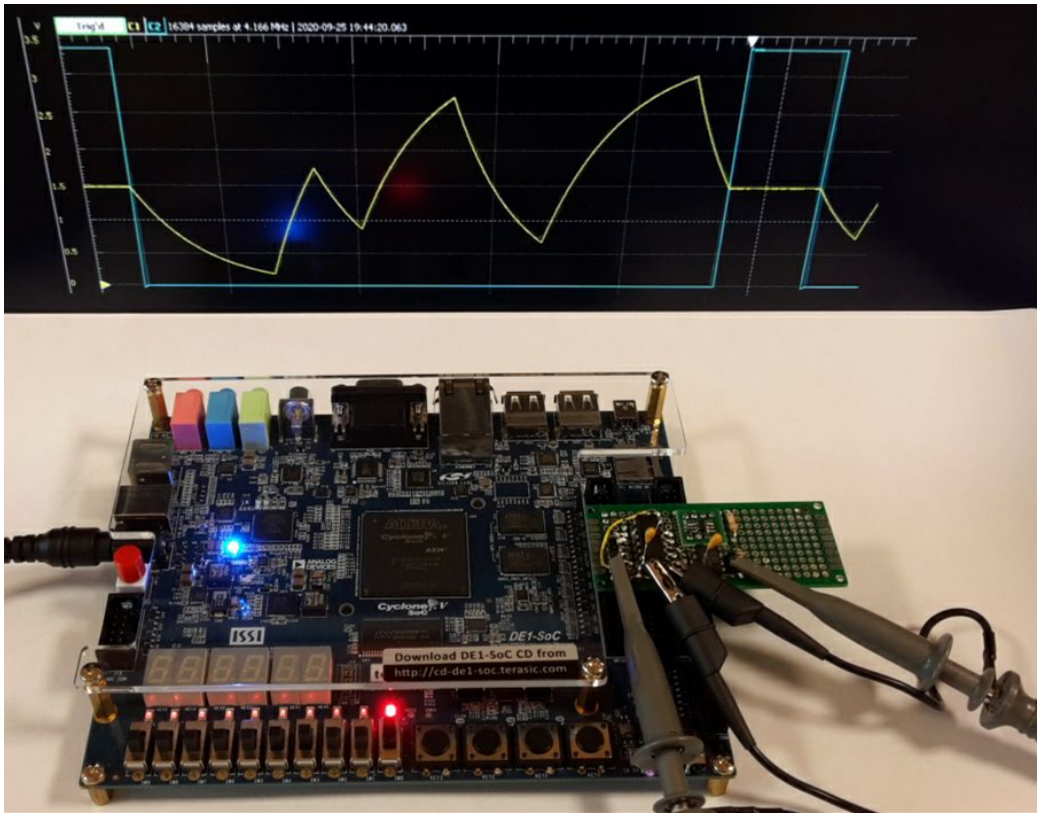
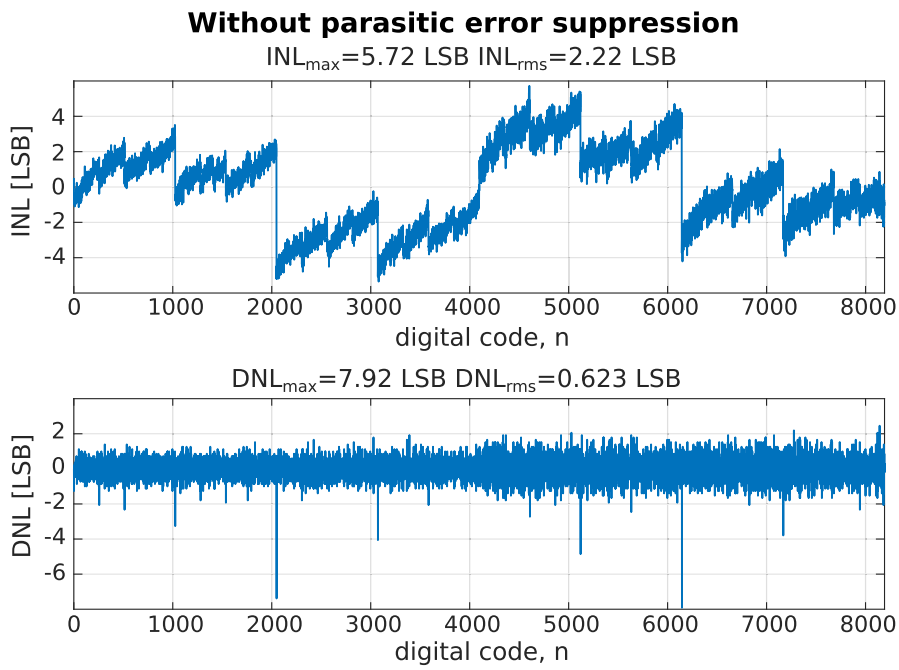


Figure 4.6: ReDAC FPGA prototype test setup photograph. The probed capacitor voltage of a generic conversion is shown.

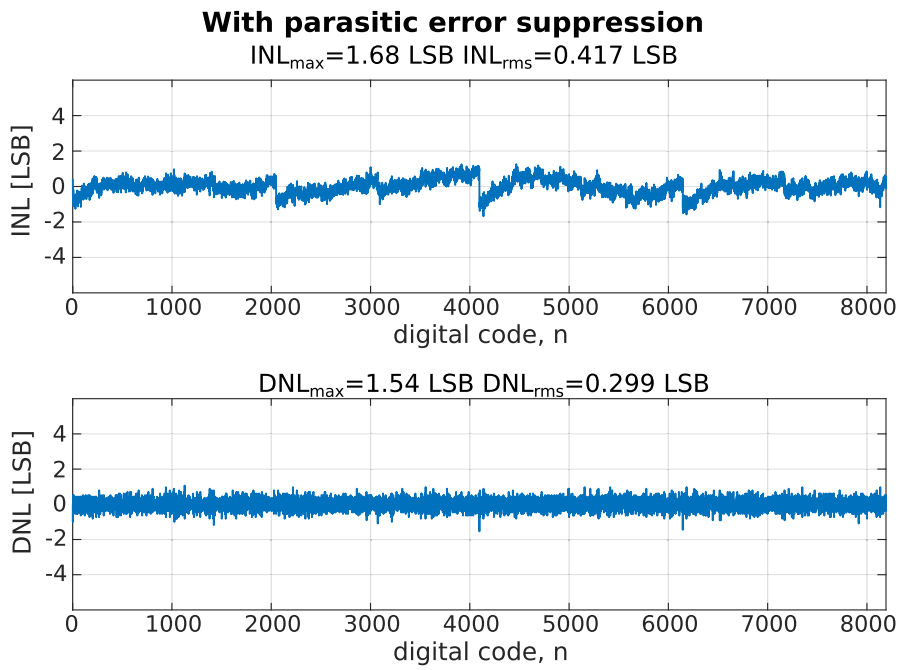
4.3.2 ReDAC1 characterization

The characterization of ReDAC1 provided the chance to validate the parasitics error suppression by experimental results for the first time [105]. In Fig. 4.7(a) and Fig. 4.7(b) the ReDAC1 static performance, derived after running the automatic digital self calibration, is reported for the same ReDAC without and with (i.e. $T_{\text{del}} = 0\,\mu\text{s}$ and $T_{\text{del}} = 2.4\,\mu\text{s}$) the parasitic error suppression strategy.

It is shown that the maximum INL (DNL) of 5.72 LSB (7.92 LSB) without using the parasitics error suppression is reduced to 1.68 LSB (1.54 LSB) by using the parasitics suppression. Analogously, the rms INL (DNL) is improved from 2.22 LSB (0.623 LSB) to 0.417 LSB (0.299 LSB) thanks to the adoption of the error suppression, effectively proving the effectiveness of the technique.



(a)

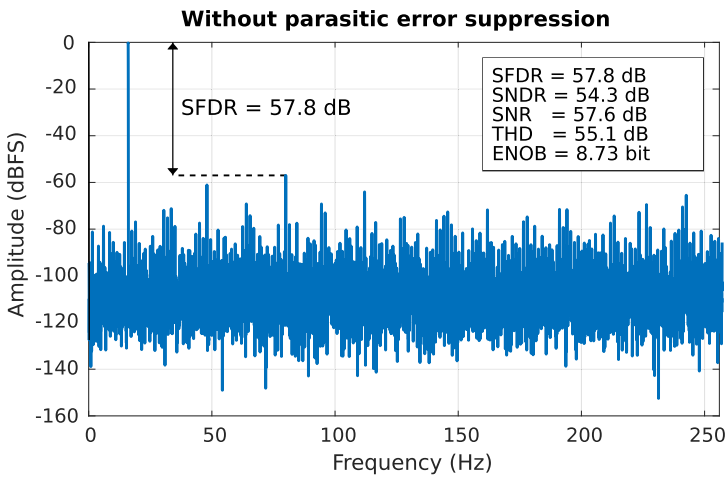


(b)

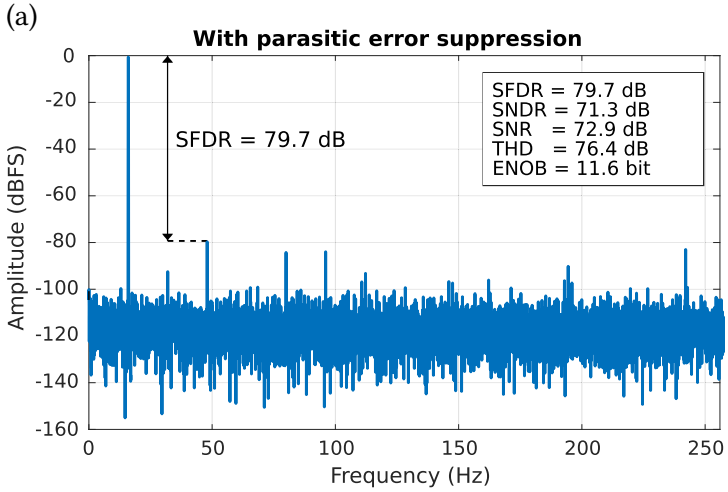
Figure 4.7: Static characterization of ReDAC1 without (a) and with (b) the parasitics error suppression, showing the efficacy of the strategy.

Dynamic characterization at 16 Hz sinewave input, 90% swing without the error suppression (Fig. 4.8(a)) technique reveal 57.8 dB of SFDR, 57.6 dB SNR, 55.1 dB of THD and 54.3 dB SNDR, equivalent to 8.73 ENOB. Performance improve with the introduction of the parasitics suppression (Fig. 4.8(b)) and achieve, for the same prototype, 79.7 dB SFDR, 72.9 dB SNR, 76.4 dB THD and 71.3 dB SNDR, resulting in 11.6 ENOB, corresponding in a net accuracy improvement of 2.87 effective bits.

Figure 4.9(a) reports the dynamic characterization in frequency for input sine waves having constant amplitude (90% of full swing) up to the Nyquist frequency while Fig. 4.9(b) shows the dynamic characterization at constant sine frequency (0.3 Hz) ranging in the ReDAC swing, both revealing consistent ReDAC operation.



(a)



(b)

Figure 4.8: Single frequency dynamic characterization of ReDAC1 without (a) and with (b) the parasitic error suppression.

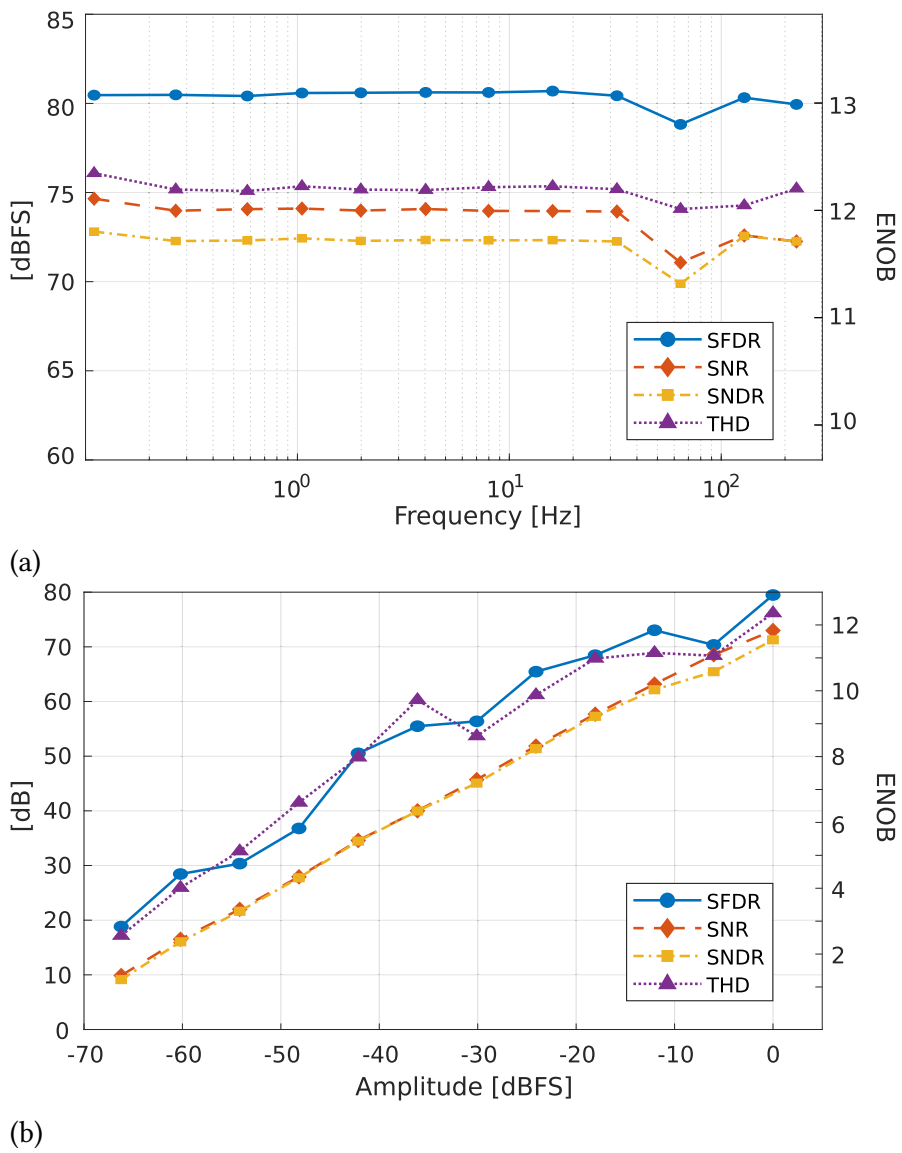


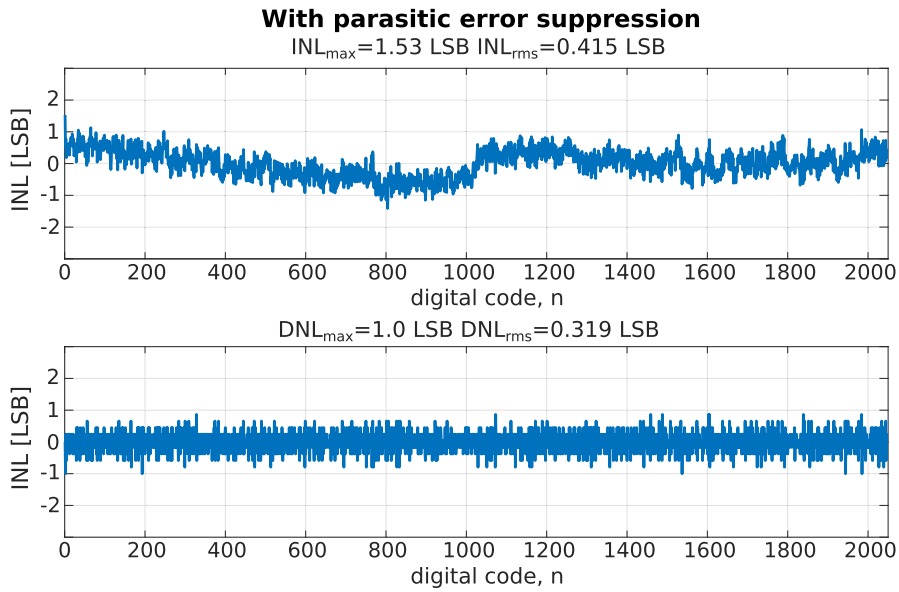
Figure 4.9: Dynamic ReDAC1 characterization with 90% swing sine wave input up to the Nyquist frequency (a) and 0.3 kHz frequency across the input swing (b).

4.3.3 ReDAC2 characterization

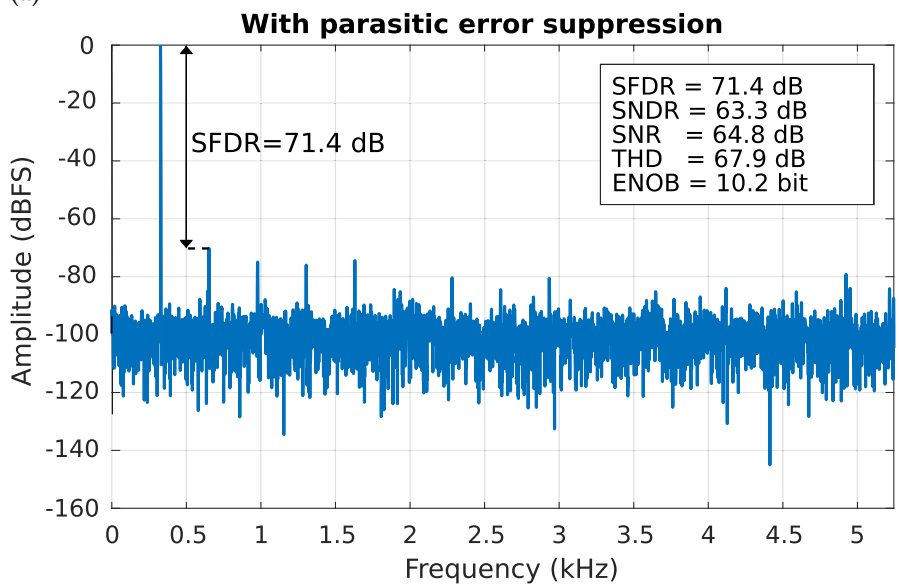
Static and single frequency dynamic characterization of ReDAC2, featuring the parasitics error suppression technique, operating at 11 bit resolution 10.5 kS/s sample rate, is reported in Fig. (a) and (b) respectively

The maximum (rms) INL is found to be 1.53 LSB (0.415 LSB) while the maximum (rms) DNL is 1.0 LSB (0.319 LSB). Dynamic characterization for a 90% swing 330 Hz input sine wave reports 71.4 dB SFDR, 67.9 dB THD, 64.8 dB SNR and 63.3 dB of SNDR, equivalent to 10.2 effective bits (ENOB).

Figure (a) reports the ReDAC2 dynamic characterization in frequency for input sine waves having constant amplitude (90% of full swing) under varying frequency while Fig. (b) shows the dynamic characterization at constant sine frequency (1.5 Hz) ranging in the ReDAC swing, both revealing consistent ReDAC operation up to Nyquist and over the whole input swing.

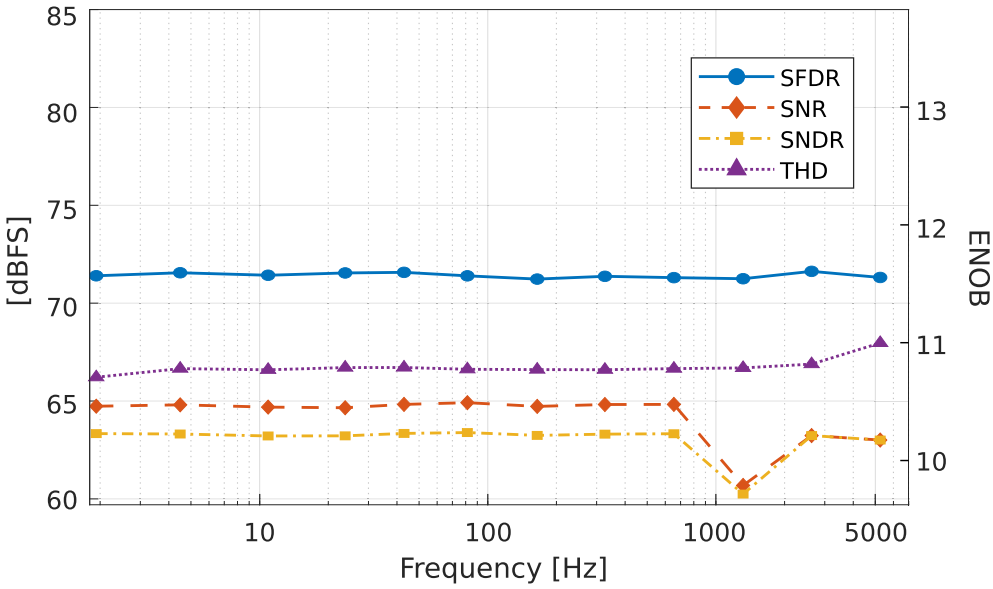


(a)

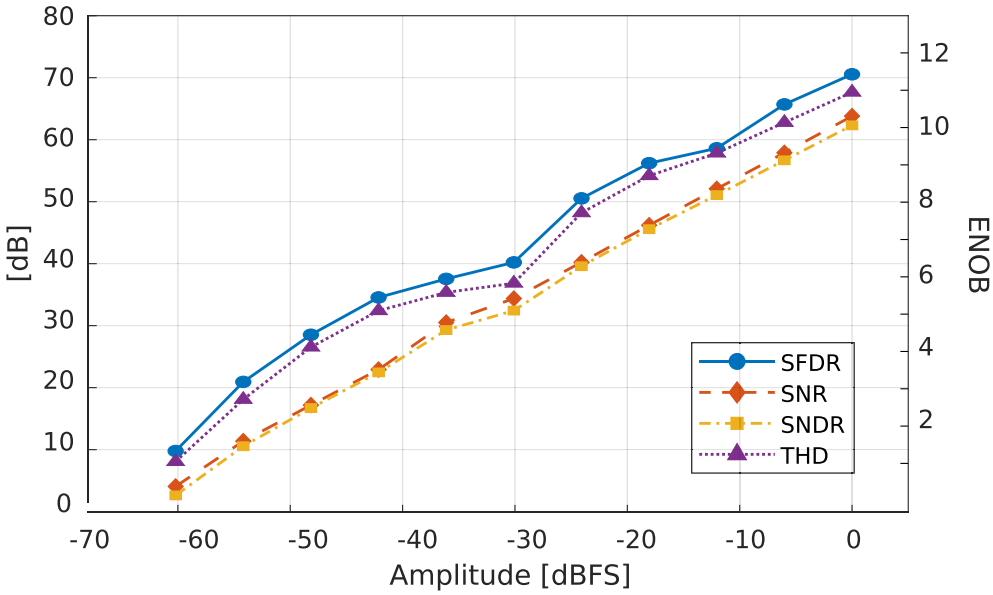


(b)

Figure 4.10: ReDAC2 static (a) and single frequency dynamic (b) characterization, 90% swing 330 Hz.



(a)



(b)

Figure 4.11: Dynamic ReDAC2 characterization with 90% swing sine wave input up to the Nyquist frequency (a) and 1.5 kHz frequency over the input swing (b).

4.3.4 Comparison

The FPGA ReDAC implementations presented in the previous sections are compared to other FPGA-based D/A converters and previously reported ReDAC implementations (both integrated and on FPGA).

Compared to previously reported ReDAC implementations, the FPGA-based ReDAC1 reports the better effective resolution thanks to the parasitics error suppression strategy, 4.47 more ENOB at 1.7× the sample rate compared to the first reported FPGA prototype in [30]. At the same time, ReDAC1 achieves 1.7 and 2.2 more ENOB with respect to simulated static performance in 40 nm CMOS implementations of [81] and [87] respectively, which although achieve 778× and 3,112× higher sample rate.

Comparing ReDAC1/ReDAC2 to other bitstream-based DACs implemented on FPGA, the ReDACs have a resource footprint of only 6 logic elements on FPGA, 8.8× and 2,237× smaller than a DDPM [31] and a ΣΔ [104] DAC respectively, in which the digital calibration footprint is not included for fair comparison, making the Relaxation Digital-to-Analog Converter (ReDAC) attractive in very low cost applications and where (possibly) more instance of the DAC are required.

Compared to DPWM DAC [97], the ReDAC1(ReDAC2) achieve considerably better accuracy quantifiable in +3.6 (+2.2) ENOB, even if operating at 334× (16.4×) smaller sample rate. The DPWM and two-segment double-slope calibrated DDPM [86] sample rates are comparable but require 2^N pulses for the single conversion, as opposed to $N+2$ pulses of the ReDACs, suggesting a non negligible energy saving of the Relaxation Digital-to-Analog Converter (ReDAC) (even if it can not be measured directly on the FPGA board).

It needs to be noted that, even though the reported performance of the ΣΔ DAC [104] seem considerably better in terms of ENOB, the comparison is not fair since the results in [104] lack a complete analog characterization and are obtained by FFT of the digital output stream.

Comparing ReDAC1 (ReDAC2) with a second order 16 bit ΣΔ implemented on comparable FPGA hardware which analog output is suitably characterized by a spectrum analyser, the Relaxation Digital-to-Analog Converter (ReDAC)s achieve +2.4 (+1.0) ENOB and comparable FPGA resources requirement.

Table 4.1: DAC Performance Comparison

	Units	[97]	[100]	[104]	[31]	[86]	[30]	[81]	[87]	**This Chapter**	
Type		PWM	$\Sigma\Delta$	$\Sigma\Delta$	DDPM	DDPM	ReDAC	ReDAC	ReDAC	ReDAC1	ReDAC2
Valid.		Meas.	Meas.	Sim.[a]	Meas.	Meas.	Meas.	Sim.	Sim.	Meas.	
Techn.	nm	FPGA	FPGA	FPGA	FPGA	40	FPGA	40	40	FPGA	
R	kΩ	N/A[b]	N/A	0.1	180	300	100	288	128	180	4.7
C	pF	N/A[b]	N/A	80,000	1,000	5	2,200	1	0.45	1,000	2,200
Area	μm^2	N/A	N/A	N/A	N/A	270	N/A	910	677	N/A	
Logic Elements		N/A	87	13,426	53	N/A	N/A	N/A	N/A	6	6
Logic Elements (cal.)		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	105	105
Resolution	bit	N/A	16	24	16	12	10	10	10	13	11
Sample Rate	kS/S	172	20	44.1	1.525	110	0.3	400	2,000	0.514	10.5
OSR		Nyq.	50	128	Nyq.	Nyq.	Nyq.	Nyq.	Nyq.	Nyq.	
$\mathrm{INL_{max}}$	LSB	N/A	N/A	N/A	13	3	2.4	0.33	0.72	1.68	1.53
$\mathrm{INL_{rms}}$	LSB	N/A	N/A	N/A	N/A	1	0.9	0.10	0.34	0.417	0.415
$\mathrm{DNL_{max}}$	LSB	N/A	N/A	N/A	1	1	3.3	0.2	1.27	1.54	1.0
$\mathrm{DNL_{rms}}$	LSB	N/A	N/A	N/A	N/A	0.47	0.62	0.01	0.07	0.299	0.319
SNDR (Low Freq.)	dB	50	57.3	N/A	N/A	71.6	43.27	61.0	58.3	71.3	63.3
SNDR (Nyq.)	dB	< 10	N/A	N/A	N/A	35	N/A	N/A	N/A	72.3	63.01
SFDR	dB	37	78	N/A	N/A	85	51.36	76.8	62.4	79.7	71.4
THD	dB	N/A	63.7	N/A	N/A	85	47.52	66.7	62.2	76.4	67.9
SNR	dB	57	58.5	141	N/A	75	44.66	66.7	62.2	72.9	64.8
ENOB	bit	8	9.2	23.4	12.1[c]	11.6[c]	7.13	9.9	9.4	11.6	10.2
Calibration		No	No	N/A	Manual[c]	Manual[c]	Manual	Manual	Auto	Auto	

[a]Measurements performed on the digitally acquired bitstream, not comparable with a true analog characterization.
[b]Second-order Sallen-Key filter used.
[c]Double-slope error calibration considered for comparison, higher effective resolution requires more complex 8-segment calibration.

Chapter 5

180 nm ReDAC with Radix-Based Digital Correction and Digital Self-Calibration

Fifth chapter addresses a self-calibration ReDAC solution not relying on clock tuning to enforce ReDAC linearity, and it is based on the algorithmic translation of the digital code from base 2 to the generic radix r for which the converter operates linearly. The approach, already exploited in literature to compensate mismatch in two-capacitors serial DACs, is here accompanied by a novel calibration strategy, which requires simpler yet effective hardware to find the optimal radix. The architecture digital architecture and layout is exposed and performance validated by simulations in 180 nm CMOS technology.

5.1 Motivation

In the previous chapters the Relaxation Digital-to-Analog Converter has been presented as an effective bitstream-based digital implementation of

the D/A conversion function.

As introduced in Chapter 2, the ReDAC linearity depends on a single condition (2.4) to be guaranteed between the clock period driving the digital bitstream and the time constant of the RC network at the ReDAC output.

To meet (2.4) the clock period needs therefore to be tuned manually [30] or automatically by digital self calibrations employing a voltage controlled oscillator (VCO) [87] (see Chapter 3) or by digital clock dividers (see Chapter 4).

In many digitally-intensive applications the tuning of the clock period may be impractical or undesirable, therefore impairing the use of the aforementioned methods. The need for a clock-indifferent ReDAC linear operation arises and was addressed in [106] for the first time by exploiting the Radix-Based Digital Correction (RBDC) technique which is also discussed in the present chapter.

5.2 Radix-Based Digital Correction

5.2.1 Clock Errors and ReDAC Radix

It is recalled from Chapter 2 that, imposing $T = \tau \log 2 = T^*$ (2.4), the ReDAC implements the linear relation between the digital input code n and the analog output V_{DAC}:

$$v_{\mathrm{C}}(NT^*) = \frac{V_{\mathrm{DD}}}{2^N} \sum_{i=0}^{N-1} b_i 2^i = V_{\mathrm{DAC}}(n).$$

If (2.4) is not met, the ReDAC voltage becomes proportional to a different binary code, weighted with respect to the generic radix $r = e^{T/\tau} \neq 2$:

$$v_C(NT) = \frac{V_{\mathrm{DD}}}{2^N} G \sum_{i=0}^{N-1} b_i r^i \tag{5.1}$$

equivalent to the relation holding in two-capacitor (two-cap) DACs in the presence of capacitors mismatch [107], being $G = \frac{2^N}{r^N}(r-1)$ a gain factor.

When the code is expressed in the conventional radix-2 and (2.4) is not satisfied, the ReDAC presents a nonlinearity which is maximum at half swing and proportional to the clock error as expressed by (2.10) in Chapter 2.

Linear operation can be regained at fixed clock frequency by translating the radix-2 binary code into the appropriate radix-r binary code by a

digital pre-processing algorithm, analogous to the one proposed in [107] to compensate capacitor mismatch errors [108]–[110] in two-cap DACs.

The radix-correction algorithm needs to be combined with a digital foreground calibration to estimate numerically the value of the optimal radix r_o, expressed analytically as

$$e^{-\frac{T}{\tau}} = \frac{1}{r} \qquad \Longrightarrow \qquad r = r_o = e^{\frac{T}{T^*}\log 2}. \tag{5.2}$$

Differently from [107], in which a bulky $\Delta\Sigma$ acquisition of capacitor mismatch is employed to estimate the optimal radix, an approach similar to what presented in Chapters 3 and 4 [87], [105] is here exploited to estimate r_o by simple hardware.

5.2.2 Radix-Based Digital Correction

According to 5.1, linearity is achievable even disregarding the constraint (2.4), given that the optimal radix is known and the binary code is converted from radix-2 to radix-r according to (5.2).

Given the generic radix-r, a binary radix-2 digital code D_2 can be translated into its corresponding radix-r code D_r expressed on M-bits by a SAR-like algorithm presented in [107] according to the flow graph in Fig. 5.1. In the beginning of the RBDC digital code translation, register D_2 stores the radix-2 code to be corrected and the index i set to the MSB, i.e. $i = M - 1$. In each flow graph loop D_2 is compared with a power of the radix r^iG and the comparison result resolves the ith bit of the radix-r code D_r.

The register D_2 is then updated with the residue of the comparison $D_2 - r^iG$ if $D_2 < r^iG$ or kept constant in the case $D_2 \geq r^iG$. The index i is then decremented and a new iteration starts until $i = 0$ and all the beets have been resolved. The value stored in D_r at the end of the radix correction corresponds to the radix-r representation of the code D_2.

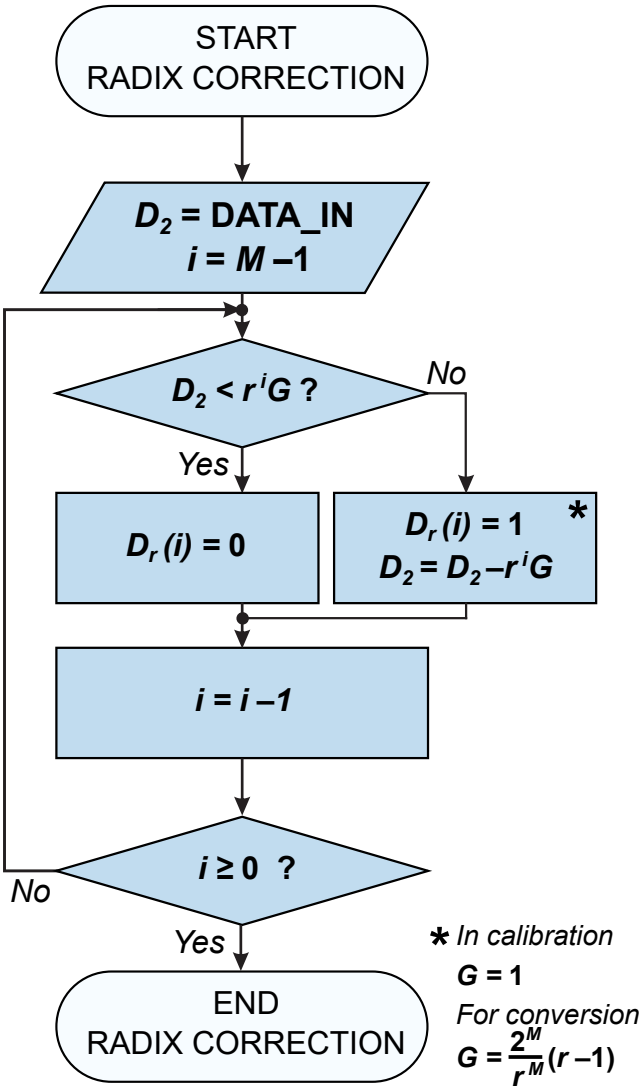


Figure 5.1: Flow diagram of the SAR-like Radix-Based Digital Correction algorithm.

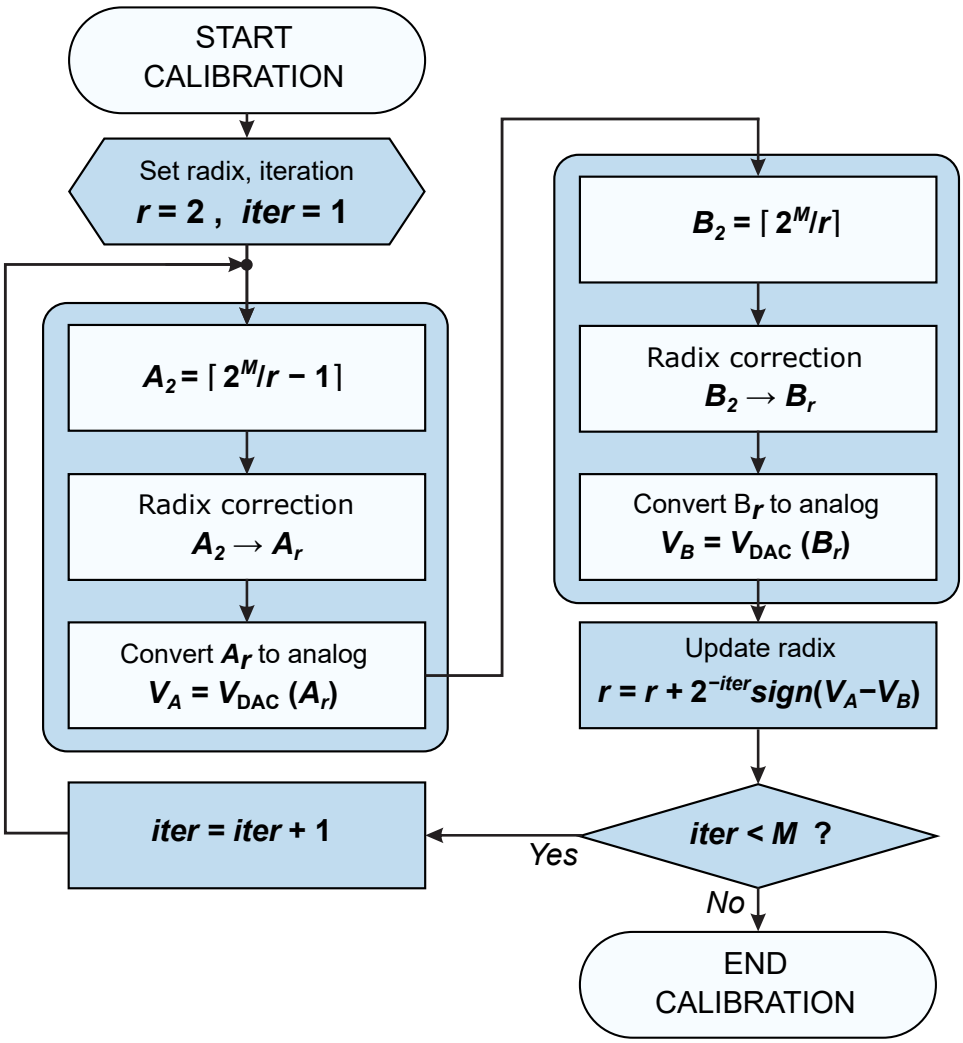


Figure 5.2: Flow diagram of the radix-based DAC calibration.

5.2.3 Radix-Based Calibration

To effectively get linear operation from the RBDC, the radix $r = r_o$ of (5.2) has to be known in advance or estimated.

Contrary to the $\Delta\Sigma$ ADC proposed in [107] to compute the optimal radix in two-capacitor DACs a simpler solution is proposed for the ReDAC estimation of r_o, generalizing the strategy exploited in [87], [105].

Extending the considerations exposed in Chapter 2, where the maximum nonlinearity is found between codes 2^{N-1} and $2^{N-1} - 1$ when $T \neq T^\star$, nonlinear error is maximum between codes $A_2 = \lceil 2^N/r - 1 \rceil$ and $B_2 = \lceil 2^N/r \rceil$ when $r \neq r_o$, as observable in Fig. 5.3.

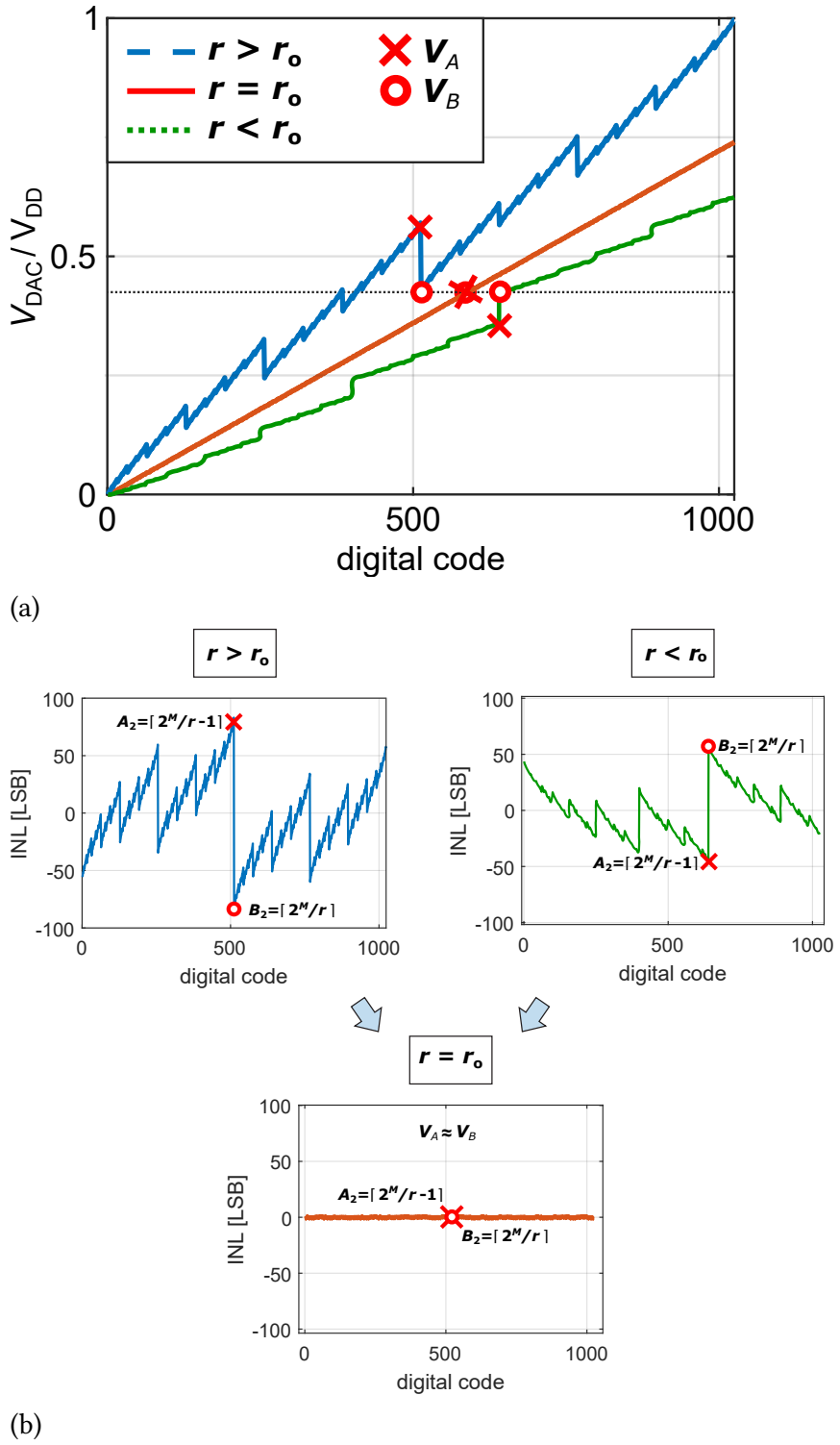


Figure 5.3: ReDAC swing (a) and nonlinearity (b) related to the radix-r digital code representation for $r < r_o$, $r = r_o$ and $r > r_o$.

The difference between the output voltages $V_A = V_{\mathrm{DAC}}(A_2)$ and $V_B = V_{\mathrm{DAC}}(B_2)$ is monotonically increasing with r, positive for $r > r_{\mathrm{o}}$ and negative for $r < r_{\mathrm{o}}$.

This behaviour is exploited to estimate r_{o} implementing a self calibration strategy similar to the one in [87], [105] by tuning, in place of the clock period, the radix r used in the radix-based correction of Section 5.2.2 depending on the sign of $V_{\mathrm{A}} - V_{\mathrm{B}}$, until the condition $V_{\mathrm{A}} = V_{\mathrm{B}}$ is enforced, which is enough to keep the ReDAC INL below half LSB.

The radix-based calibration flowchart is reported in Fig. 5.2 for a generig M-bit converter. When the calibration starts, the iteration index is initialized to $iter = 1$ and the radix is set to the nominal $r = 2$. The radix-2 binary codes A_2 and B_2 are translated to their radix-r representations A_r and B_r by the RBDC algorithm of Fig.5.1 (note that $A_r = A_2$ and $B_r = B_2$ just for the first iteration). The translated codes A_r and B_r are converted into their corresponding voltages V_{A} and V_{B}, and the estimated radix-r value updated dichotomously at each iteration *iter* based on the sign of V_{A} - V_{B}:

$$r = r + 2^{-iter}\mathrm{sign}(V_A - V_B) \tag{5.3}$$

until $V_{\mathrm{A}} = V_{\mathrm{B}}$ with less than 1 LSB error, which is practically reached after M cycles, when all the bits have been resolved. Gain correction $G = 1 \rightarrow$ is performed before normal ReDAC operation. The ReDAC swing nonlinearity evolution during an example calibration in the presence of a 30% error on the clock period is reported in Fig. 5.4.

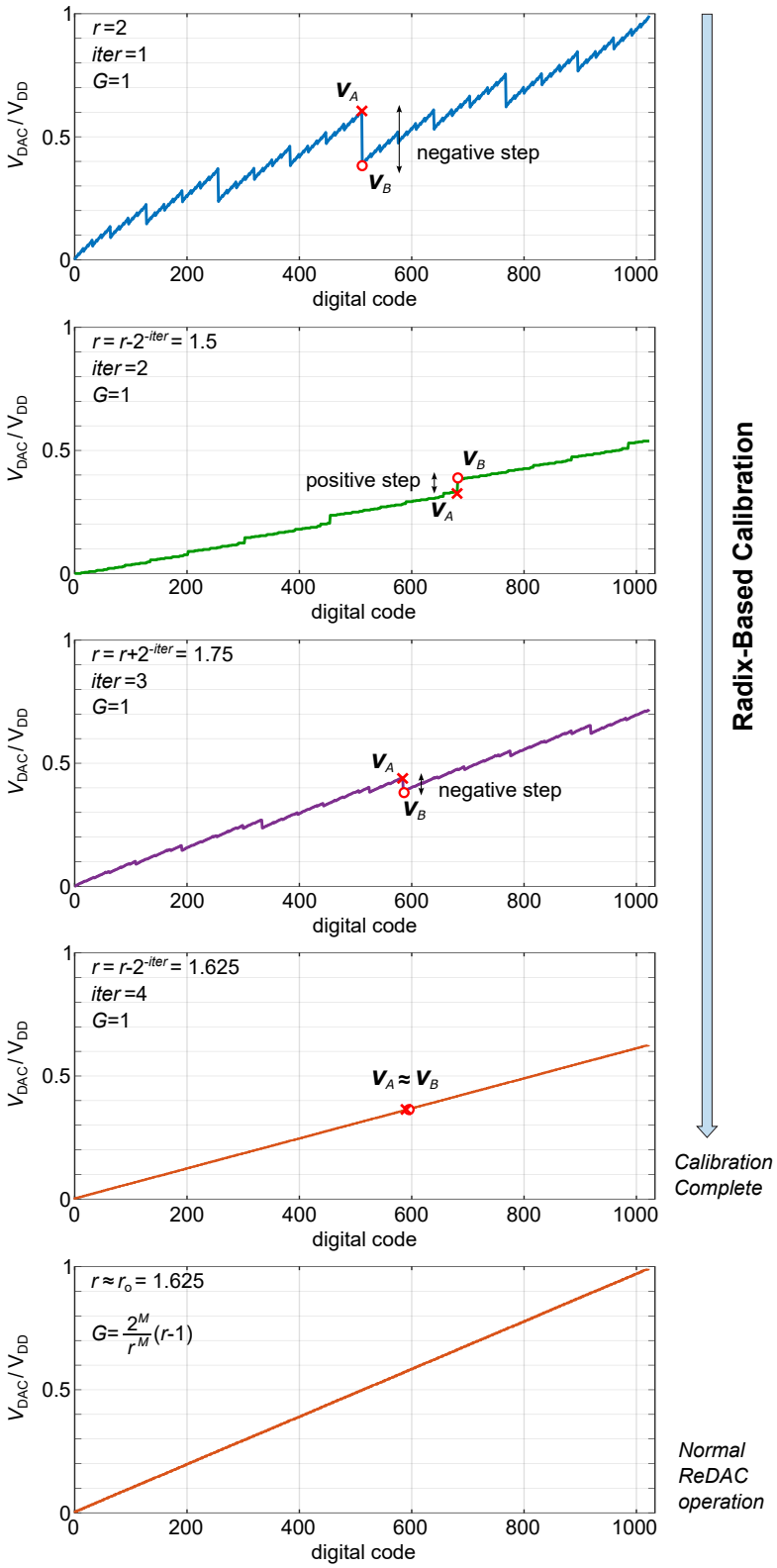


Figure 5.4: ReDAC nonlinearity evolution in an example Radix-Based Calibration lasting four iterations. Post-calibration digital gain correction is performed at the end.

5.3 Circuit Implementation

The Radix-Based Digital Correction presented so far has been designed for an integrated ReDAC for the first time [106] by the architecture in Fig. 5.5(a), consisting in a ReDAC core block (ReDAC), a Radix-Correction block implementing the digital code translation presented in Fig.5.1 and a digital Calibration estimating the optimal radix r_o following the algorithm in Fig. 5.2.

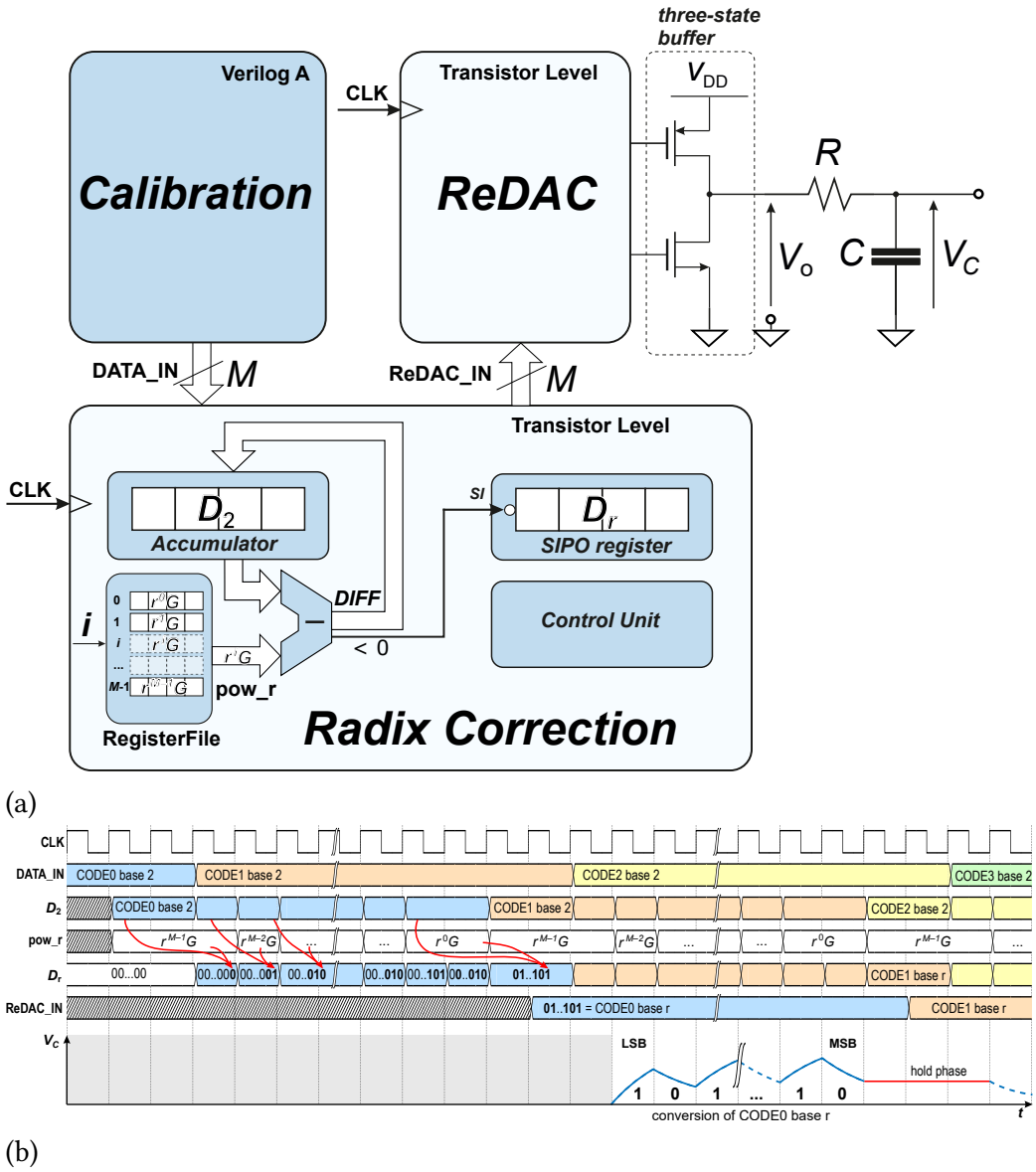


Figure 5.5: Radix-based ReDAC correction architecture (a) and radix-correction timing diagram (b).

5.3.1 Digital Architecture

The Radix-Based Digital Correction operates on two registers: the register D_2 stores the initial radix-2 data to be converted as well as the comparison residues in each radix correction cycle. The register serial-in-parallel-out (SIPO) register D_r is updated according to the results of the correction. The RBDC block also includes a logic subtractor and a register file storing the powers r^iG required by the correction algorithm.

The radix correction execution is governed by a finite-state machine (FSM) Control Unit according to the timing diagram of Fig. 5.5, implementing the algorithm in Fig. 5.1 and described in what follows.

When the radix correction begins, the input code to be translated is loaded in the register D_2, setting the internal counter i to the MSB: $i = M-1$. The subtractor performs the difference between the register D_2 and the value value r^iG currently indexed in the register file.

The sign of the difference $DIFF = D_2 - r^iG$, corresponding to the MSB of the two's complement of the subtractor is serially-input to D_r, resolving the ith bit of the radix-corrected code. At the same time D_2 is updated with the value of $DIFF$ in the case of $DIFF \geq 0$, kept constant otherwise ($DiFF < 0$).

The indexing counter i is decremented and a new cycle begins until $i = 0$ (i.e. all the bits of D_r are resolved). The value in D_r is sampled on ReDAC_IN to be converted by the ReDAC, meanwhile a new radix-correction cycle starts processing the next digital code, effectively achieving continuous D/A operation in a pipelined fashion of subsequent correction-and-conversion sequences, as highlighted in Fig. 5.5(b).

5.3.2 Digital Calibration Operation

In order to estimate the radix value based on the calibration flow in Section 5.2.3 the Calibration block is introduced, to estimate r_o in foreground (disabled in normal ReDAC operation).

The Calibration drives the ReDAC across the M steps in Fig. 5.2 providing the codes $A_2 = \lceil 2^M/r - 1 \rceil$ and $B_2 = \lceil 2^M/r \rceil$, whose converted voltage difference corresponds to the maximum nonlinearity step. Depending on the sign of $V_A - V_B$, which can be evaluated e.g. by VCO-based ADC [87] as in Chapter 3 or single slope A/D conversion [105] as in Chapter 4, the radix r is updated.

At each calibration iteration, when r is updated, the Calibration block also updates the register file storing the powers r^iG of the current radix, as needed by the Radix-Correction block.

5.4 Validation

A Relaxation Digital-to-Analog Converter featuring the Radix-Based Digital Correction technique has been designed in a 180 nm CMOS technology targeting 10 bit resolution and validated by transistor level simulations. The ReDAC is designed according to the indications provided in Chapter 2, resulting in a Metal-insulator-Metal (MiM) capacitor $C = 450\,\text{fF}$ and a high-res poly resistor $R = 140\,\text{k}\Omega$ ($\tau = 63\,ns$). The ReDAC core block and the RBDC have been designed and synthesized starting from VHDL and simulated at transistor level under 0.55 V supply, while the custom three-state buffer driving the RC is operated at 0.7 V. The circuit layout as shown in Fig. includes the RC network driven by the three-state buffer (1,080 μm^2), the ReDAC core (1,890 μm^2) and the Radix-Based Correction block (10,620 μm^2) summing up to a total area of 13,590 μm^2.

The Calibration block of Section 5.3.2 is behaviourally simulated in a Verilog-A block. It can be conveniently implemented in a system by a microprocessor or a DSP, and includes the network to perform the comparison of V_A and V_B, which can be implemented by simple voltage-to-time-to-digital conversions [87], [105].

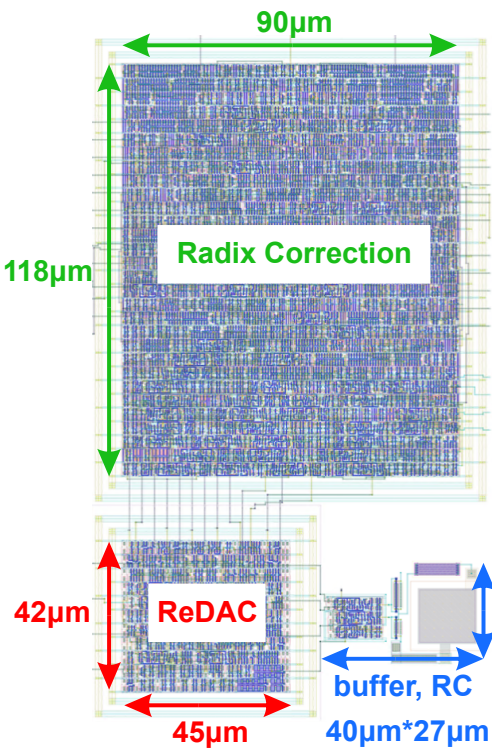


Figure 5.6: ReDAC cith Radix-Based Digital Correction Layout in 180 CMOS.

5.4.1 Performance Evaluation

To validate the effectiveness of the Radix-Based Digital Correction, 180 nm CMOS transistor level simulations of the same design with and without the radix correction have been performed, starting from a 16% deviation of the clock period T from the one $T^* = 43\,ns$ required by (2.4) to have linear conversion of radix-2 digital codes.

The considerably large error takes into account by far the process variations in the RC time constant and in the reference frequency produced by a reduced cost and power relaxation oscillator.

The capacitor voltage waveform during calibration is shown in Fig. validating the effectiveness of the calibration, enforcing the equality of V_A and V_B corresponding to the converted codes $A_2 = \lceil 2^M/r - 1 \rceil$ and $B_2 = \lceil 2^M/r \rceil$ respectively.

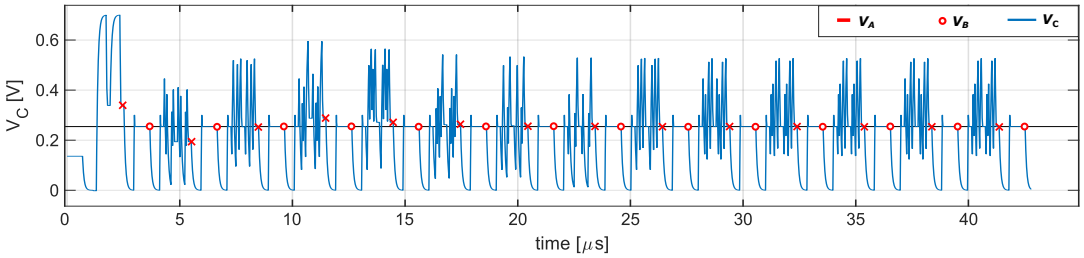
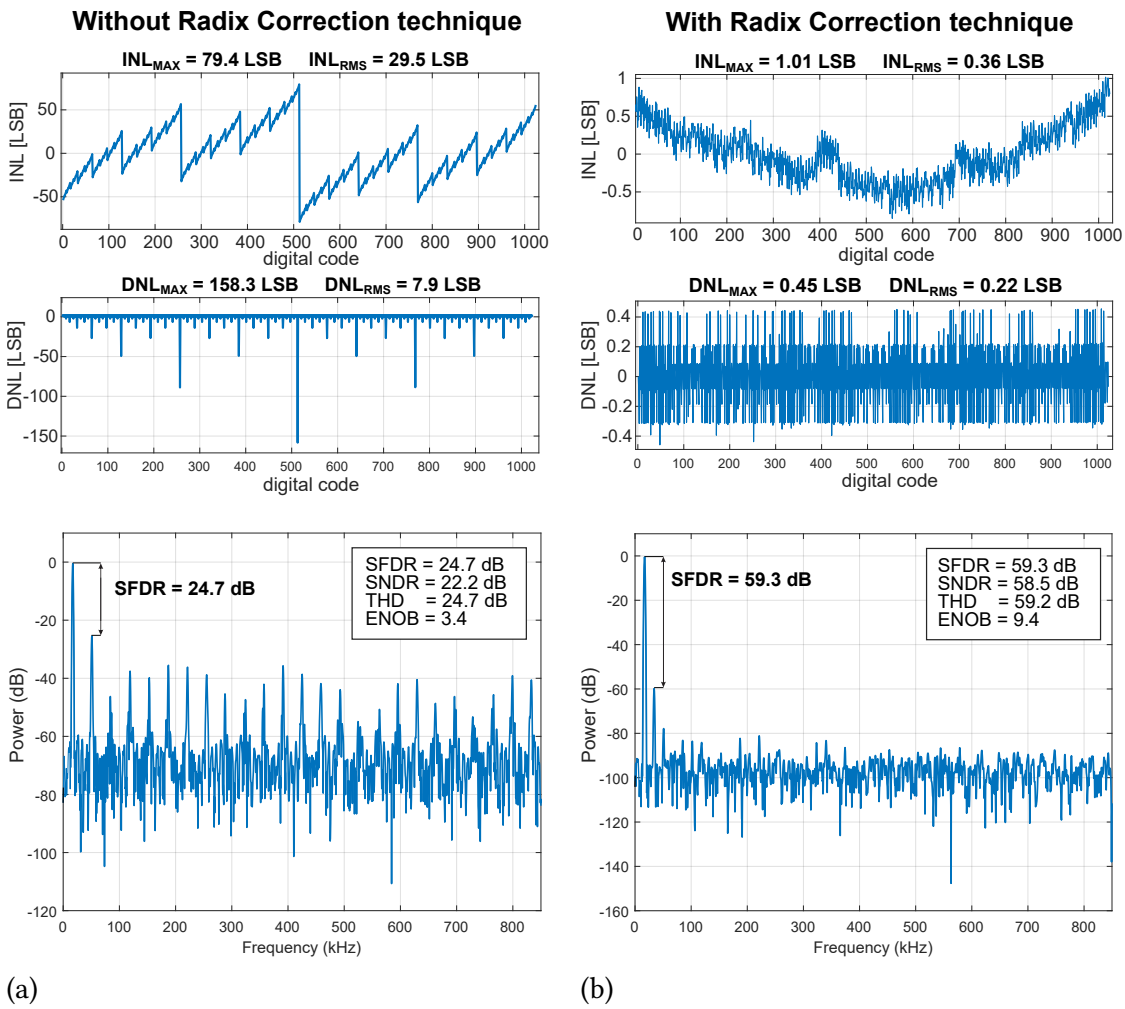


Figure 5.7: RBDC ReDAC calibration waveforms, showing the convergence of V_A and V_B.

ReDAC performance without and with the Radix-Based Digital Correction are reported in Fig. 5.8(a) and Fig. 5.8(b) respectively. It can be noted a drastic improvement in the maximum (rms) INL from 79.4 LSB (29.5 LSB) to 1.01 LSB (0.36 LSB) and maximum (rms) DNL from 158.3 LSB (7,9 LSB) to 0.45 LSB (0.22 LSB).

Dynamic performance characterization at single full-swing sine wave, 17 kHz, corresponding to 1% of the sampling frequency are reported in Fig. 5.8 as well. Simulations reveal for the RBDC ReDAC an SFDR of 59.3 dB, a THD of 59.2 dB and an SNDR of 58.5 dB, equivalent to 9.4 ENOB, achieving 6 effective bits more than the ReDAC not employing the radix-based correction, reporting an SFDR of 24.7 dB, a THD of 24.7 dB and a SNDR of 22.2 dB, corresponding to 3.4 ENOB.

The power footprint of the different blocks is 0.94 µW for the RC network, 0.91 µW for the ReDAC core and 7.3 µW for the Radix Correction block. The total energy per conversion is thus 5.38 pJ with a sample rate of 1.7 MS/s, corresponding to a Figure of Merit (FOM) of 9.21 fJ/conv-step for the RBDC ReDAC.



(a) (b)

Figure 5.8: ReDAC performance compaison with (a) and without (b) RBDC in the presence of a 16% clock frequency error.

5.4.2 Comparison

The Relaxation Digital-to-Analog Converter implementing the proposed Radix-Based Digital Correction technique is compared in 5.1 with ReDAC works relying on clock tuning for linear operation [30], [81], [87], [105] (see Chapter 3, Chapter 4).

The proposed RBDC properly meets expected performance compared to ReDACs in [30], [81], [87], [105], avoiding the need of frequency tuning itself. The presented radix correction Calibration trades the tuning of an analog quantity with a digital one, in practice resulting in a power overhead of 7.3 μW due to the digital Radix-Correction block (7.8× the analog-only ReDAC power).

The direct advantage of the digital radix-based architecture is that it inherently scales in smaller technology nodes without analog re-design effort. It is estimated that porting the design in, e.g. 40 nm CMOS, the switching radix correction power reduces by 20×, becoming a non-dominant contribution with respect to the analog power.

Table 5.1: DAC Performance Comparison

	Units	[30]	[81]	[87]	[105]	**This Chapter**
Valid.		Meas.	Sim.	Sim.	Meas.	Sim.
Techn.	nm	FPGA	40	40	FPGA	180
Supply	V	3.3	0.6	0.6	3.3	0.7/0.55
Power	μW	N/A	0.44	1.46	N/A	9.15
R	kΩ	100	288	128	4.7	140
C	pF	2,200	1	0.45	2,200	0.45
Area	μm^2	N/A	910	677	N/A	13590
Res.	bit	10	10	12	11	10
Samp. Rate	kS/S	0.3	400	2,000	10.5	1,450
$\mathrm{INL_{max}}$	LSB	2.4	0.33	0.72	1.53	1.01
$\mathrm{INL_{rms}}$	LSB	0.9	0.10	0.34	0.415	0.36
$\mathrm{DNL_{max}}$	LSB	3.3	0.2	1.27	1.0	0.45
$\mathrm{DNL_{rms}}$	LSB	0.62	0.01	0.07	0.319	0.22
SNDR	dB	43.27	61.0	58.3	63.3	58.5
SFDR	dB	51.36	76.8	62.4	71.4	59.3
THD	dB	47.52	66.7	62.2	67.9	59.2
ENOB	bit	7.13	9.9	9.4	10.2	9.4
FOM	fJ/(c.s.)	N/A	1.1	1.08	N/A	9.21
Calibr.		Manual	Manual	Auto[a]	Auto[b]	Auto[c]

[a]VCO-based clock tuning, [b]Digital clock divider clock tuning, [c]Algorithmic search of radix r.

Chapter 6

Silicon Implementation of ReDACs in 180 nm CMOS

Sixth chapter presents the silicon implementation of ReDAC converters in 180 nm CMOS test chips. Two converters are integrated, operating at 880 kS/s on 10 bits and 100 kS/s on 13 bits, featuring a digital self calibration based on digitally controlled oscillator and single-slope ultra-low power A/D conversion. The complete IC architecture, including testing harness for the converters characterization, is presented. Experimental results are provided for both ReDAC designs by single-die and multi-dice validation, reporting static and dynamic performance and effective resolution under varying supply. The analytical prediction of conversion energy is validated by measurements and the converter competitive performance synthesized and compared in Figure of Merits evaluating power-performance-area.

6.1 Motivation

In Chapter 1 the need for analog and mixed signals (AMS) frontends facing the challenges of analog design in fine CMOS technology nodes, reduction of supply voltages, power and area limitations has been introduced to meet the needs of Internet of Things (IoT) and Internet of Wearables (IoW)

nodes.

In this context, circuits for acquisition and stimuli generation (i.e. D/A conversion) featuring low distortion (<1%), µW-power range and bandwidths reaching the MS/s range are required in implantable and wearable devices for neurostimulation [111], [112], electrochemical sensing by cyclic voltammetry (CV) and electrochemical impedance spectroscopy (EIS) [20] and, more generally, in IoT nodes for audio processing, auxiliary calibration DACs, threshold and reference generation [86], [113], [114].

Targeting these applications, the first silicon implementations of the Relaxation Digital-to-Analog Converter has been presented and discussed in this chapter, previously verified only on FPGA or integrated simulated architectures [30], [81], [87], [105], [106]. Two Relaxation Digital-to-Analog Converter (ReDAC) designs have been fabricated in 180 nm CMOS i.e. a single-ended (SE-ReDAC) designed for 10 bit, 880 kS/s sample rate and a differential-output (Diff-ReDAC) [115], [116] working at 13 bit 100 kS/s, as discussed in the present chapter.

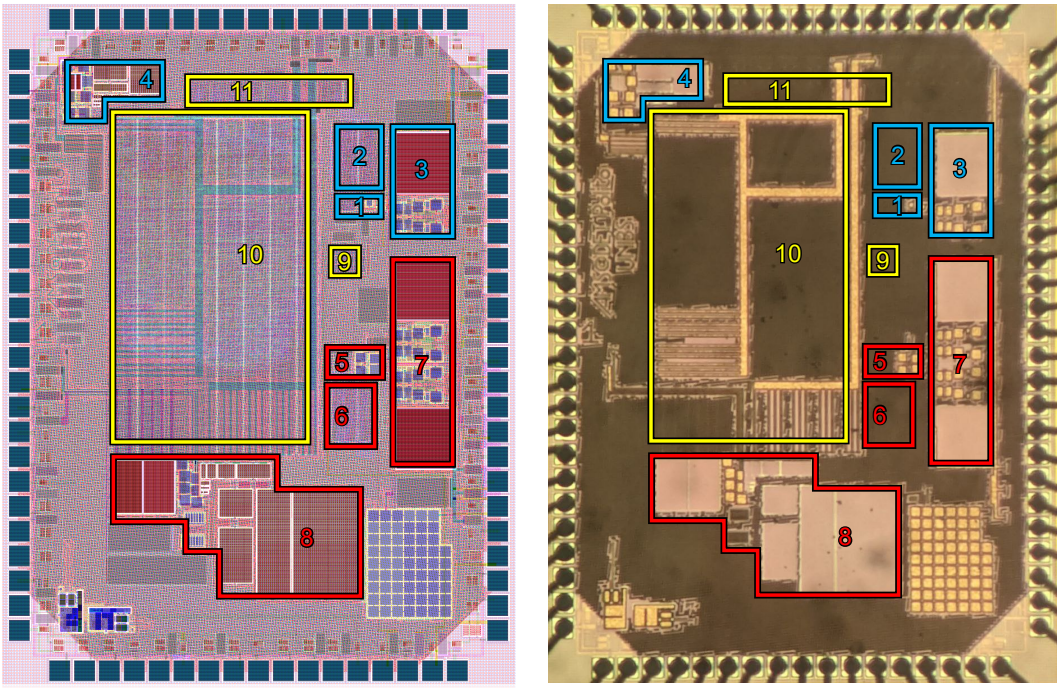
6.2 Test-Chip Architecture

The photo of the 180 nm testchip die, which is 1.5 mm wide and 2 mm high, is shown in Fig. 6.1. The integrated modules include the SE-ReDAC with related blocks (highlighted in blue), the Diff-ReDAC and related blocks (highlighted in red) and auxiliary blocks shared bewtween the two ReDACs (contoured by yellow boxes).

Each ReDAC core module is complemented by a digital calibration, performing clock tuning by means of a digitally controlled oscillator (DCO) to achieve ReDAC linearity, and a Sample-and-Hold Amplifier (SHA) to decouple the analog ReDACs outputs from the probing PADs.

SE-ReDAC and Diff-ReDAC share a ultra-low power two-transistor reference (yellow box 9), required by calibration blocks, a Direct Digital Synthesizer (box 10) to generate digital test signals to be fed to the ReDACs and a serial communication (Scanchain: box 11) to digitally control the on-chip blocks by out-of-chip testing hardware.

The detailed operation of the two ReDACs and their dedicated calibrations will be developed in Section 6.3 and 6.4, while the description of other blocks (Digital Synthesizer, DCOs, Sample-and-Hold Amplifier (SHA)s) is reported in the following sections.



SE-ReDAC related blocks
1 SE-ReDAC core (5,030 µm2)
2 Calibration (CAL) (24,800 µm^2)
3 Sample and Hold (SHA) (46,130 µm^2)
4 Digitally Controlled Oscillator (DCO1) (38,800 µm2)

Diff-ReDAC related blocks
5 Diff-ReDAC core (7,800 µm^2)
6 Calibration (CAL) (24,800 µm^2)
7 Sample and Hold (SHA) (92,260 µm^2)
8 Digitally Controlled Oscillator (DCO2) (188,600 µm^2)

Shared blocks
9 Two-Transistors Reference (REF) (7,400 µm^2)
10 Direct Digital Synthesizer (SYNT) (0.54 mm^2)
11 Scanchain (SCAN) (37,600 µm^2)

Figure 6.1: Test-chip full GDS (left) and die photo (right). The different integrated modules are highlighted in colored boxes. The legend reports the area footprint of each module in the tapeout.

6.2.1 Direct Digital Synthesizer

The Direct Digital Synthesizer is based on the architecture shown in Fig. 6.2.

Digital ramps and sinusoids at different frequencies and amplitudes can be generated by a consolidated synthesizer architecture [117]. A Phase Accumulator register indexes a read-only memory (ROM), implemented as a combinatoric lookup table (LUT), which stores the quantised samples of a quarter-wave sinusoid.

The Phase Accumulator register generates continuous sawtooth digital ramps having steps dictated by the frequency control word (FCW). The LUT-Address and LUT-Word digital buses are, respectively, preceded and followed by a Complementor, effectively exploiting the horizontal and vertical sinusoid symmetries to get a full sine wave from the quarter-wave sine stored in the LUT.

The FCW is synchronously updated at the end of each ReDAC conversion, while multiplexers redirect the digital word to be converted (Ramp or Sine) and synchronism signals (not illustrated for the sake of simplicity) to either the SE-ReDAC or Diff-ReDAC by Scanchain configuration.

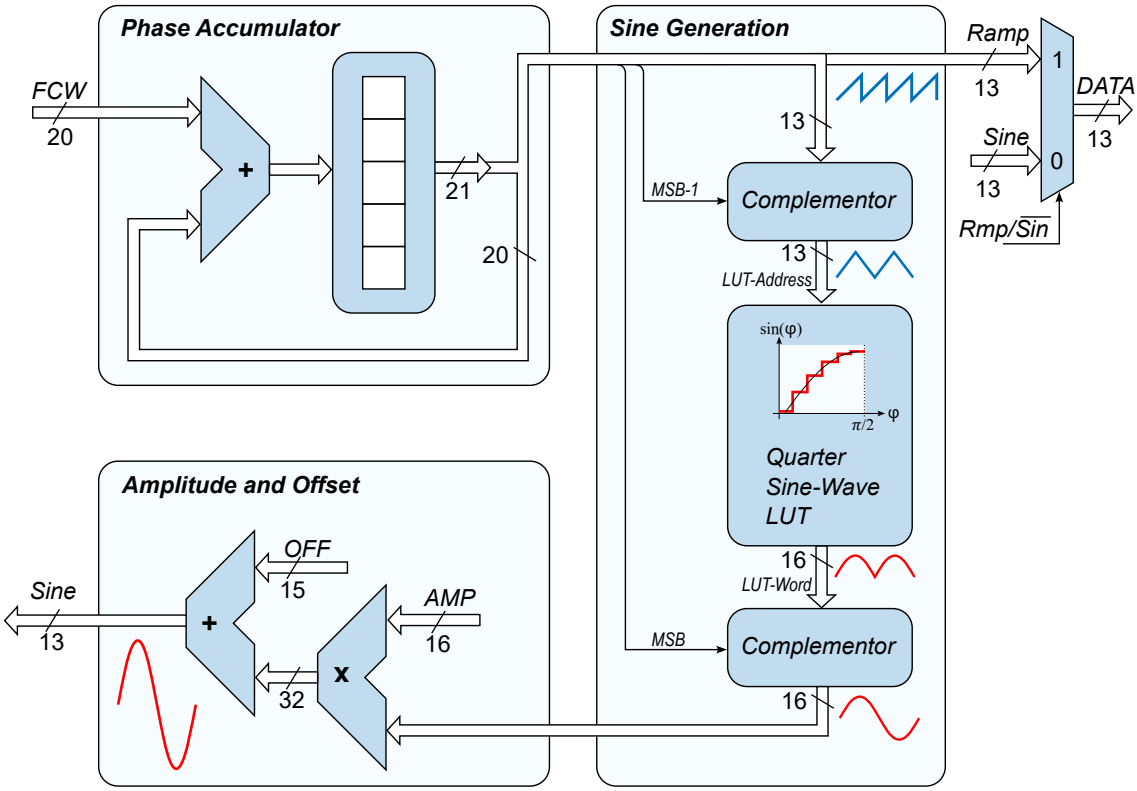


Figure 6.2: On-chip Direct Digital Synthesizer architecture (SYNT).

6.2.2 Digitally Controlled Oscillators

The two digitally controlled oscillators DCO1 and DCO2, indicated by number 4 and 8 in the die photo of Fig. 6.1, are both based on the architecture of Fig. 6.3, exploiting the well-known source-coupled relaxation oscillator topology [118], [119].

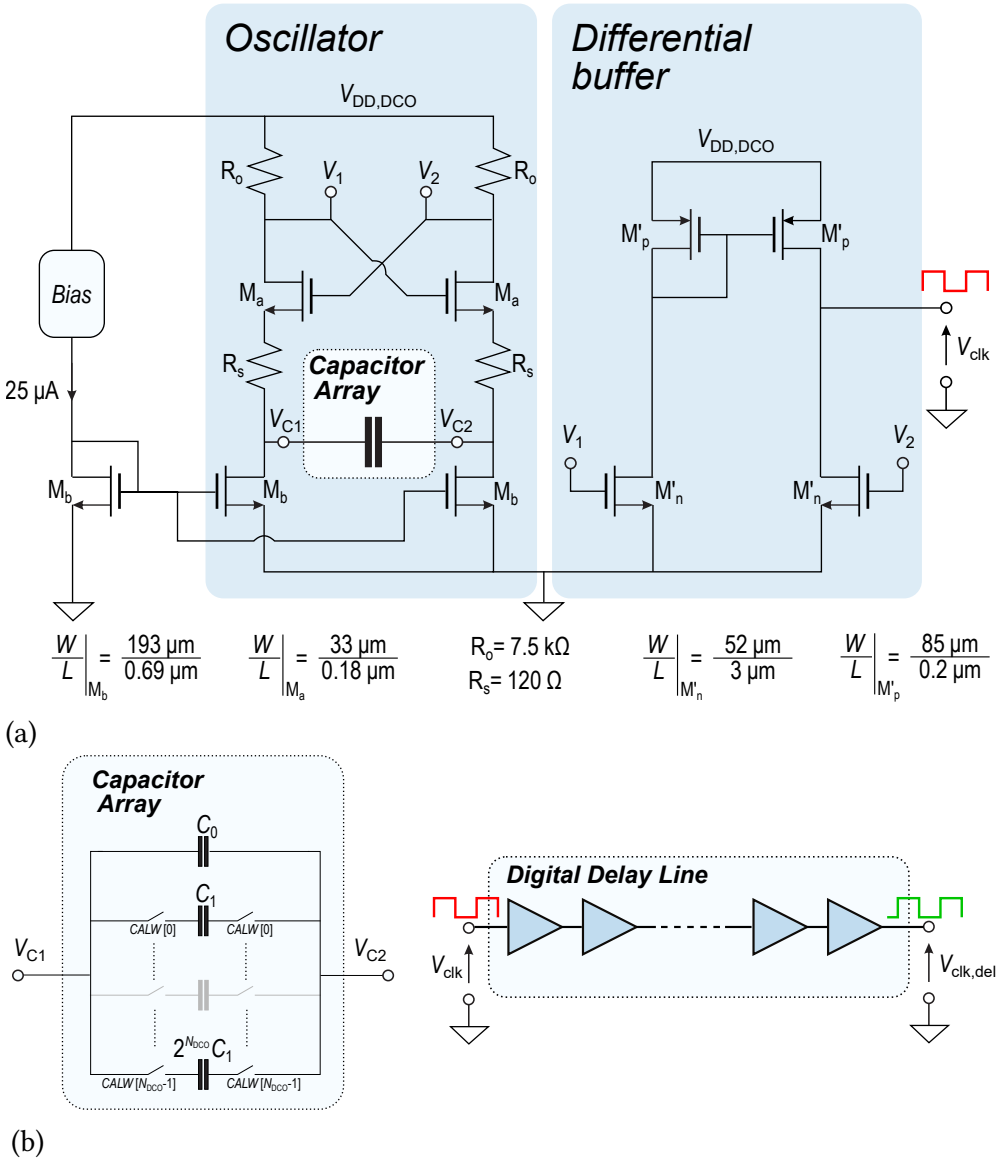


Figure 6.3: Architecture of the digitally controlled oscillators DCO1 and DCO2.

The DCO design is related to the resolution and conversion time of the SE-ReDAC (Diff-ReDAC) having $N = 10$ bit ($N = 13$ bit) and $T_{\text{conv}} = (N+3)T = 1/880\,\text{kS/s}$ ($T_{\text{conv}} = (N+2)T = 100\,\text{kS/s}$) respectively, where the +3 (+2) extra periods are dedicated to the ReDACs hold phase.

The tuning-range center period T generated by DCO1 (DCO2) is therefore designed to be close to the typical clock period $T^* = RC\log 2 = 95\,\text{ns}$ ($T^* = 670\,\text{ns}$) required by the SE-ReDAC (the Diff-ReDAC).

DCO1 (DCO2) is designed to achieve power consumption in the tens of µW, at the nominal supply of 0.7 V and verified by simulations to be 70 µW (100 µW) at the center frequency of the tuning range.

Given the ReDACs period T and target resolution N the rms jitter of the oscillators is designed to satisfy (2.23) of Chapter 2 which, in practice, translates to

$$\sigma_T \leq \frac{T}{2^{N+1}} \tag{6.1}$$

to get less than half LSB of jitter-related nonlinearity, and evaluates as $\sigma_T \leq 45\,\text{ps}$ ($\sigma_T \leq 40\,\text{ps}$) for the SE-ReDAC (Diff-ReDAC), validated by simulations to be $\sigma_T = 36\,\text{ps}$ ($\sigma_T = 32\,\text{ps}$).

The tuning range of both DCOs is designed to include the optimal period of the ReDAC in presence of process variations, as reported in the Monte Carlo process simulations of the DCO2 tuning range in Fig. .

The two DCOs, whose components size is reported in Fig. 6.3(a), differ only for the capacitor array (defining the tuning range) and an output digital delay line (see Fig. 6.3(b)).

The minimum period of the DCO1 (DCO2) tuning range is set by the always-connected floating capacitor $C_0 = 830\,\text{fF}$ ($C_0 = 11\,\text{pF}$), while the tuning range is spanned by selectively connecting the remaining $N_{\text{DCO}} = 9$ ($N_{\text{DCO}} = 12$) binary weighted capacitors $[C_1, 2C_1, ..., 2^{N_{\text{DCO}}-1}C_1]$ of the array, switchable by the bits of the tuning word CALW trough pass gates. The smallest capacitor C_1 is, in both DCOs, the minimum 6 fF allowed by the technology.

The digital delay lines are cascaded to the output of the two DCOs, and required to generate a clock *clk*, *del*, delayed by a fraction of period $T_{\text{del}} \ll T$ with respect to the *clk*, in order to implement the parasitics error suppression strategy as presented in Chapter 2.

The DCOs have been simulated to verify that the typical period T is in the tuning range under 3σ process and mismatch variations. Temperature variations of the ReDAC RC time constant are partially compensated by introducing the source degeneration R_S in the DCO crossed-couple transistors.

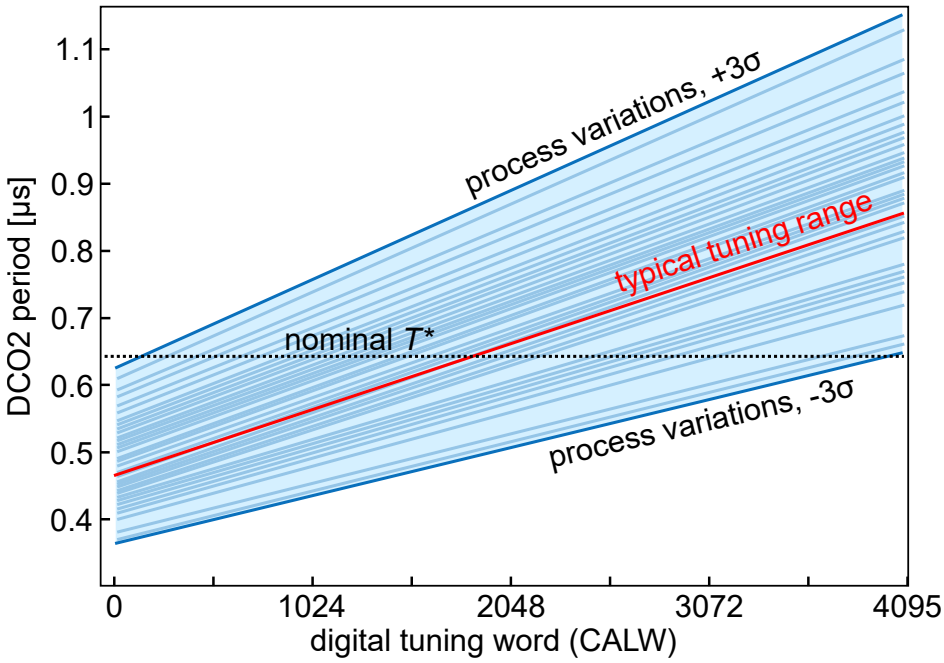
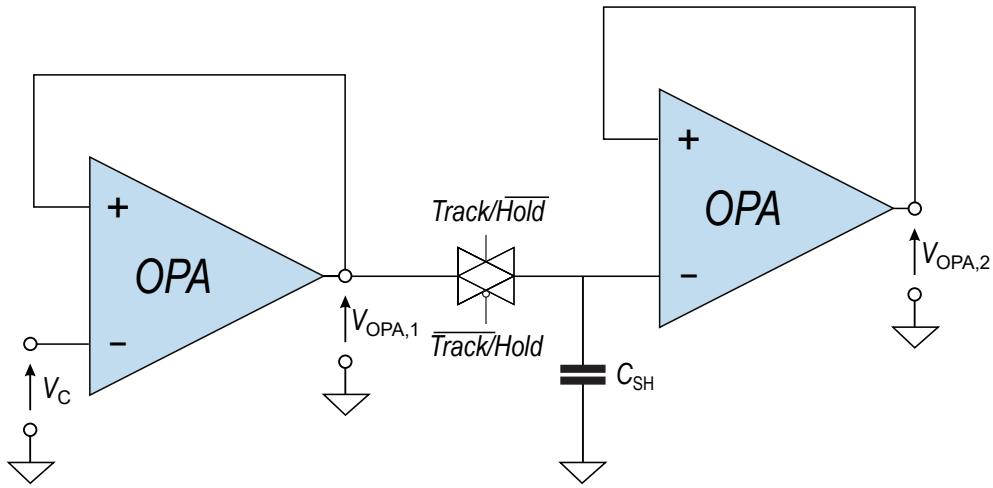
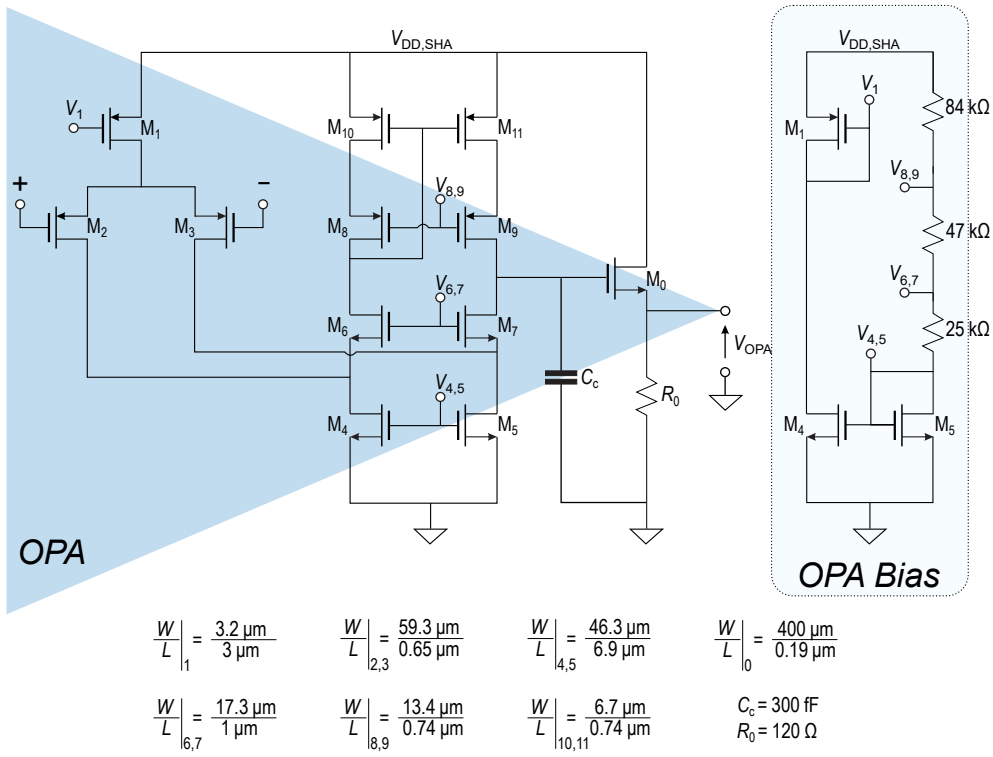


Figure 6.4: Monte Carlo Process variations of the DCO2 tuning range.



(a)



$\left.\frac{W}{L}\right|_1 = \frac{3.2\ \mu m}{3\ \mu m}$ $\left.\frac{W}{L}\right|_{2,3} = \frac{59.3\ \mu m}{0.65\ \mu m}$ $\left.\frac{W}{L}\right|_{4,5} = \frac{46.3\ \mu m}{6.9\ \mu m}$ $\left.\frac{W}{L}\right|_0 = \frac{400\ \mu m}{0.19\ \mu m}$

$\left.\frac{W}{L}\right|_{6,7} = \frac{17.3\ \mu m}{1\ \mu m}$ $\left.\frac{W}{L}\right|_{8,9} = \frac{13.4\ \mu m}{0.74\ \mu m}$ $\left.\frac{W}{L}\right|_{10,11} = \frac{6.7\ \mu m}{0.74\ \mu m}$ $C_c = 300\ fF$, $R_0 = 120\ \Omega$

(b)

Figure 6.5: Sample and hold amplifier (a) and op-amp schematic (b).

6.2.3 Sample-and-Hold Amplifiers

The Sample-and-Hold Amplifiers (SHAs) (blocks number 3 and 7 in Fig. 6.1) are based on the consolidated [28], [120] architecture in Fig. 6.5(a), employing two operational amplifiers in voltage follower configuration and a sampling capacitance $C_{SH} = 30\,\text{pF}$. The SHA input is connected to the ReDAC output capacitor probing the voltage V_C, while the SHA output $V_{OPA,2}$ is connected to an output analog PAD. The track and hold operation is triggered by the ReDACs logic trough level shifters switching the $Track/\overline{Hold}$ signal of the pass-gate.

The operational amplifiers (op-amp), based on the folded cascode [121] topology, are designed to operate at 1.8 V supply considering a worst-case 50 pF output load (compatible with the output PAD capacitance) to achieve 80 dB open-loop DC-gain (suitable to probe with appropriate DC accuracy a 13 bit DAC), a slew-rate of 18 V/μs, a gain-bandwidth product (GBW) of 26 MHz (enough to guarantee a settling time of the output voltage within half LSB in one clock period) and 62 degrees of phase margin.

The op-amp performance are verified by post-layout simulations under process and mismatch variations, resulting in a 3σ spread of the DC-gain (phase margin, GBW) of 2.1 dB (2.7 degrees, 4.7 MHz) for process, and 0.2 dB (1.2 degrees, 0.6 MHz) for matching variations.

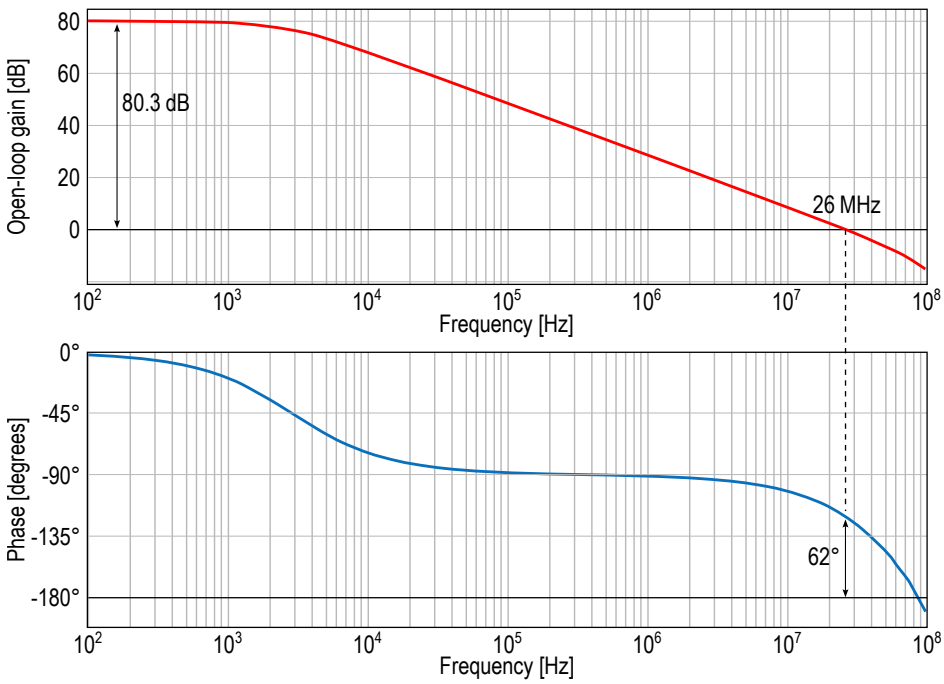


Figure 6.6: SHA op-amp post-layout simulated loop-gain in magnitude and phase.

The typical simulated post-layout op-amp loop gain in magnitude and phase is reported in Fig. 6.6, while mismatch and process-related Monte Carlo op-amp performance are shown in Fig. 6.7 and Fig. 6.8 respectively.

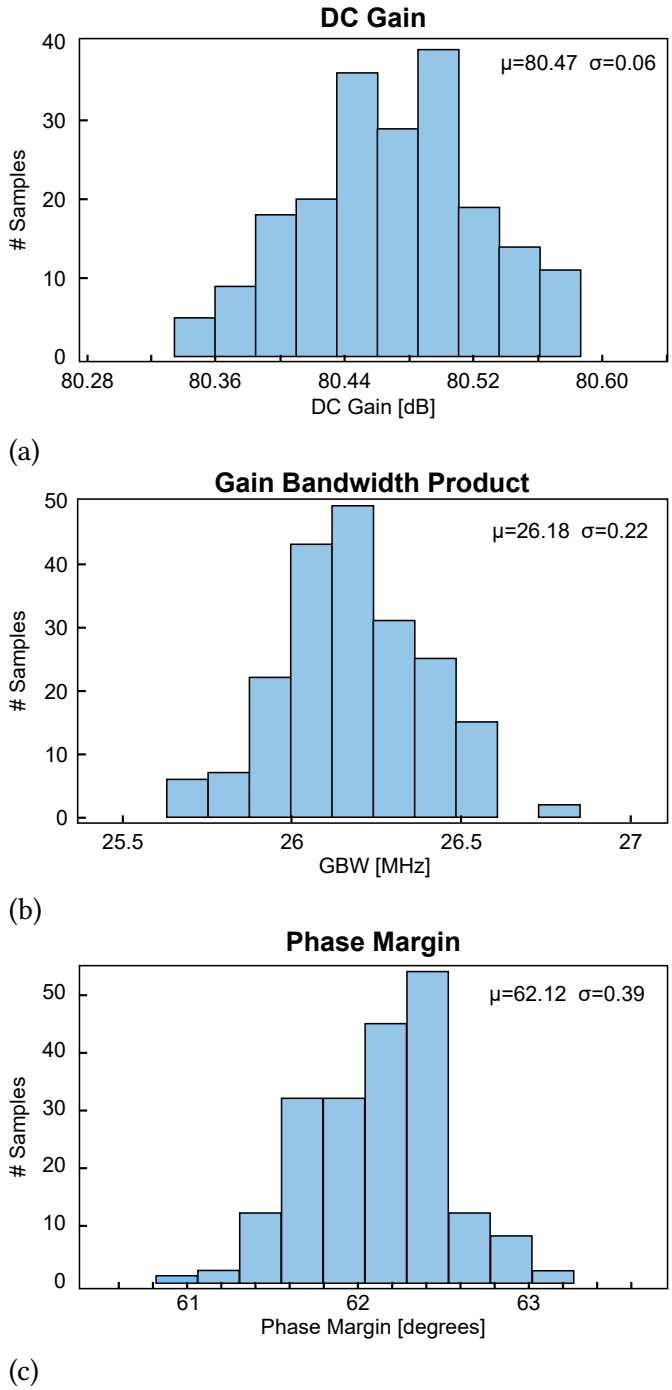


Figure 6.7: Monte Carlo mismatch-related simulated performance of the SHA op-amp open loop gain (a) gain-bandwidth (b) and phase margin (c).

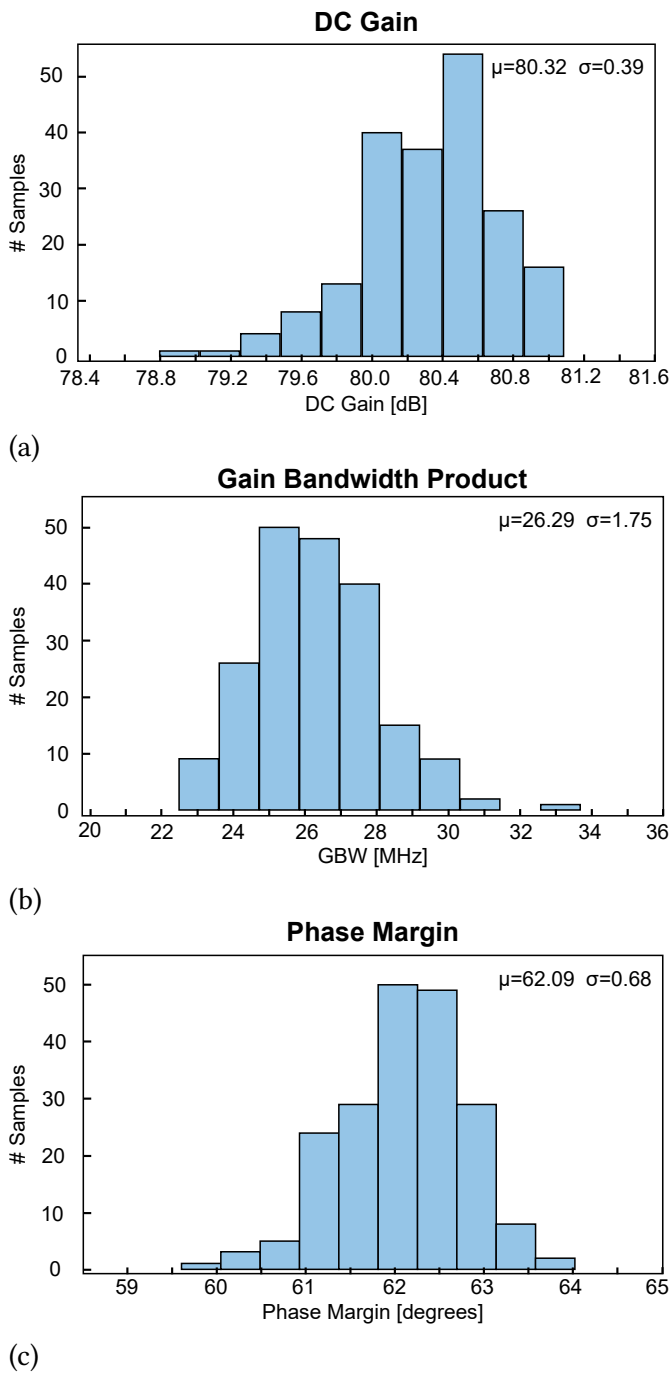


Figure 6.8: Monte Carlo process-related simulated performance of the SHA op-amp open loop gain (a) gain-bandwidth (b) and phase margin (c).

6.3 Single-Ended ReDAC (SE-ReDAC)

In this chapter section the Single-Ended 10 bit, 880 kS/s ReDAC design in 180 nm (SE-ReDAC), first published in [115] is presented.

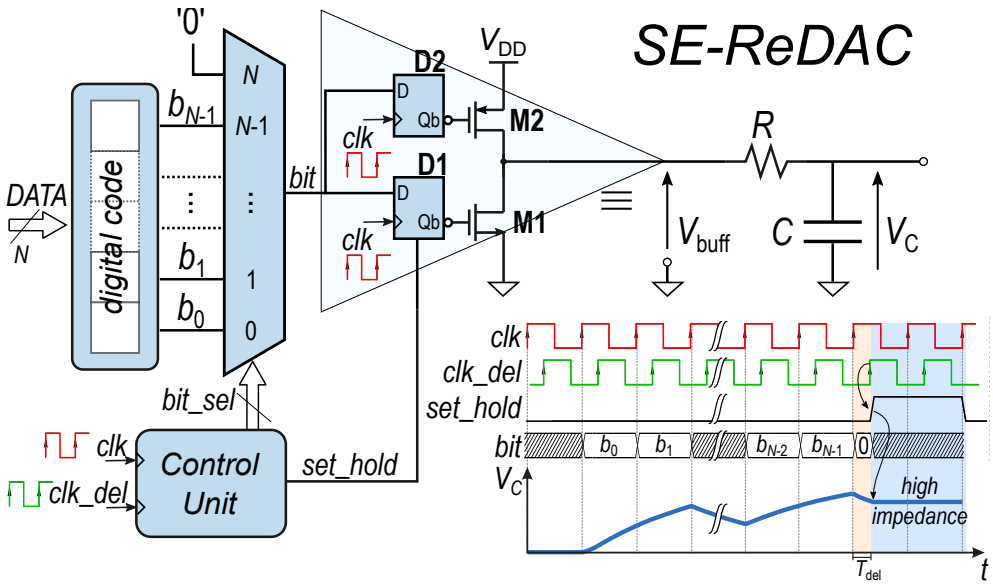


Figure 6.9: SE-ReDAC core architecture.

6.3.1 SE-ReDAC design

The SE-Relaxation Digital-to-Analog Converter (ReDAC) core block architecture shown in Fig. 6.9 is designed starting from the RC network according to the general design guidelines presented in Chapter 2.

The MiM capacitor $C = 900$ fF is designed close to the limit imposed by the $\kappa T/C$ noise 2.18 at 10 bit resolution. The high-res polysilicon resistor is sized based on the relation $T^* = \tau \log 2$ (2.4) between the conversion time, clock period, and the RC time constant, i.e.

$$T_{\text{conv}} = (N+3)T^* = (N+3)RC\log 2, \tag{6.2}$$

where $N = 10$ bit periods are required for the conversion and 3 more allocated to the hold phase. Considering (6.2) and the sample rate of $880\,\text{kS/s} = T_{\text{conv}}^{-1}$, the time constant $\tau = 126$ ns and therefore the resistance $R = 140\,\text{k}\Omega$ are derived.

The three-state buffer transistors M1 and M2 are designed based on simulations to achieve a nonlinear-loading related DNL below half LSB on 10 bit, resulting in aspect ratios of 3.3 μm/0.18 μm (6.6 μm/0.18 μm).

M2 and M1 are directly diven by the flip-flops D2 and D1, operated at the ReDAC DCO1 clock frequency $f_{\text{clk}} = 1/T$. The flip-flops, in particular, implement the parasitic suppression strategy (see Chapter 2) by being synchronously set at the end of conversion (M2 off, M1 on) and D1 asynchronously preset after a period T_{del} (M2 off, M1 off) by the delayed clock *clk_del* generated by the DCO1 of Section 6.2.2 and represented in the timing diagram of Fig. 6.2.

Contrary to the ReDAC digital cores presented in previous chapters, the SE-ReDAC architecture is implemented by sampling from the bus *DATA* the digital code on a static register, which bits are selected starting from the LSB by a multiplexer (MUX), instead of a shift register connected to the output buffer, with the aim of reducing the switching activity.

For the sake or reducing power, the finite-state machine (FSM) Control Unit is implemented as Gray-encoded counter.

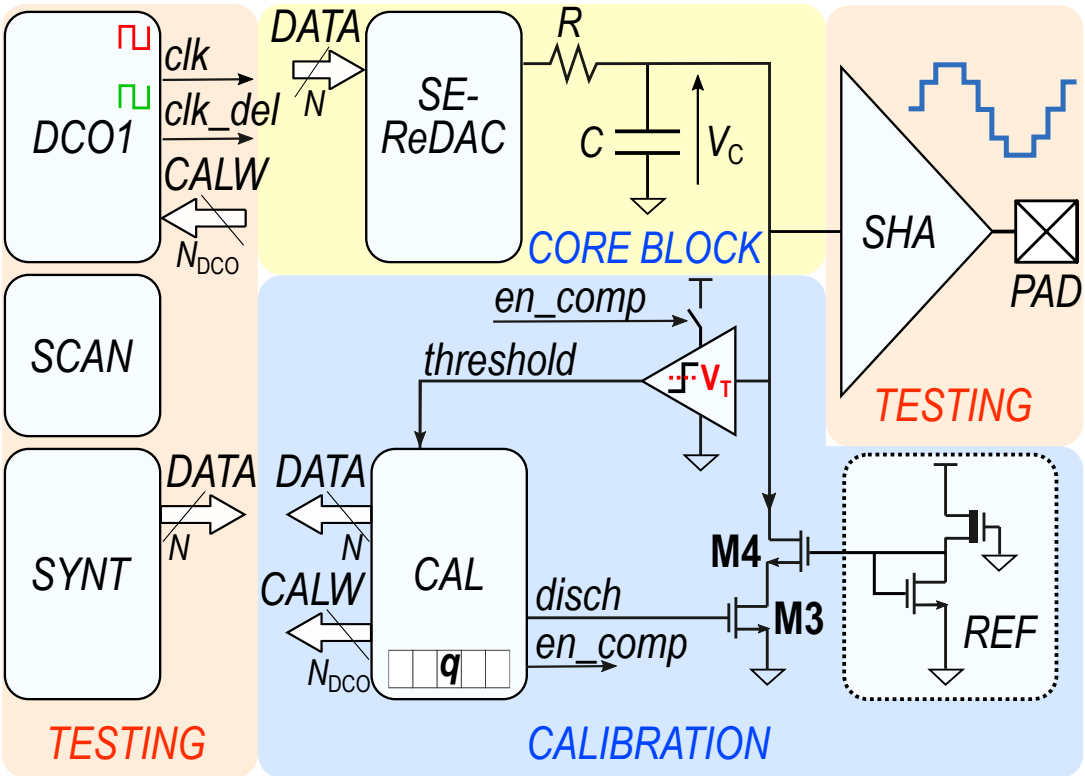


Figure 6.10: SE-ReDAC on-chip Validation Architecture

6.3.2 On-Chip Validation Architecture

The on-chip architecture for the SE-ReDAC validation, shown in Fig. 6.10, includes the SE-ReDAC core, the Sample-and-Hold Amplifier (SHA), the digital Calibration (CAL), the Digitally Controlled Oscillator (DCO1), the Direct Digital Synthesizer (SYNT). Configuration signals are provided to all the digital blocks trough a Scanchain (SCAN). It is noted that all the blocks are integrated for testing purpose and are not part of the SE-ReDAC, except for the digital CAL block, required to enforce linear operation.

6.3.3 Calibration

As in [81], [87], [105] the CAL module is designed to guarantee the SE-ReDAC linearity enforcing (2.4), i.e. $T = RC\log 2$ by detecting the sign of $\Delta V_{\mathrm{DAC}} = V_{\mathrm{DAC}}(2^{N-1}) - V_{\mathrm{DAC}}(2^{N-1} - 1)$, which is estimated and stored in its internal register q.

Similarly to the prototype presented in Chapter 4 [105], the sign of the difference ΔV_{DAC} is detected by converting alternatively $V_{\mathrm{DAC}}(2^{N-1})$ and $V_{\mathrm{DAC}}(2^{N-1} - 1)$, then measuring the time it takes for each voltage to reach a fixed threshold V_{T} when discharged trough a constant current sink. The discharge time is quantised by the UP/DOWN counter q, while the current sink is implemented by transistor M4 (W/L=0.22 µm/8 µm) enabled by the switch M3 (W/L=0.22 µm/0.18 µm) and the comparator is a single CMOS inverter enabled by power gating.

The current sink M4 is biased at constant gate voltage of 200 mV by an ultra-low power two-transistor [122] reference (REF in Fig. 6.10), exploiting the difference in threshold voltages between a depletion-mode transistor (W/L=30 µm/1 µm) and a standard nMOS (W/L=0.3 µm/20 µm), and dissipates $2, nW$ at 0.65 V supply.

The Calibration algorithm operates according to the flowgraph of Fig. 6.11. At startup the calibration word $CALW$ of DCO1 is set to $2^{N_{\mathrm{DCO}}-1}$ to make it oscillate at the the center of its tuning-range, being $N_{\mathrm{DCO}} = 9\,bit$.

At the calibration step #1, the voltage $V_{\mathrm{DAC}}(2^{N-1} - 1)$ is converted, the three-state buffer put in high impedance after T_{del} and the capacitor discharged trough M4 while incrementing the counter q. When the capacitor voltage V_{C} crosses the comparator threshold V_{T}, the count-up is stopped.

Analogously, in the calibration step #2, $V_{\mathrm{DAC}}(2^{N-1})$ is converted and the discharge network activated while decrementing q, until V_{T} is crossed and the count-down stopped.

At the end of each sequence of step #1, stap #2, the sign of the counter q is equal, neglecting comparator noise and counter quantization, to the sign

of $-\Delta V_{\mathrm{DAC}}$ and therefore $-\Delta T$, according to what discussed in Chapter 2. The timing diagram of the generic calibration loop is shown in Fig. 6.12.

If $q \neq 0$, the DCO1 tuning word $CALW \propto T$ is increased (or decreased) dichotomously depending on if $q > 0$ ($q < 0$), in a SAR-like fashion. If conversely $q = 0$, the SE-ReDAC linearity condition $T = RC \log 2$ is met with a less-than 1 LSB error, and the calibration procedure ends.

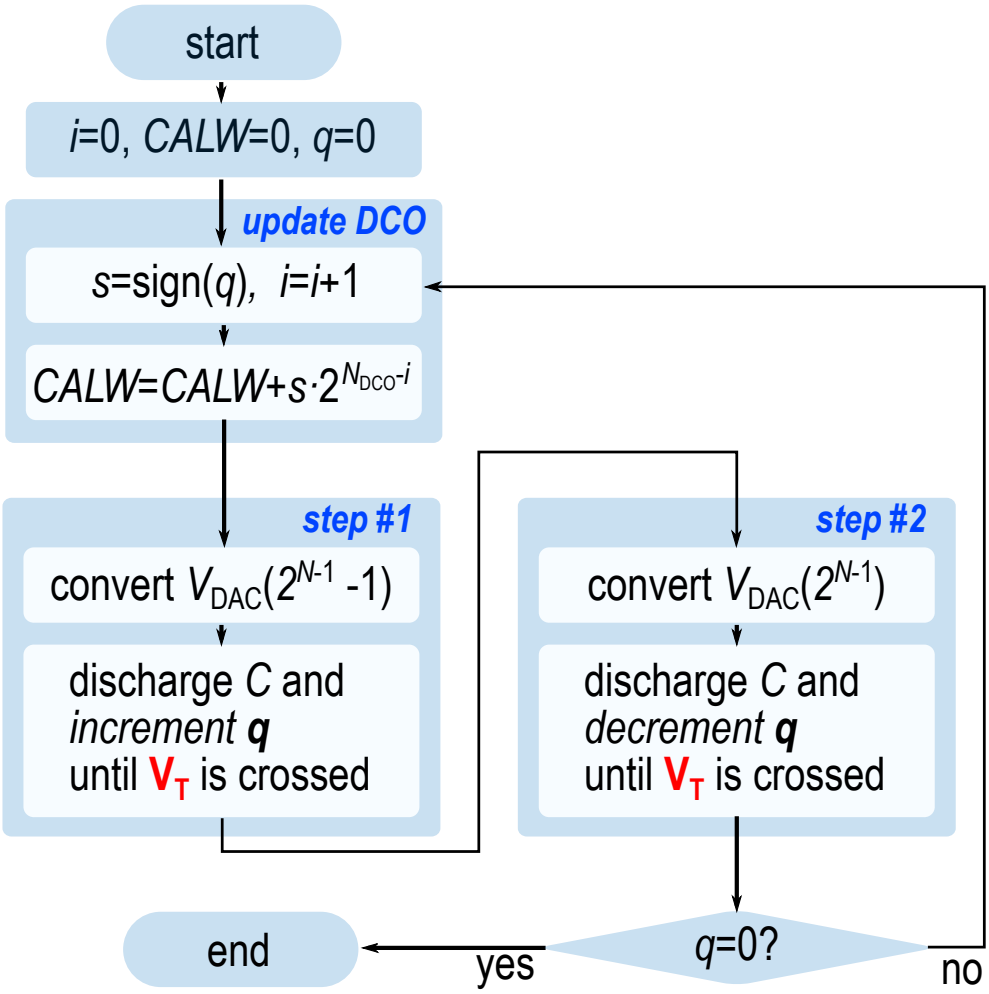


Figure 6.11: SE-ReDAC Calibration flowchart

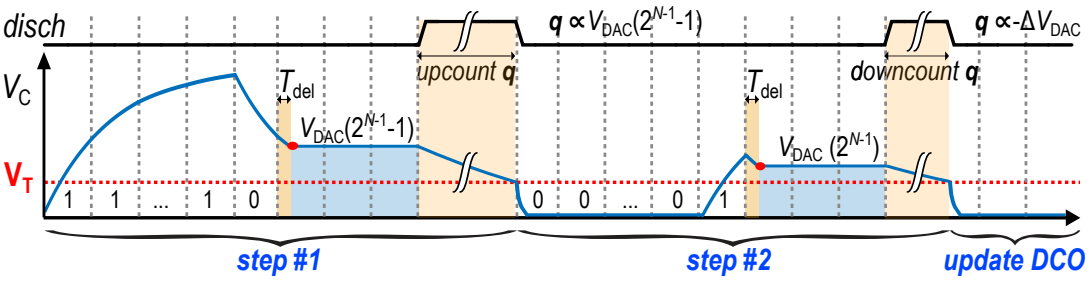
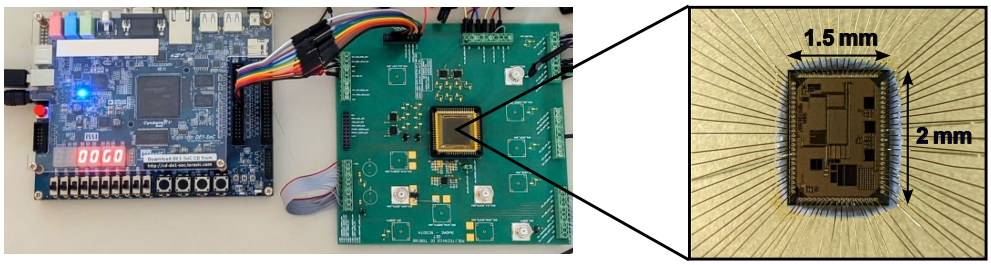
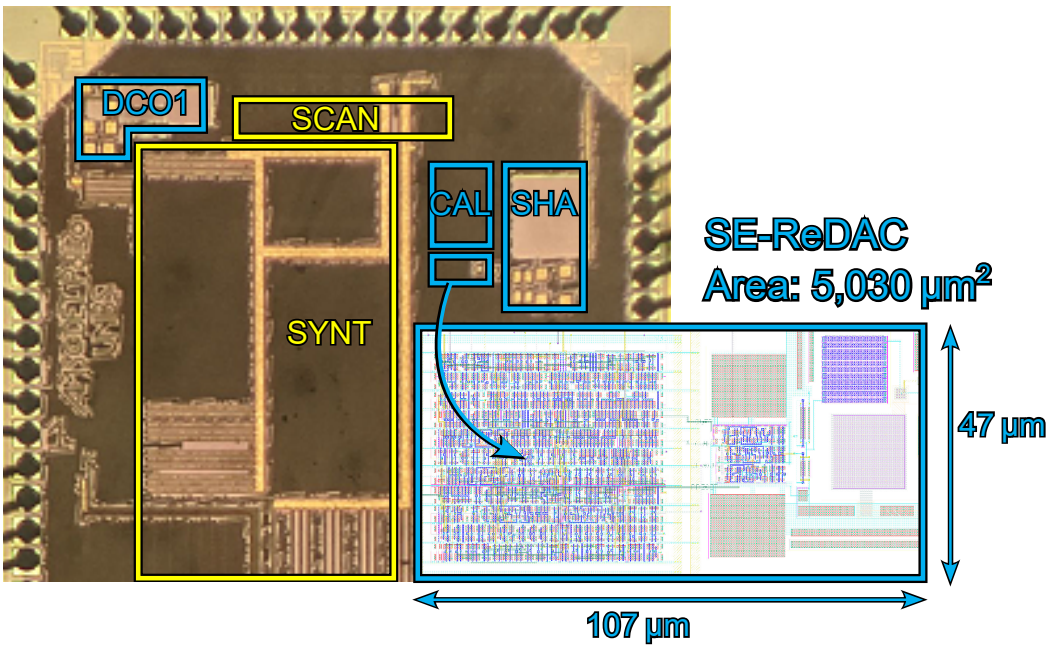


Figure 6.12: SE-ReDAC calibration cycle timing diagram.



(a)



(b)

Figure 6.13: Photo of the test setup (a) and IC micrograph highlighting the SE-ReDAC related blocks.

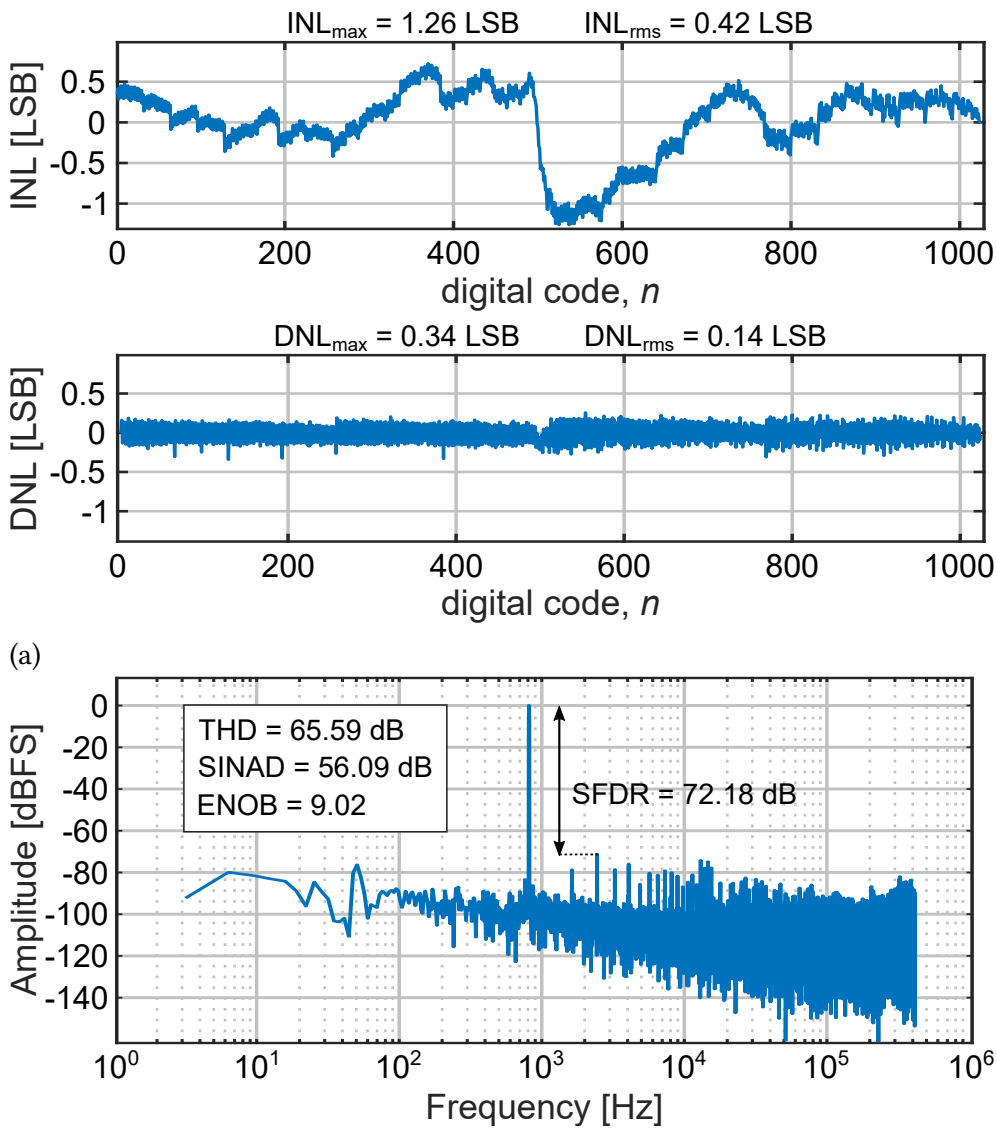


Figure 6.14: SE-ReDAC static nonlinearity (a) and single-frequency dynamic characterization (b) at 0.8 kHz, 90% swing.

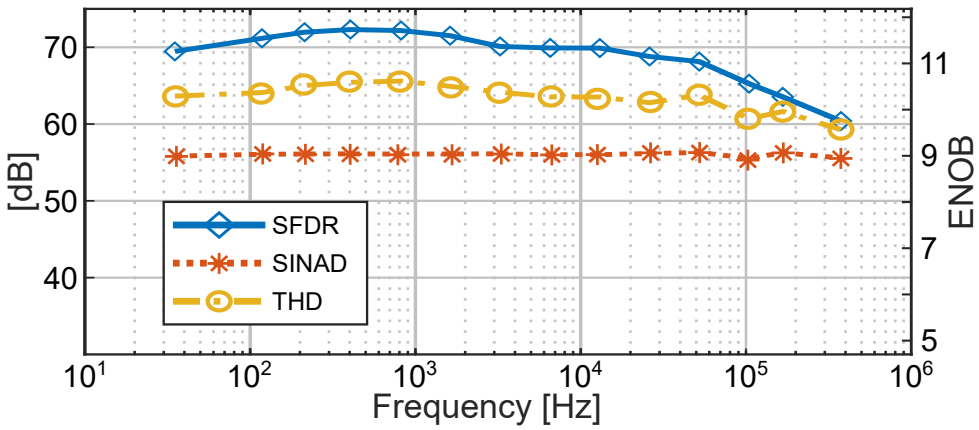
6.3.4 Single-Dice Validation

The 180 nm ReDAC IC test setup is reported in Fig. 6.13(a) along with the micrograph of the IC highlighting the SE-ReDAC related blocks in Fig. 6.13(b). The SE-Relaxation Digital-to-Analog Converter (ReDAC) area is just 5,030 μm^2.

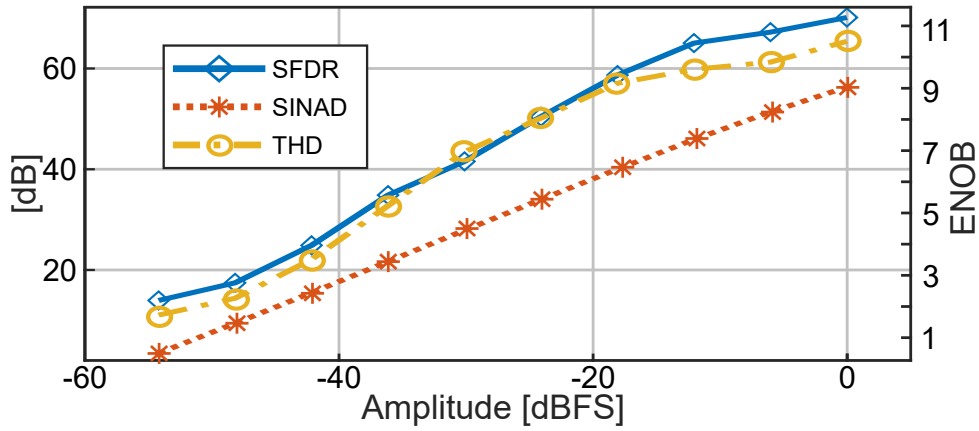
The IC is powered using bench-top voltage sources trough a custom PCB board. The on-chip blocks are driven by the Scanchain (SCAN) serial

communication signals operated from a PC trough an external FPGA board. The analog SE-Relaxation Digital-to-Analog Converter (ReDAC) output is probed via a BNC connector mounted on the custom PCB and acquired by a Picoscope® 4262 oscilloscope.

The single SE-ReDAC IC is tested under the nominal supply of 0.65 V at ambient temperature. After running the self calibration procedure, static SE-ReDAC characterization is performed, revealing a maximum INL (DNL) of 1.26 LSB (0.34 LSB) and a rms INL (DNL) of 0.42 LSB (0.14 LSB), as per Fig. 6.14(a).



(a)

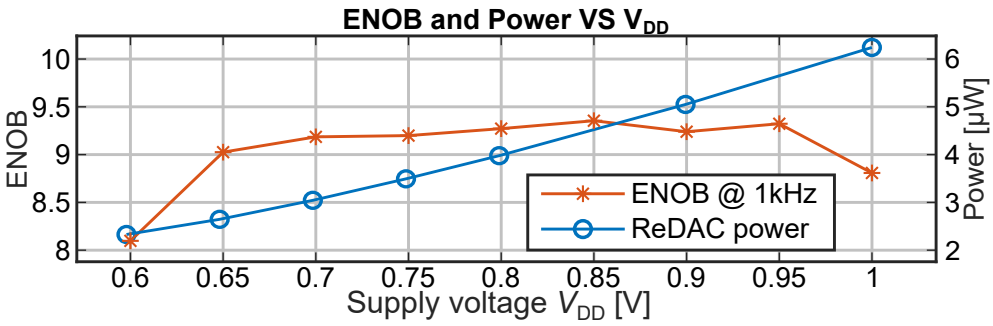


(b)

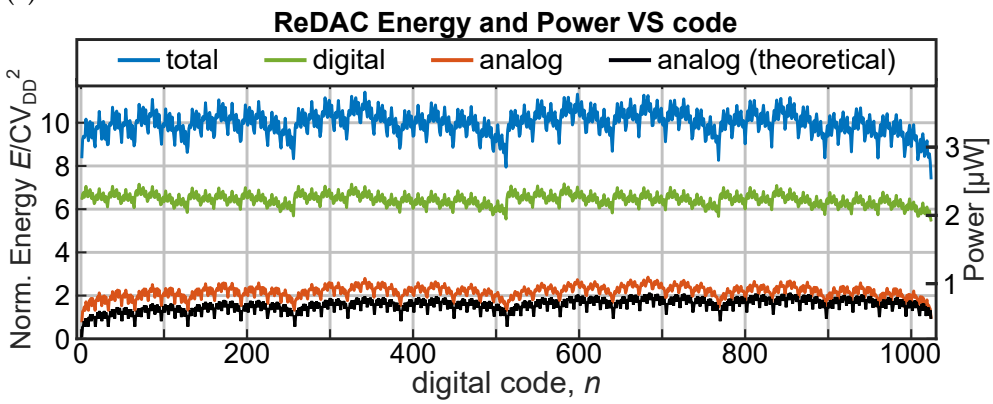
Figure 6.15: SE-ReDAC dynamic characterization in frequency, 90% swing amplitude (a) and in amplitude, 0.8 kHz frequency (b).

Dynamic characterization in Fig. 6.14(b) at single sine wave input of 90% swing amplitude and 0.8 kHz frequency results in measured 72.18 dB of SFDR, 65.59 dB THD and 56.09 dB SNDR, equivalent to 9.02 effective bits (ENOB).

Dynamic characterizations at constant amplitude (90% swing) spanning the frequency band up to the Nyquist rate and at constant frequency (0.8 kHz) spanning the whole input swing are shown in Fig. 6.15(a) and Fig. 6.15(b) respectively, revealing proper DAC operation in amplitude and consistent linearity at full bandwidth.



(a)



(b)

Figure 6.16: SE-ReDAC ENOB and average power against supply voltage (a) and energy per conversion/average power versus digital code.

Performance characterization under supply voltages ranging from 0.6 V up to 1 V, 1 kHz 90% swing input sine, reveal an ENOB higher than 9 bit on most of the supply voltage range, as reported in Fig. 6.16(a).

Considering the same supply sweep, the average SE-ReDAC power in continuous conversion shown in Fig. 6.16(a), results in power consumption that ranges from 2.3 μW to 6.2 μW and an optimum power-performance operation between 0.65 V and 0.7 V.

The analog energy per conversion versus code, initially analytically evaluated in (2.41) of Chapter 2 as

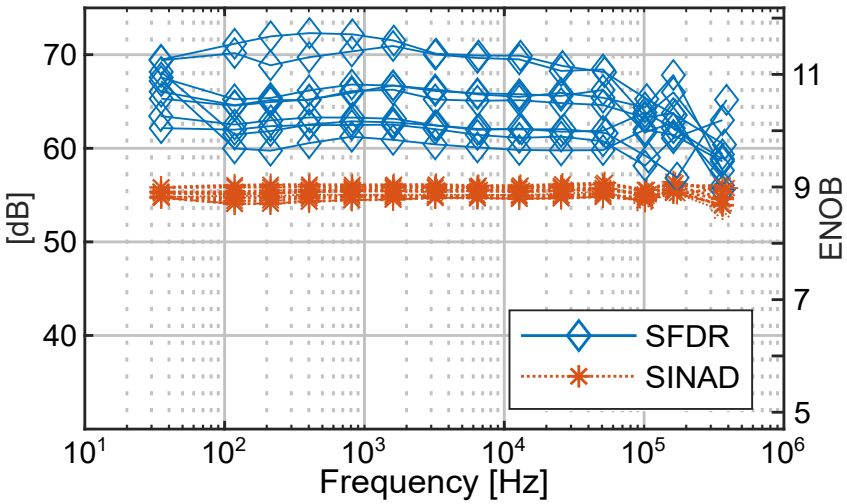
$$E(n) = CV_{\mathrm{DD}}^2 \sum_{i=0}^{N-1} b_i \sum_{j=0}^{i} 2^{j-i}(b_j - b_{j-1}), \qquad b_{-1} \triangleq 0$$

is experimentally verified [115] for the first time and compared to the measured analog energy per conversion in Fig. 6.16(b) (red and black curves). The digital core and the total power versus code (green and blue curves) are also measured and reported so that the SE-Relaxation Digital-to-Analog Converter (ReDAC) analog (digital, total) power is 0.8 μW (2.5 W, 3.3 W).

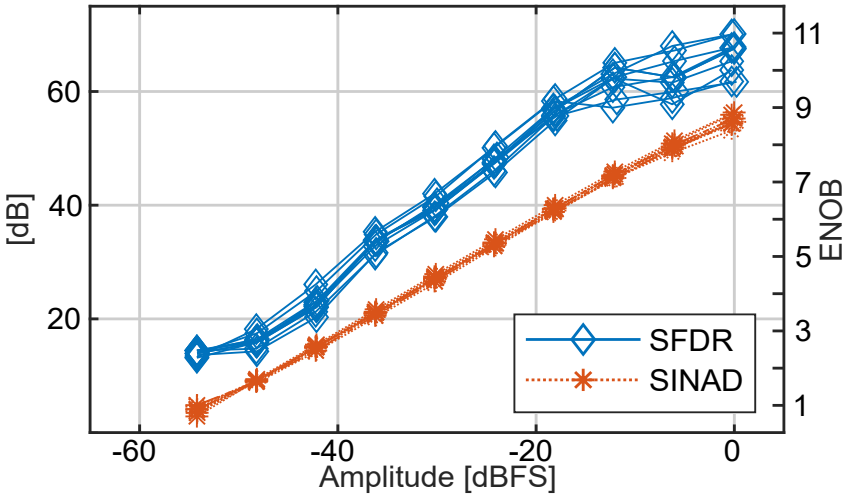
6.3.5 Multi-Dice Validation

Multi-dice validation of the SE-ReDAC has been performed by a 90% swing input sine wave under frequencies sweeping up to the Nyquist rate and at constant 0.8 kHz frequency up to the full input range, as reported in Fig. 6.17(a) and Fig. 6.17(b) respectively.

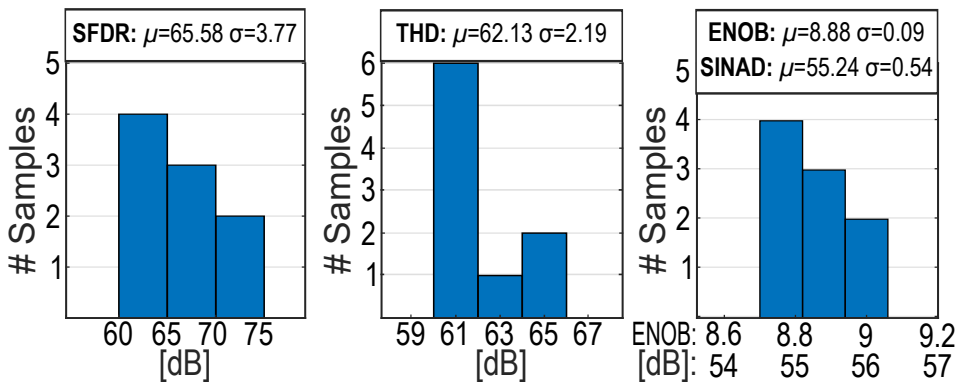
The performance distribution related to the single-frequency (90% swing, 0.8 kHz) characterization reported in Fig. 6.17(c) shows a mean (standard deviation) value for SFDR of 65.58 dB (3.77 dB), THD of 82.13 dB (2.19 dB) and SNDR of 55.24 dB (0.54 dB). These results prove a consistent SE-ReDAC linearity of average 8.88 bit ENOB among all the samples with a tiny standard deviation of 0.09 bit.



(a)



(b)



(c)

Figure 6.17: SE-ReDAC multi-dice dynamic characterization in frequency, 90% swing (a) and in amplitude, 0.8 kHz (b). Distribution of the multi-dice dynamic performance at 0.8 kHz, 90% swing (c).

6.3.6 Comparison

The SE-ReDAC is compared in Table 6.1 with integrated ReDAC designs presented in previous chapters as well as state-of-the-art DACs.

The SE-ReDAC achieves the second smallest normalised total area among the reported works (1.3× the minimum one in [123], which has tough lower performance in terms of both accuracy and sample rate). The proposed work also reports the lowest normalised digital area, quantified as 2.3× less than [86], 13× less than [124] and from 4× to 4.7× less than previously presented ReDACs ([87] and [81] respectively).

The SE-ReDAC requires a clock frequency which is much lower than DDPM converters given the same sample rate, with the further advantage that ReDAC dynamic performance are kept consistent in the whole bandwidth, translating into an ENOB degradation of solely 0.08 bit at the Nyquist-rate, as opposed to 6.1 bit degradation of the DDPM in [86].

All these features result in highly competitive SE-ReDAC Figure of Merit in terms of energy (FOM) and normalised area (FOM_A) equal to 166 dB and 175 dB respectively.

The SE-ReDAC FOMs, compared in the graphs of Fig. 6.18 with other non-ReDAC architectures, are comparable only to the ΣΔ audio DAC in [125], which achieves 7.8 bit more ENOB (which is tough A-weighted) at the cost of 212× higher power, 20× lower bandwidth and 19× larger area footprint. The SE-ReDAC also operates at the smallest reported supply voltage, equal to [81] and [126]).

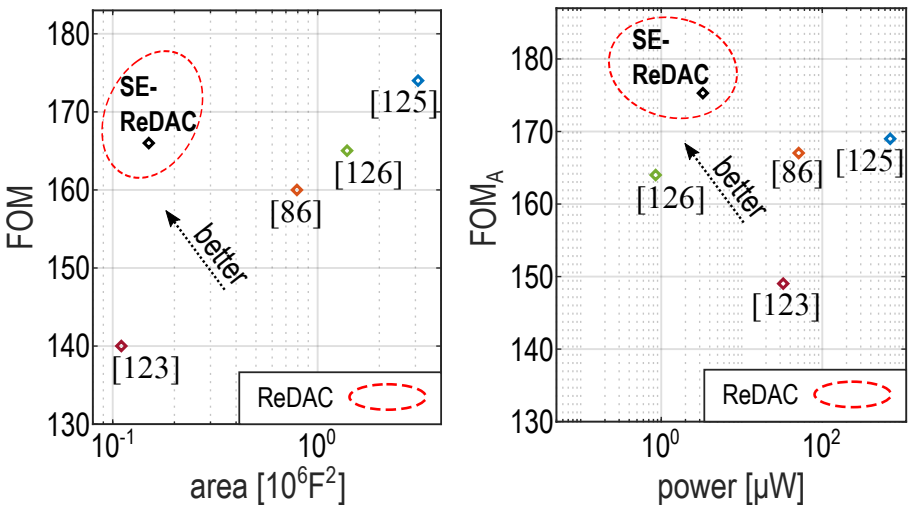


Figure 6.18: Comparison with state of the art based on FOM versus area and FOM_A versus power.

Table 6.1: DAC Performance Comparison
[86] [81]

		SE-ReDAC	[86]	[81]	[106]	[126]	[124]	[123]	[125]
Technology F (nm)		180	40	40	180	180	180	350	180
Synthesizable		yes	yes	yes	yes	no	no	no	partially
Type		ReDAC	DDPM	ReDAC	ReDAC	cap+mos-string	R-string	curr. steer.	$\Sigma\Delta$
Validation		meas.	meas.	sim.	sim.	meas.	meas.	meas.	meas.
Digital area ($10^6 F^2$)		0.075	0.17	0.30	0.39[a]	N/A	1	N/A	0.62
Area ($10^6 \mu m^2$) / ($10^6 F^2$)		0.00503 / 0.15	0.00127 / 0.79	0.00091 / 0.57	0.01359[a] / 0.42	0.045[b] / 1.39	0.15 / 4.6	0.014 / 0.11	0.10[c] / 3.08
Resolution (bit)		10	12	10	10	10	12	9	N/A
Sample rate (kS/s)		880	110	400	1,450	200	72[d]	111	40[e]
Supply / min.supply (V)		0.65 / 0.6	1 / 0.7	0.6 / N/A	0.7 / N/A	0.6 / N/A	18 / 1.8	3.3 / N/A	1.8 / N/A
INL / DNL (LSB)		1.26 / 0.34	3 / 1	0.33 / 0.2	1.01 / 0.45	0.56 / 0.32	0.54 / 0.26	1.6 / 0.8	N/A
SFDR / THD (dB)		72.18 / 65.59	85 / 85	76.8 / 66.7	59.3 / 59.2	71 / N/A	N/A	N/A	N/A
SINAD (dB)	peak	56.09	72	61.0	58.5	56.43	N/A	48[b]	103[f]
	@$f_s/2$	55.59	35	N/A	N/A	N/A	N/A	N/A	N/A
ENOB	peak	9.02	11.6	9.9	9.4	9.08	N/A	8[b]	16.8
	@$f_s/2$	8.94	5.5	N/A	N/A	N/A	N/A	N/A	N/A
Power (μW)		3.3	50.8	0.44	9.15	0.85[b]	875[b]	33	700[g]
†FOM / ‡FOM_A (dB)		166 / 175	160 / 161	176 / 178	166 / 170	165 / 164	N/A	140 / 149	174[f] / 169

†$\mathrm{FOM} = 10\log_{10}\left(\frac{2^{2\cdot\mathrm{ENOB}}BW}{P}\right)$ ‡$\mathrm{FOM_A} = \mathrm{FOM} + 10\log_{10}(1/A_\mathrm{F})$ being A_F the F-normalised area
[a]includes part of the calibration [b]based on text and figures [c] not including reconstruction filter [d]from row-line time [e]twice the signal bandwidth [f]A-weighted
[g]analog power only.

6.4 Differential ReDAC (Diff-ReDAC)

The present section describes the implementation of the 13 bit 100 kS/s Differential-ReDAC (Diff-ReDAC) as first presented in [116], which core architecture is shown in Fig. 6.19.

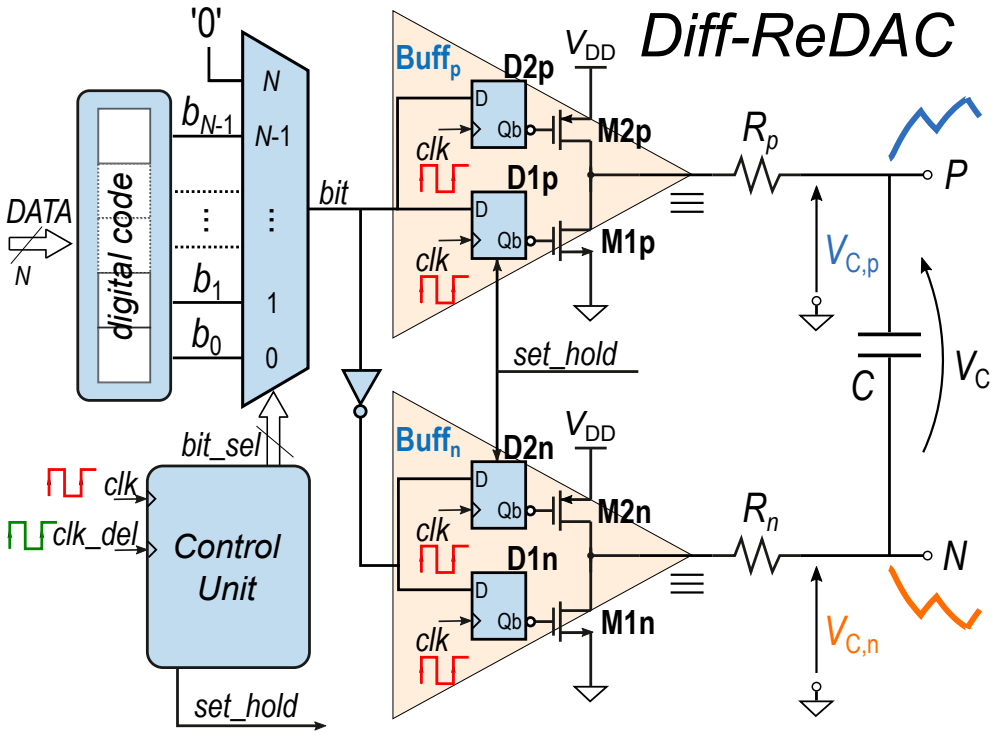


Figure 6.19: Diff-ReDAC core architecture.

6.4.1 Diff-ReDAC Design

The Diff-ReDAC of Fig. 6.19 is the first presented differential-output implementation of the ReDAC [116]. The differential output includes two three-state buffers, Buff_p, Buff_n, driving a floating RC network made of $R_\text{p} = R_\text{n} = R/2$ and C.

The two buffers Buff_p and Buff_n are driven by the digital input bitstream $(b_0 ... b_{N-1})$ and its complemented version $(\bar{b}_0 ... \bar{b}_{N-1})$, respectively, trough the four flip-flops D1_p, D2_p, D1_n, D2_n.

As in the SE-ReDAC implementation, the Diff-ReDAC employs a multiplexer (MUX) to feed serially the bits of the digital-code to the three-state buffer, LSB-first, at the constant rate provided by the *clk* signal of the DCO2 oscillator, presented in Section 6.2.2.

The Diff-ReDAC output voltage after the MSB has been converted, i.e. $V_{\mathrm{DAC}}(n) = v_C(NT^*) = v_{C,\mathrm{p}}(NT^*) - v_{C,\mathrm{n}}(NT^*)$ is expressed as

$$V_{\mathrm{DAC}}(n) = 2\frac{n}{2^N}V_{\mathrm{DD}} - V_{\mathrm{DD}} \tag{6.3}$$

and it is held constant by putting $\mathrm{Buff_p}$ and $\mathrm{Buff_n}$ in high impedance at the end of conversion.

The parasitics error suppression presented for the single-ended DACs (see Chapters 2-5) is here extended to the differential architecture by driving $\mathrm{Buff_p}$ and $\mathrm{Buff_n}$ to logic 0 (logic 1) at the end of conversion, and asynchronously setting them in high impedance at the same time $t = NT^* + T_{\mathrm{del}}$ trough the *set_hold* signal, exploiting the flip-flops $\mathrm{D1_p}$ ($\mathrm{D2_n}$) asynchronous set (clear), triggered by the delayed clock *clk_del*, generated by the DCO2.

The Diff-ReDAC is designed according to the flow presented in Chapter 2, to achieve a conversion time $T_{\mathrm{conv}} = (100\,\mathrm{kS/s})^{-1}$ of

$$T_{\mathrm{conv}} = (N+2)T^* = (N+2)RC\log 2, \tag{6.4}$$

where the resolution is $N = 13$ bit and 2 period are reserved for T_{del} and the hold phase. Based on that, the Metal-insulator-Metal (MiM) capacitor is designed close to the $\kappa T/C$ thermal noise limit, resulting in $C = 2.6\,\mathrm{pF}$ and poly-resistors to meet the time constant in (6.4) equal to $R_{\mathrm{p}} = R_{\mathrm{n}} = R/2 = 180\,\mathrm{k\Omega}$.

The final stage transistors $\mathrm{M1_p}$, $\mathrm{M2_p}$, $\mathrm{M1_n}$, $\mathrm{M2_n}$ have the same aspect ratio of $5\,\mu\mathrm{m}/0.18\,\mu\mathrm{m}$, designed to keep the nonlinear loading effect on DNL below half LSB.

6.4.2 On-Chip Validation Architecture

The on-chip architecture to test the Diff-ReDAC is shown in Fig. 6.20. It entails the Diff-ReDAC core block, a Sample-and-Hold Amplifier (SHA) to probe the differential Digital-to-Analog Converter (DAC) output, a digital foreground calibration (CAL), a digitally controlled oscillator (DCO2), a Direct Digital Synthesizer (SYNT) and a serial interface (SCAN) to configure the on-chip digital blocks.

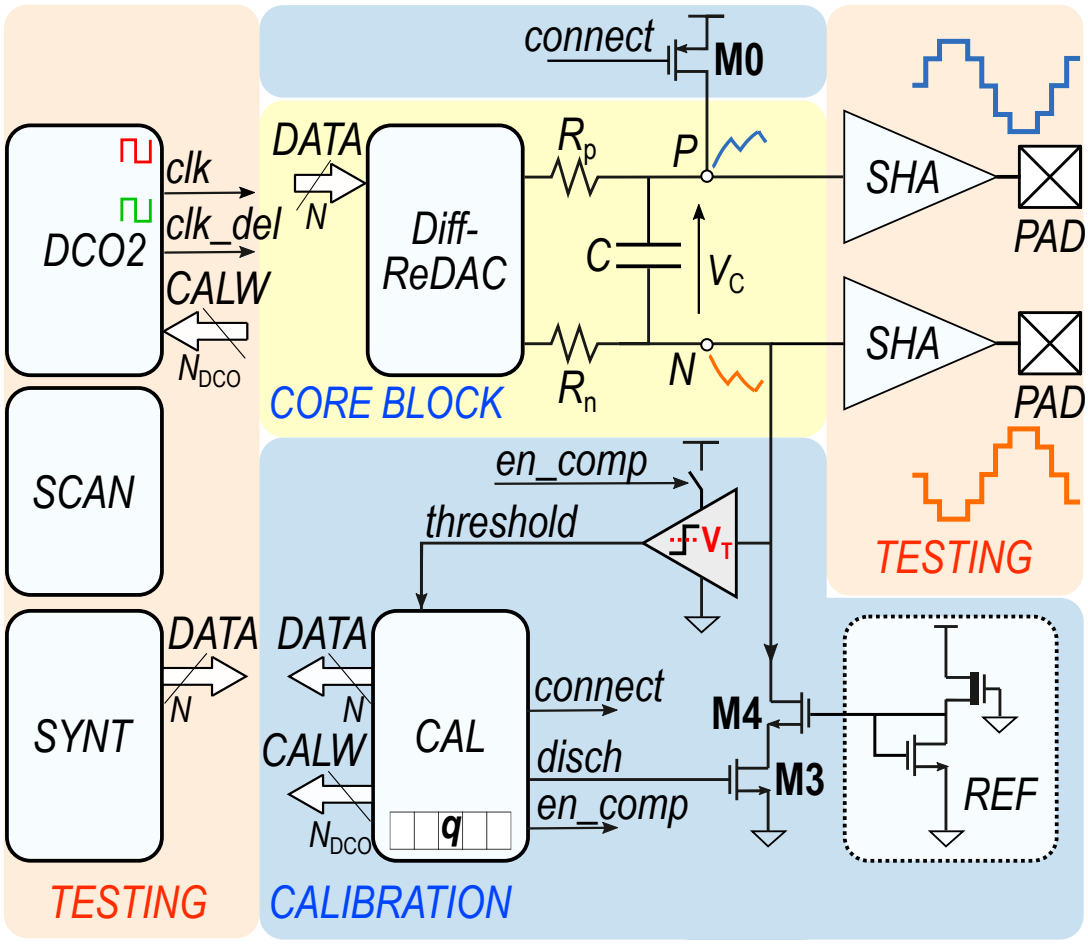


Figure 6.20: Diff-ReDAC Validation Architecture

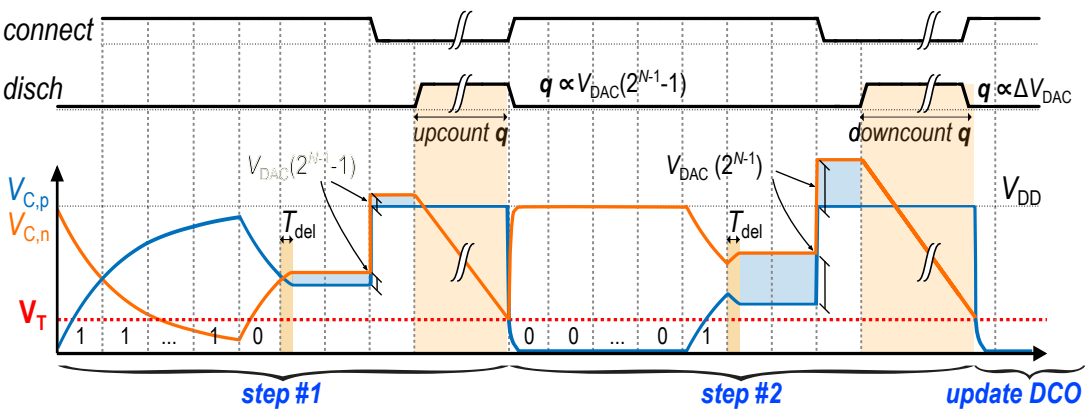


Figure 6.21: Diff-ReDAC timing diagram of a calibration cycle.

6.4.3 Calibration

The digital CAL module is implemented to enforce $T = \tau \log 2$ (2.4 in Chapter 2) as required to get linear Diff-ReDAC operation, by tuning the DCO2 tuning $N_{\mathrm{DCO}} = 12$ bit word $CALW$ depending on the mid-range voltage step $\Delta V_{\mathrm{DAC}} = V_{\mathrm{DAC}}(2^{N-1}) - V_{\mathrm{DAC}}(2^{N-1} - 1)$ digitised and stored in the q register (see Fig. 6.20).

The sign of ΔV_{DAC} by a single-lope A/D conversion performed by discharging at constant current the Diff-ReDAC capacitor after the conversion of $V_{\mathrm{DAC}}(2^{N-1} - 1)$ and $V_{\mathrm{DAC}}(2^{N-1})$. To acquire the discharge time at the end of each CAL conversion, node P is connected to V_{DD}, while the output three-state buffers are kept in high impedance. Then the current sink M4 (biased at constant 200 mV gate voltage by the 2 nW power two-transistor reference REF [122]) is enabled by the switch M3 to discharge node N. The time it takes fro the two voltages $V_{\mathrm{DD}} - V_{\mathrm{DAC}}(2^{N-1} - 1)$ and $V_{\mathrm{DD}} - V_{\mathrm{DAC}}(2^{N-1})$ to reach the comparator threshold $\mathrm{V_T}$ is quantised and acquired by the UP/DOWN counter q, operated respectively in UP and DOWN counting mode for the two voltages, as shown in the time diagram of Fig. 6.21.

The CAL algorithm operates according to the flow diagram of Fig. 6.22. At startup, the $N_{\mathrm{DCO}} = 12$ bit DCO2 tuning word $CALW$ is reset to $2^{N_{\mathrm{DCO}}-1}$, to set the oscillator *clk* period T at the center of its tuning range, while the counter q is set to zero. In calibration step #1, the voltage $V_{\mathrm{DAC}}(2^{N-1} - 1)$ is converted, the parasitic error suppression applied, the node P connected to V_{DD} by activating M0, then the capacitor is discharged trough M4 while incrementing q at the *clk* rate.

In the calibration step #2, the Diff-ReDAC converts $V_{\mathrm{DAC}}(2^{N-1})$, node P connected to V_{DD} and the capacitor discharged trough M4, decrementing the counter q until threshold V_{T} is crossed by $v_{C,\mathrm{n}}$. Neglecting the counter quantization and the comparator noise, the sign of the q counter at the end of the two calibration steps is equal to the sign of ΔV_{DAC} and ΔT. Based on that sign, (when $q \neq 0$) the DCO2 tuning word $CALW$ can be dichotomously updated by decrease (increase) its value by a SAR-like logic when $q > 0$ ($q < 0$), and a new calibration cycle starts.

When $q = 0$ is met at the end of one calibration cycle, $T = T^* = \tau \log 2$ (see (2.4) of Chapter 2) is enforced within 1 LSB, and the calibration is complete.

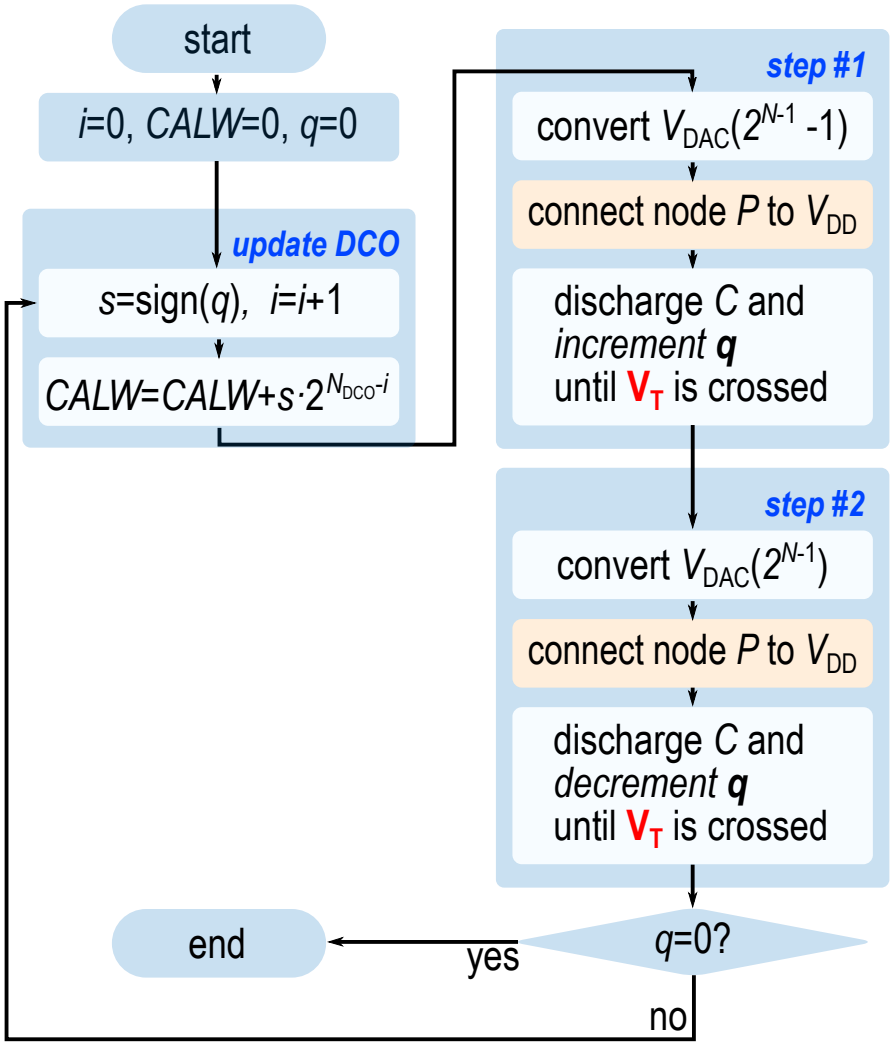
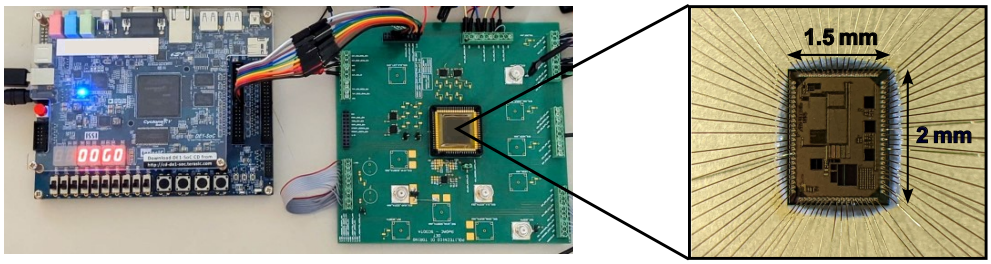
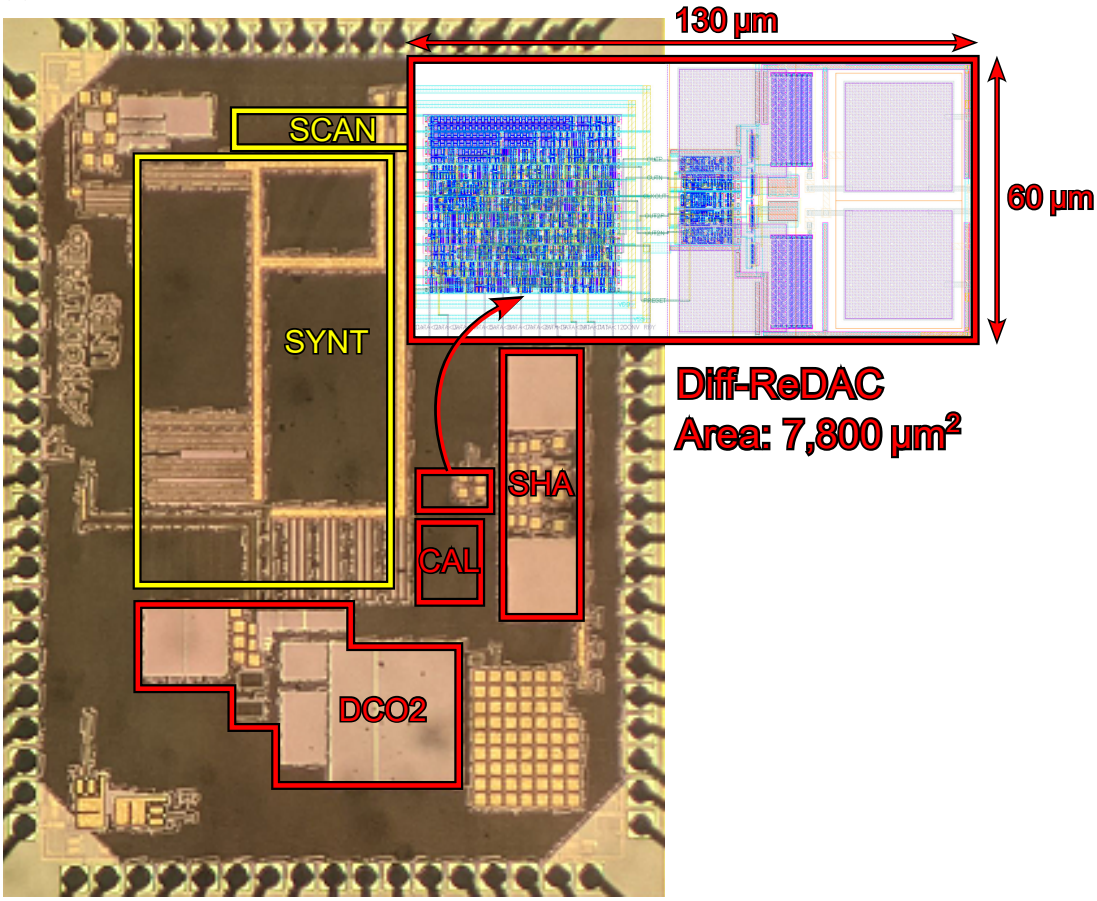


Figure 6.22: Diff-ReDAC Calibration flowchart



(a)



(b)

Figure 6.23: Photo of the test setup (a) and IC micrograph highlighting the Diff-ReDAC related blocks.

6.4.4 Single-Dice Validation

The measurement test bench and the micrograph highlighting the Diff-ReDAC related blocks in 180 nm CMOS technology are reported in Fig. 6.23(a) and Fig. 6.23(b) respectively, where the Diff-ReDAC area is highlighted as 7,800 μm^2. The on-chip modules are operated via serial communication from a PC, driving the on-chip Scanchain trough an FPGA board.

The analog output pads of the Diff-ReDAC are probed via BNC connectors on a custom PCB board, where the test dice is mounted, and the signals acquired by a Picoscope® 4262 oscilloscope.

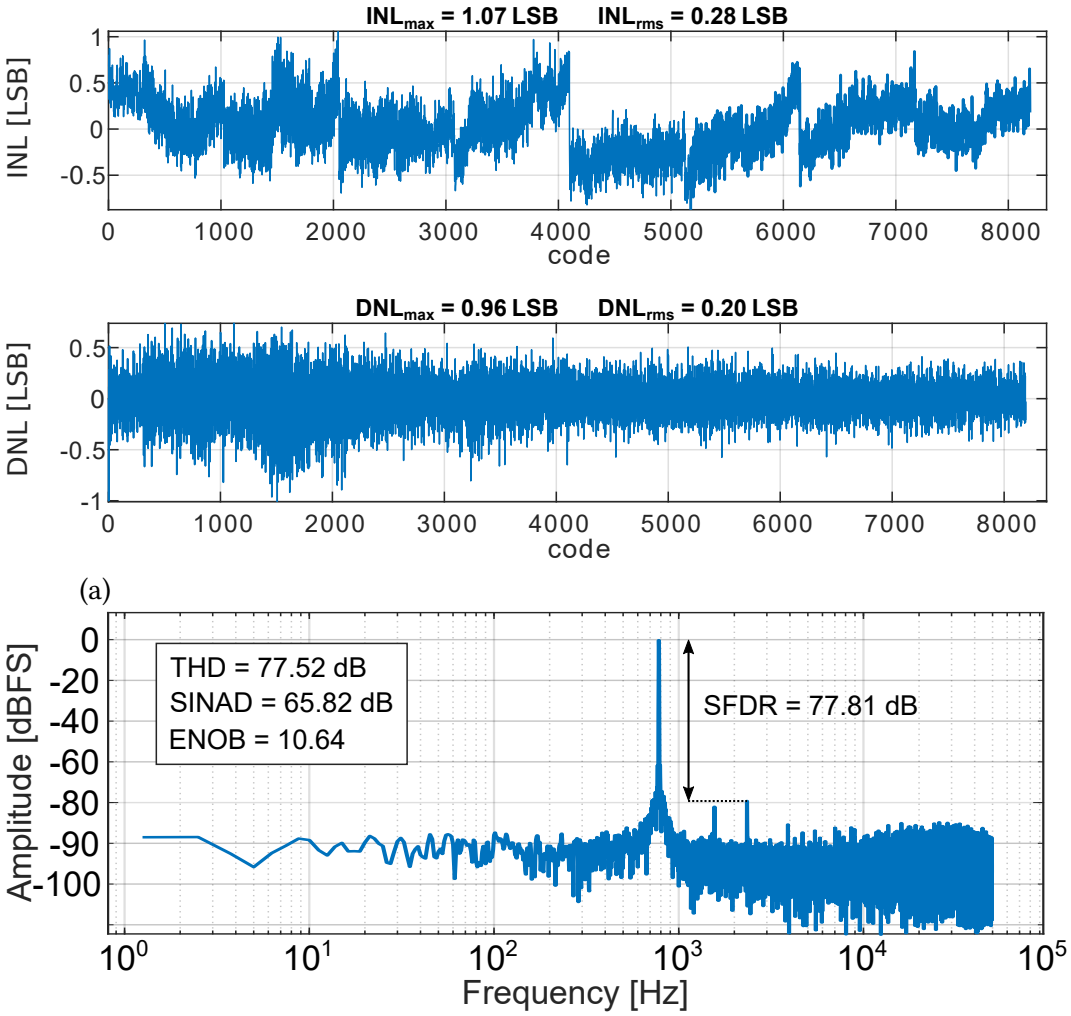
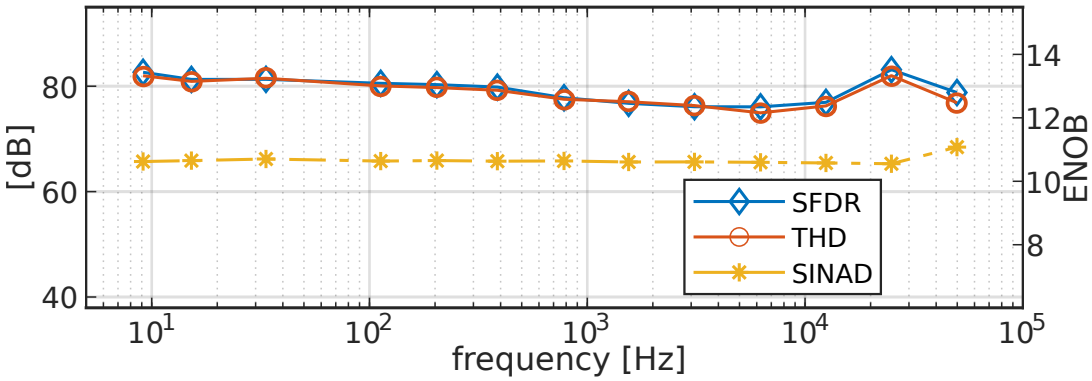
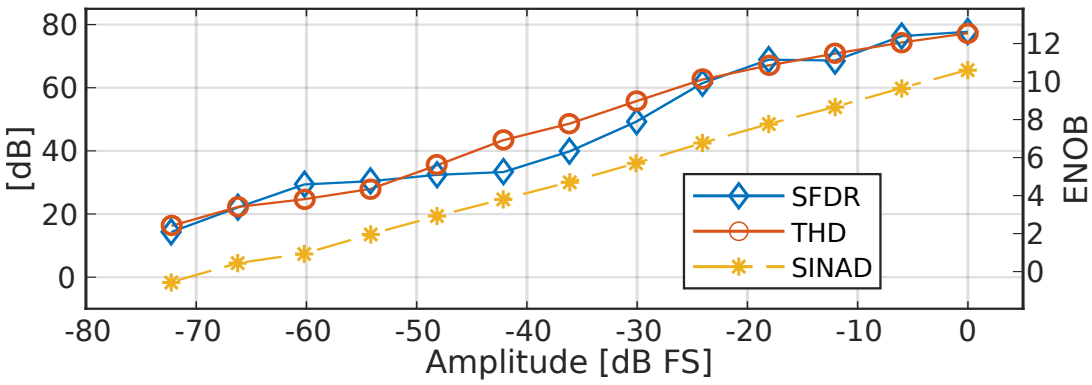


Figure 6.24: Diff-ReDAC static nonlinearity (a) and single-frequency dynamic characterization (b) at 0.8 kHz, 90% swing.

The static Diff-ReDAC characterization on 13 bits, under 0.6 V nominal supply, in Fig. 6.24(a) reveal a maximum INL (DNL) of 1.07 LSB (0.28 LSB) and a rms INL (DNL) of 0.28 LSB (0.20 LSB). Dynamic characterization under 0.8 kHz sine wave input, 90% swing, shown in Fig. 6.24(b) reveals 77.81 dB SFDR, 77.52 dB THD and 65.82 dB SINAD, corresponding to 10.64 ENOB.



(a)



(b)

Figure 6.25: Diff-ReDAC dynamic characterization in frequency, 90% swing amplitude (a) and in amplitude, 0.8 kHz frequency (b).

The dynamic characterization at constant amplitude (90% swing) and frequencies covering the whole bandwidth is reported in Fig. 6.25(a), while dynamic characterization at constant frequency (0.8 kHz) and up to full swing is reported in Fig. 6.25(b). Both figures reveal consistent Diff-ReDAC operation over the input swing and up to Nyquist.

The evaluation of dynamic performance under different supply voltages ranging from 0.45 V to 1 V and 1 kHz, 90% swing, input sine wave reveal an ENOB larger than 10 bits on a large portion of the supply range while the power consumption spans from 420 nW to 2,650 nW, and it is 880 nW

at the nominal 0.6 V supply voltage.

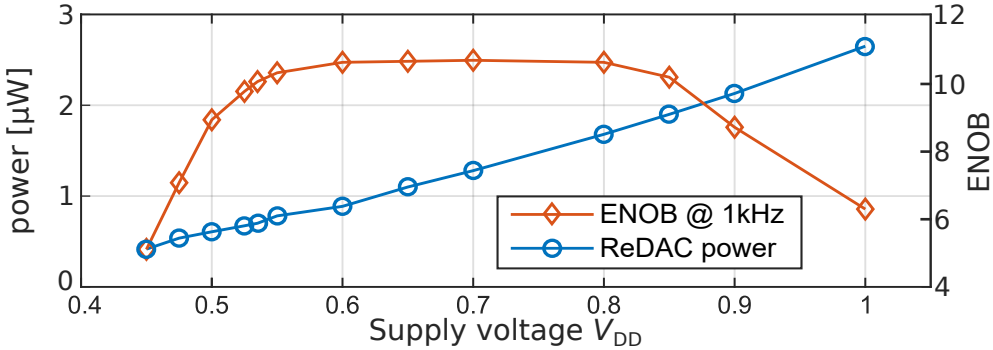
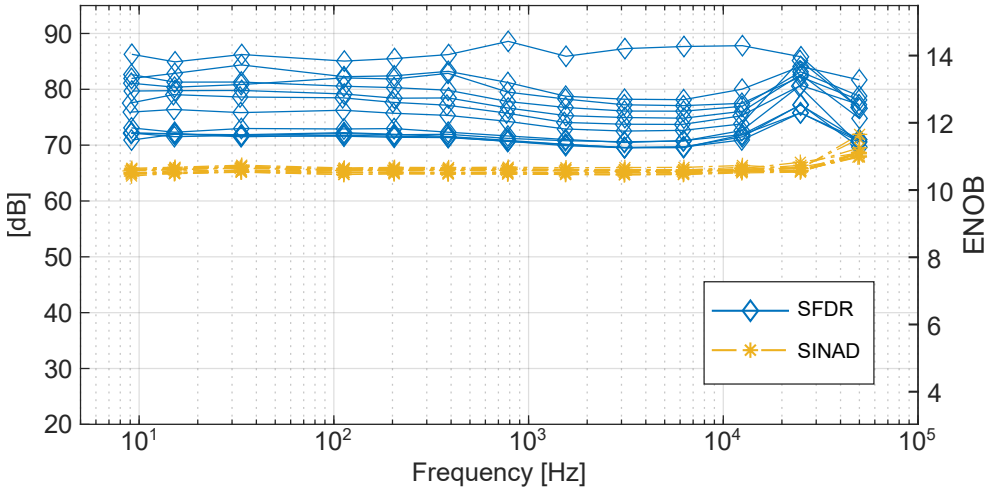


Figure 6.26: SE-ReDAC ENOB and average power under different supply voltages.

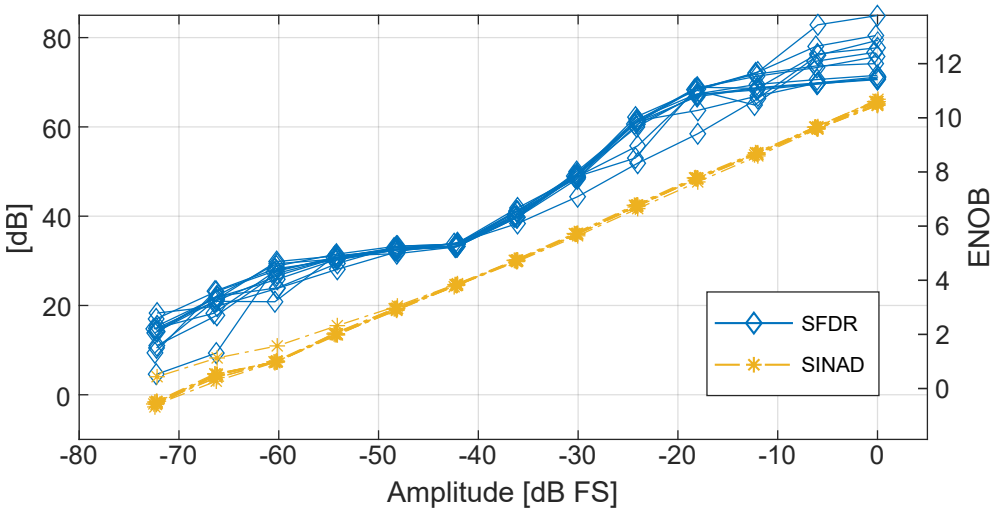
6.4.5 Multi-Dice Validation

The multi-dice validation across 12 samples is performed under 90% input sinewave and up to Nyquist (Fig. 6.27(a)) and at constant 0.8 kHz frequency spanning the whole input range (Fig. 6.27(b)).

Performance characterization at 90% swing sine, single frequency (0.8 kHz) are distributed according to the histograms in Fig. 6.28(c), revealing a mean (standard deviation) of 75.94 dB (5.31 dB) for SFDR, 74.65 dB (3.98 dB) for THD and 65.42 dB (0.40 dB) for SINAD, resulting in consistent Diff-ReDAC linearity of 10.57 bit ENOB with only 0.07 bit standard deviation.



(a)



(b)

Figure 6.27: Diff-ReDAC multi-dice dynamic characterization in frequency, 90% swing (a) and in amplitude, 0.8 kHz (b).

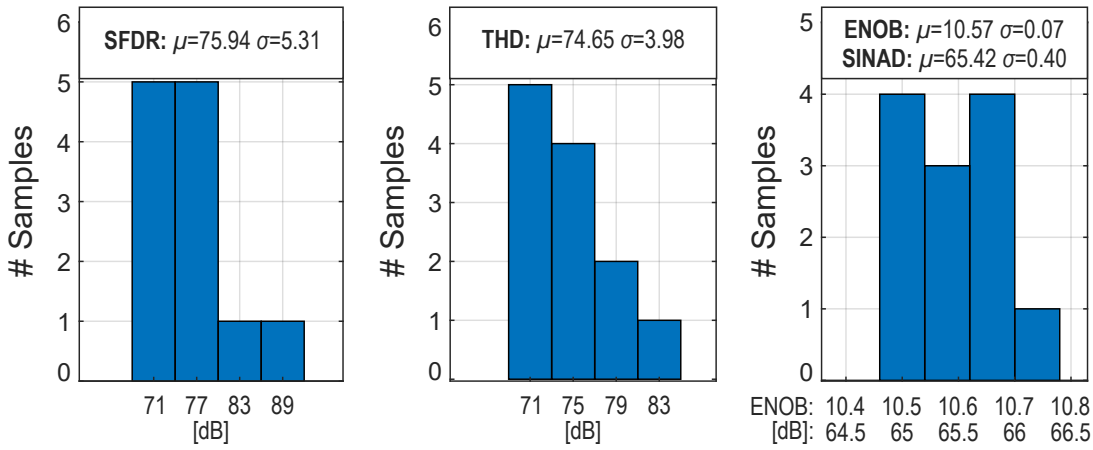


Figure 6.28: Distribution of the Diff-ReDAC multi-dice dynamic performance at 0.8 kHz, 90% swing.

6.4.6 Comparison

Comparing the DiffReDAC with other silicon integrated DACs reported in Table 6.2, the second smallest absolute area is achieved by the Diff-ReDAC, and it is 4.1× than [127], which is tough fabricated in a smaller feature size node.

It also achieves the second smallest normalised area, 2.2× the one of [123], which has 2.6 worse ENOB at comparable sample rate, and 19× smaller than [124].

The Diff-ReDAC is able to operate at the lowest reported supply voltage of 0.45 V by energy-quality scaling, and achieves the second best energy Figure of Merit (FOM) of 172 dB at the nominal supply (only 2 dB less than the oversampled converter [125], which ENOB is A-weighted and power dissipation is 795× higher). The best area-normalised Figure of Merit (FOM_A) is reported in the Diff-ReDAC, evaluated as 178 dB: 29 dB more than current steering [123] and 9 dB more than ΣΔ [125], proving the proposed strategy as an energy-and-area efficient DAC.

Table 6.2: DAC Performance Comparison
[127] [81]

	Diff-ReDAC	[127]	[81]	[106]	[126]	[124]	[123]	[125]
CMOS Tech. F (nm)	180	40	40	180	180	180	350	180
Type	ReDAC	DDPM	ReDAC	ReDAC	cap+mos-string	R-string	curr. steer.	$\Sigma\Delta$
validation	meas.	meas.	sim.	sim.	meas.	meas.	meas.	meas.
Digital Area ($10^6 F^2$)	0.075	0.17	0.30	0.39[a]	N/A	1	N/A	0.62
Area ($10^6 \mu m^2$) / ($10^6 F^2$)	0.00780 / 0.24	0.00127 / 0.79	0.00091 / 0.57	0.01359[a] / 0.42	0.045[b] / 1.39	0.15 / 4.6	0.014 / 0.11	0.10[c] / 3.08
Resolution (bit)	13	12	10	10	10	12	9	N/A
Sample rate (kS/s)	100	110	400	1,450	200	72[d]	111	40[e]
Supply / min.supply (V)	0.6 / 0.45	1 / 0.7	0.6 / N/A	0.7 / N/A	0.6 / N/A	18 / 1.8	3.3 / N/A	1.8 / N/A
INL / DNL (LSB)	1.07 / 0.96	3 / 1	0.33 / 0.2	1.01 / 0.45	0.56 / 0.32	0.54 / 0.26	1.6 / 0.8	N/A
SFDR / THD (dB)	77.81 / 77.52	85 / 85	76.8 / 66.7	59.3 / 59.2	71 / N/A	N/A	N/A	N/A
SINAD (dB)	65.82	72	61.0	58.5	56.43	N/A	48[b]	103[f]
ENOB	10.64	11.6	9.9	9.4	9.08	N/A	8[b]	16.8
Power (μW)	0.88	50.8	0.44	9.15	0.85[b]	875[b]	33	700[g]
†FOM / ‡FOM$_A$ (dB)	172 / 178	160 / 161	176 / 178	166 / 170	165 / 164	N/A	140 / 149	174[f] / 169

$^{\dagger}\mathrm{FOM} = 10\log_{10}\left(\frac{2^{2\cdot \mathrm{ENOB}} BW}{P}\right)$ $^{\ddagger}\mathrm{FOM_A} = \mathrm{FOM} + 10\log_{10}(1/A_F)$ being A_F the F-normalised area [a]includes part of the calibration [b]based on text and figures [c] not including reconstruction filter [d]from row-line time [e]twice the signal bandwidth [f]A-weighted [g]analog power only.

Chapter 7

Direct Digital Sensing Potentiostat targeting Body Dust

The present chapter presents a Direct Digital Sensing Potentiostat (DDSP) potentiostat for electrochemical non-enzymatic glucose sensing targeting the next-generation biosensing in Body Dust particles. The architecture is developed on the base of the Digital-Based Operational Transconductance Amplifier, which working principle is initially revised, and it is modified to merge the OTA-based potentiostat function with a digital-based moving-average A/D conversion. A model for the electrochemical interface is devised and employed to validate the potentiostat by post-layout simulations, proving the effectiveness of the design reporting the tiniest area and smallest power consumption.

7.1 Motivation

As seen in Chapter 1, the implementation of tiny biosensors is more and more desired, not only in commercial wearable and implantable personal

devices, but also in the context pioneering applications such as the Body Dust (BD) concept [56], envisioning the integration of micrometer-scale energy-autonomous devices comparable to the size of human cells (tens of µm range) allowed to circulate in the human body for in-vivo, point-of-care, remote health monitoring and diagnosis (see Fig. 7.1).

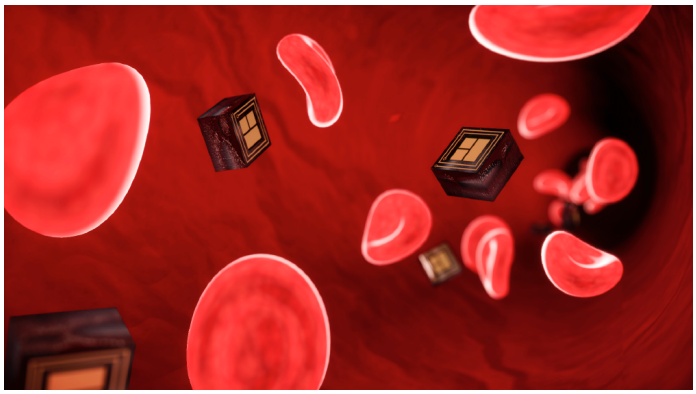


Figure 7.1: Rendered representation of micrometer-scale sensing nodes in human blood vessels, as envisioned by the Body Dust concept. Source [56].

Even if sensors exploiting electrical biological signals (EEG, ECG, EMG, PPG) are very common, electro-chemical (EC) sensors are of relevant interest for biosensor applications as well, detecting biological parameters which are not directly available as electrical quantities.

This is commonly achieved by a Bio-CMOS [15] interface exploiting electrodes which are bio-functionalised (immobilizing on them organic elements i.e. DNA strings, antigens, antibodies, enzymes) which act as transducers between the biological quantity of interest and an electrical quantity (capacitance, impedance, current...) easily measurable in CMOS integrated circuits.

Current-based electrochemical sensors (amperometric sensors) measure the electrons released/required at the sensing electrode as produced by the number of reduction/oxidation (redox) reactions happening at the interface [15]. The electrochemical sensing requires at least two electrodes: a functionalised electrode, commonly referred to as Working Electrode (WE), which may be processed, by nano-fabrication steps (carbon nanotubes, metal nanostructures in the form of nanopetals, nanospheres, nanopores) to enhance the interface sensitivity and selectivity, and a Counter Electrode (CE) providing a low impedance path for the measured current (faradaic current i_F).

It has been demonstrated [128] that nanostructures can enhance the interface sensitivity to the point that the bio-functionalization of the WE with enzymes is no more needed. This type of electrochemical sensing,

referred to as non-enzymatic sensing, is of particular interest due to the ease of fabrication (no organic elements required, possibility to exploit the same sensing hardware for nanostructuration), long-term stability and resilience to ageing.

Amperometric methods catalyse EC reactions by biasing the solution at a fixed potential V_{ref} (chronoamperometry, CA) or by variable potentials such as ramps or sinusoids (cyclic-voltammetry CV, electrochemical impedance spectroscopy EIS) as required by the electrolyte of interest detection.

7.1.1 Potentiostat-based electrochemical sensing

A popular architecture to perform amperometric sensing is the three-electrode electrochemical cell structure, in which a third electrode, the Reference Electrode (RE), is added to WE and CE to bias the solution without sourcing or sinking current from it, thus avoiding biasing errors related to current flowing in the electrical parasitics at the electrode-solution interface, while i_F is measured between the WE and CE.

The three-electrode EC sensing is implemented by potentiostat circuits, which usually exploit the high-impedance input and feedback of CMOS operational amplifiers (opamps) to fix the cell potential with null RE current, as in the potentiostat of Fig. 7.2.

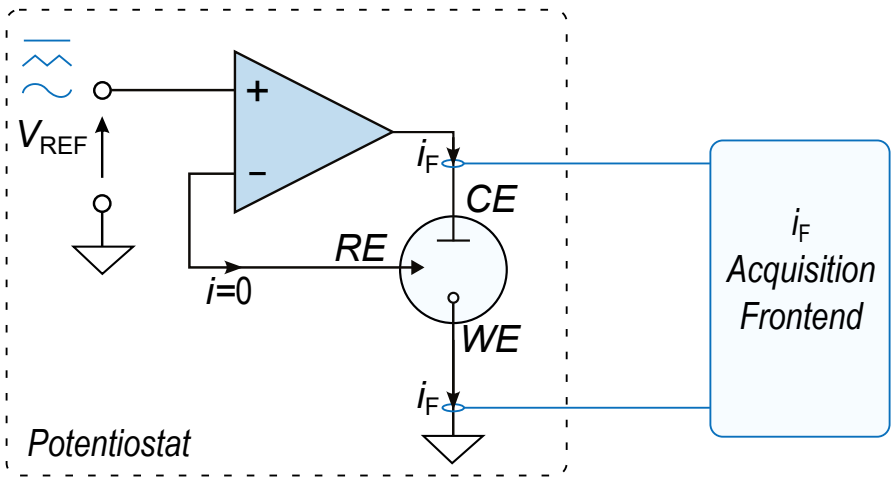


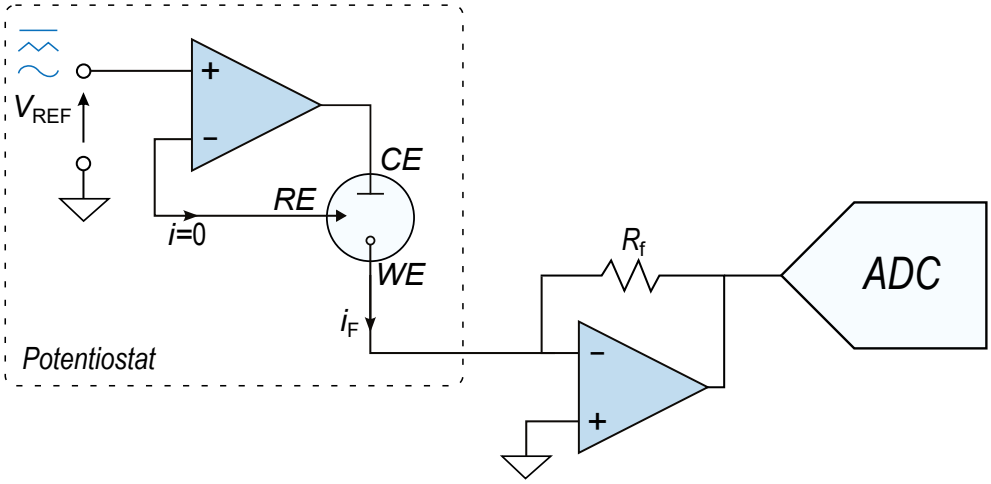
Figure 7.2: General potentiostat architecture with grounded working electrode.

To measure and digitise the current flowing between the CE and WE, additional frontend circuit is usually required. Some common topologies [15] are reported in Fig. 7.3 and Fig. 7.4 [15]. Frontends in Fig. 7.3(a), Fig. 7.3(b) and Fig. 7.4(a) translate the current trough a voltage by transimpedance amplifier, sensing resistor or current mirroring, respectively, followed by an A/D conversion stage. The architecture in Fig. 7.4(b) performs a current-to-frequency and a frequency-to digital conversion by a current-controlled oscillator and a counter.

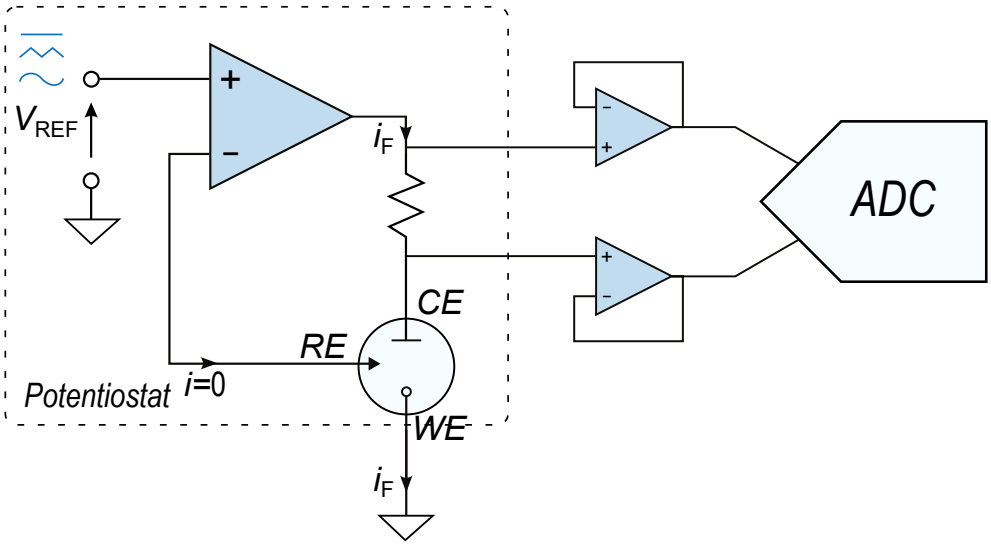
The aforementioned architectures easily require more than one operational amplifier, and an analog-to-digital conversion stage, which imply power consumptions and areas well beyond the ones available in BD applications (nW-power range and hundreds of μm^2 areas), preventing in practice the use of such architectures in BD applications.

A solution to the problem, first presented in [129] and reported in this

chapter, is to avoid the static power implied by linearly-biased operational amplifiers and the need for the additional A/D conversion stage.

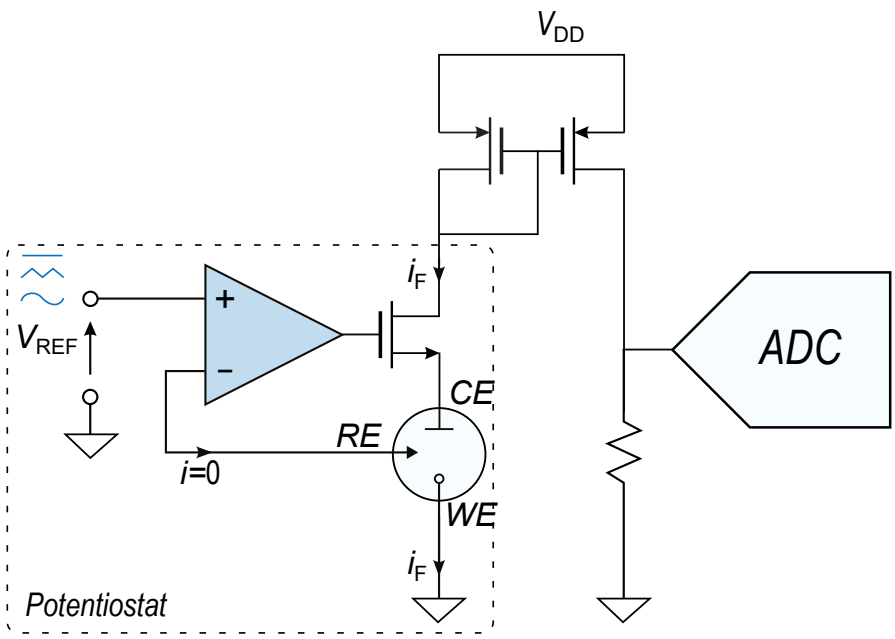


(a)

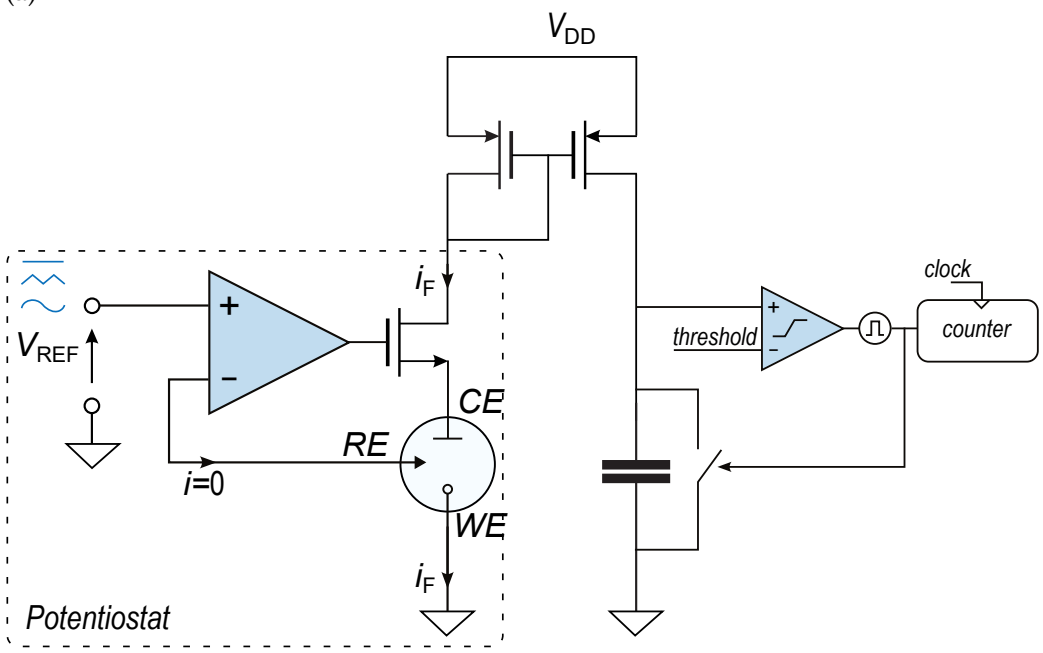


(b)

Figure 7.3: Potentiostat-based electrochemical sensor architectures. Adapted from [15].



(a)



(b)

Figure 7.4: Potentiostat-based electrochemical sensor architectures. Adapted from [15].

7.1.2 Digital-Based OTA working principle

A possible solution to implement operational amplifiers by avoiding their static power dissipation was initially proposed in 2013 [130] with a proof-of concept digital-based analog differential circuit and expanded over the last decade in different implementations of the digital-based operational transconductance amplifier (OTA) [129], [131]–[136].

The Digital-Based Operational Transconductance Amplifier (DB-OTA) has been proposed to perform the analog function af a traditional OTA while being designed by digital-flow, staring from a behavioural description of the analog differential pair in Fig. 7.5(a).

As shown in Fig. 7.5(b), the conventional OTA drives the load C_L by a current proportional to the differential signal $v_d = v^+ - v^-$, while the common-mode component $v_{cm} = (v^+ - v^-)/2$ is sensed and rejected at node A. The current is integrated at the output resulting in an output voltage

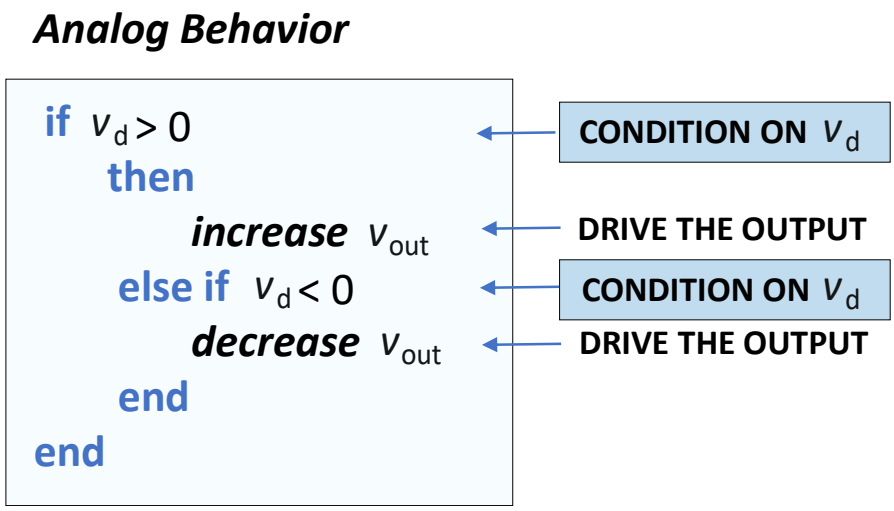
$$v_{out} = \frac{g_m}{C_L} \int_0^{t'} v_d(t')dt' \tag{7.1}$$

With an ideally-infinite g_m, the output is charged/discharged by I_{bias} depending on the sign of v_d.

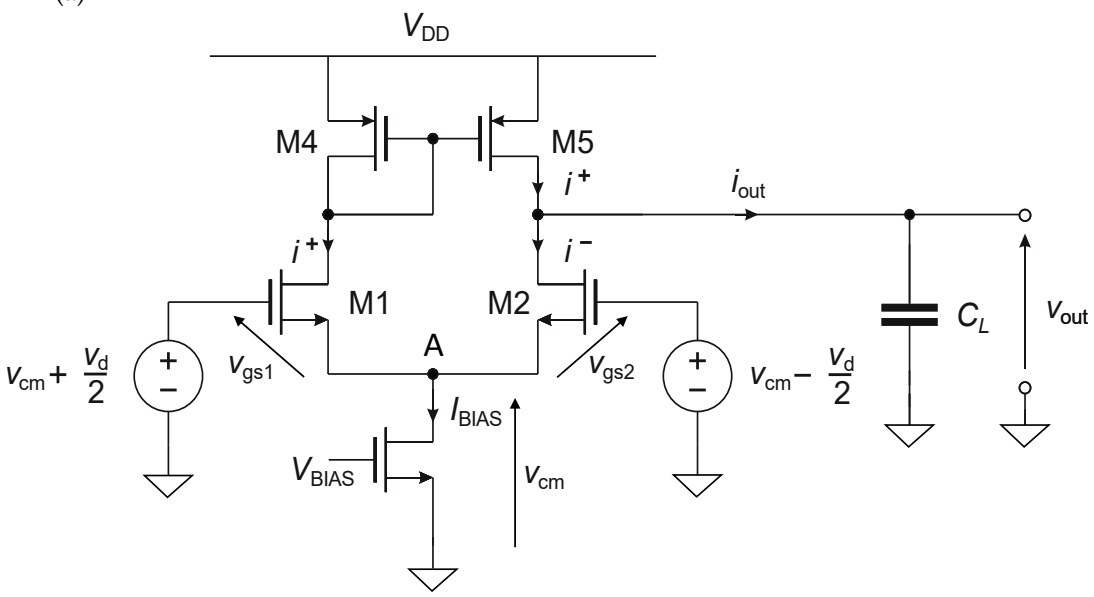
A digital circuit implementing such analog behaviour can be implemented by the circuit in Fig. 7.6(a), where two digital buffers having the same trip point V_T and (ideally) a step threshold behaviour so that, when v_{cm} is close to V_T, the output of the two buffers will either be $OUT^+ = 1$, $OUT^- = 0$ or $OUT^+ = 0$, $OUT^- = 1$, effectively detecting the sign of v_d. Their value drive digital logic to activate a three-state buffer connected to the output and effectively implement the behaviour of Fig. 7.5(a) for what concerns the Differential Mode (DM) voltage v_d. When $OUT^+ = OUT^-$ the sign of v_d can not be determined, but information on the Common Mode (CM) voltage is got based on the values $OUT^+ = 1$, $OUT^- = 1$ ($v_{cm} > V_T$) or $OUT^+ = 0$, $OUT^- = 0$ ($v_{cm} < V_T$), which allows to drive a second three-state buffer (CM extractor) to tracks the CM voltage decreasing (increasing) v_{CMP} (see Fig. 7.6(b)).

In practice, the DB-OTA in Fig. 7.6(a) operates as an operational transconductance amplifier (OTA) when connected in negative feedback configurations.

Different versions of the same circuit have been developed in last years, avoiding the need for a resistive summing network, resulting in a compact fully-digital structure which design can be automated in standard digital design flows [129], [131]–[136].



(a)



(b)

Figure 7.5: Algorithmic representation of the analog OTA behaviour(a) and analog differential circuit (b). Adapted from [130].

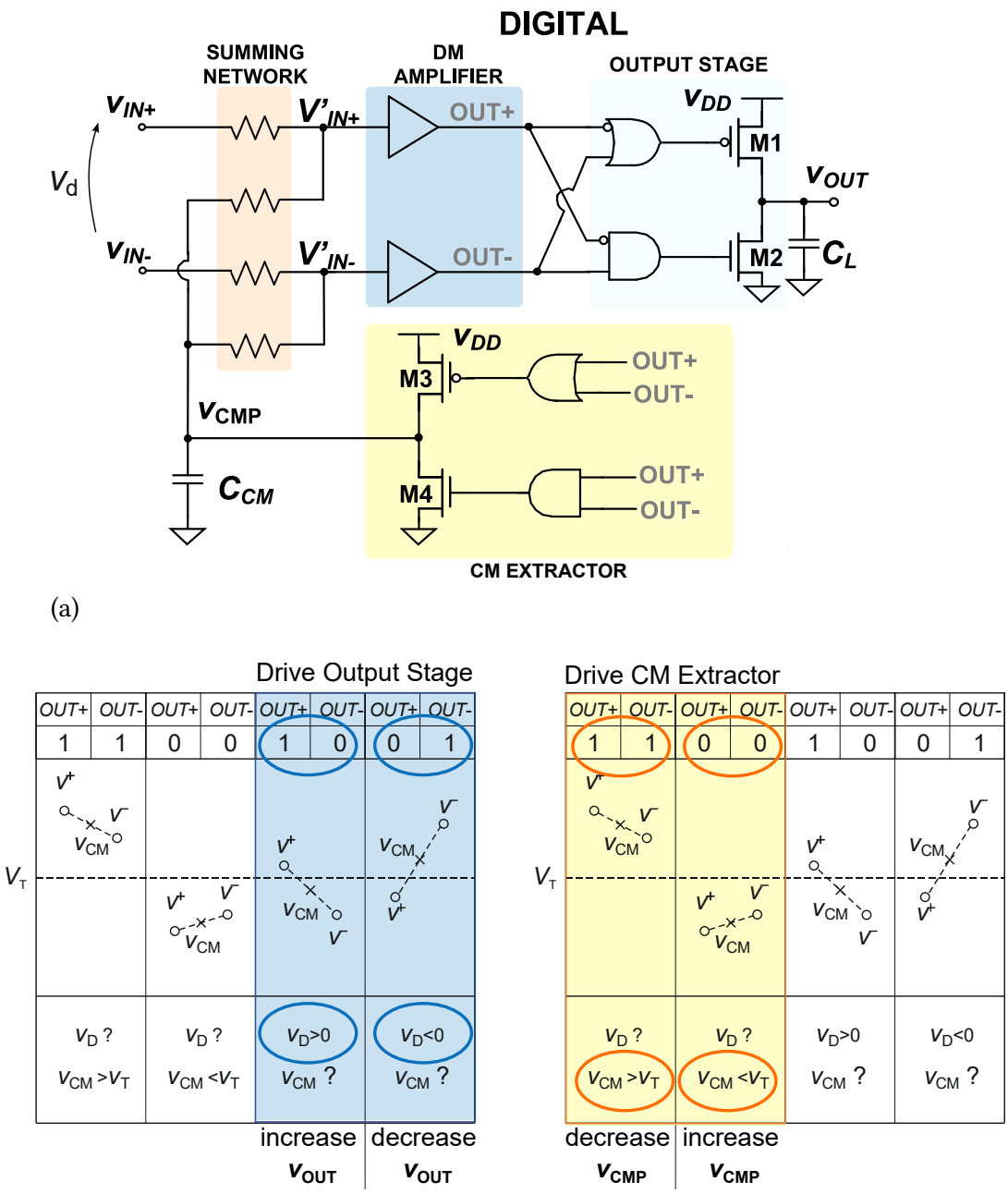


Figure 7.6: First DB-OTA implementation (a). Digital buffers configurations as related to DM and CM operation. Adapted from [130].

7.2 Direct Digital Sensing Potentiostat (DDSP)

The Direct Digital Sensing Potentiostat (DDSP) [129] is designed to perform non-enzymatic glucose sensing in the context of Body Dust by chronoamperometry (CA), i.e. by fixing the solution potential by the RE at constant V_{REF}, while measuring the redox (faradaic) current i_{F} flowing between CE and WE. The sensing is performed by a digitally-intensive architecture, avoiding the need of traditional opamps and the additional, cascaded, acquisition frontend. Those blocks are replaced a compact potentiostat-digitizer combined architecture, represented in the simplified scheme of Fig. 7.7 and discussed in the current section.

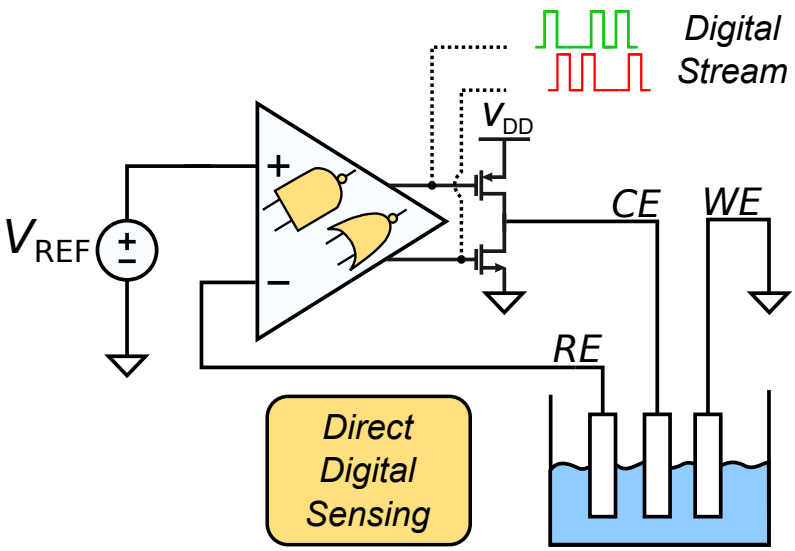


Figure 7.7: High-level diagram of DDSP.

7.2.1 Electrochemical interface modeling and electrodes design

In order to design and simulate the potentiostat, an electrical model of the electrochemical interface is required. To dimension the WE, a sensitivity of

$$S_0 = 4\,A/(\mathrm{mM}\cdot\mathrm{cm}^2) \tag{7.2}$$

is considered, as reported for the fabricated nanostructured (nanospheres) platinum electrode reported in [128] for non-enzymatic glucose sensing [137].

To design a sensor which is compatible in size to BD particles, a square WE of 45 µm-side is chosen, while the overall area for the three WE, CE, RE is 100 µm×100 µm, as in Fig 7.8(a).

The sensitivity of the nanostructured WE, expressed as faradaic current relative to glucose concentration, is de-normalized with respect to te WE area and evaluated as

$$S = \frac{4\,\mu\text{A}}{\text{cm}^2 \cdot \text{mM}} \cdot (0.0045\,\text{cm})^2 = 0.081\frac{\text{nA}}{\text{mM}} \tag{7.3}$$

from (7.2). Considering physiological glucose values in between 3 mM-8 mM range, a full scale of 10 mM (correponding to 0.8 nA current) is chosen.

Once the sensitivity is set, the faradaic current is straightforwardly implemented in simulations as a concentration-driven current source i_F at the WE. Along with the faradaic current, a comprehensive model is provided by the Randles [138] circuit at each electrode, as in Fig. 7.8(b), including a charge transfer resistance R_P and a constant phase element (CPE) C_P modeling the ion layering effect [139] at the electrode surface.

Considering an in vitro test setup using a commercial phosphate-buffered saline (PBS) solution 0.01 M, having conductivity $\sigma_\text{PBS} = 12\,\text{mS/cm}$, the value of R_S is estimated as the resistance of a cube of solution having the side equal to the 45 μm square WE side, i.e.

$$R_\text{S} = \left(\sigma_\text{PBS} \cdot \frac{A}{d}\right) \simeq 18.5\,\text{k}\Omega \tag{7.4}$$

being $A = (45\,\mu\text{m})^2$ and $d = 45\,\mu\text{m}$. The R_P and C_P at the WE and CE (dashed red and dashed blue lines of Fig. 7.8(b)) are modeled by the lumped-elements networks reported in Fig. 7.8(c).

The magnitude and phase curves expected for the designed WE are reported in Fig. 7.8(d) (blue diamonds curves) which are extrapolated from the electrical characterization of platinum microelectrodes in [140], and fit (Fig. 7.8(d), red curves) with the lumped RC model of Fig. 7.8(c) (red dashed box) according to the procedure in [141].

The same procedure has been adopted for the CE as well. For what concerns the RE, the model only includes the solution resistance R_S, since the current flowing trough it is negligible thanks to the high input impedance of the potentiostat.

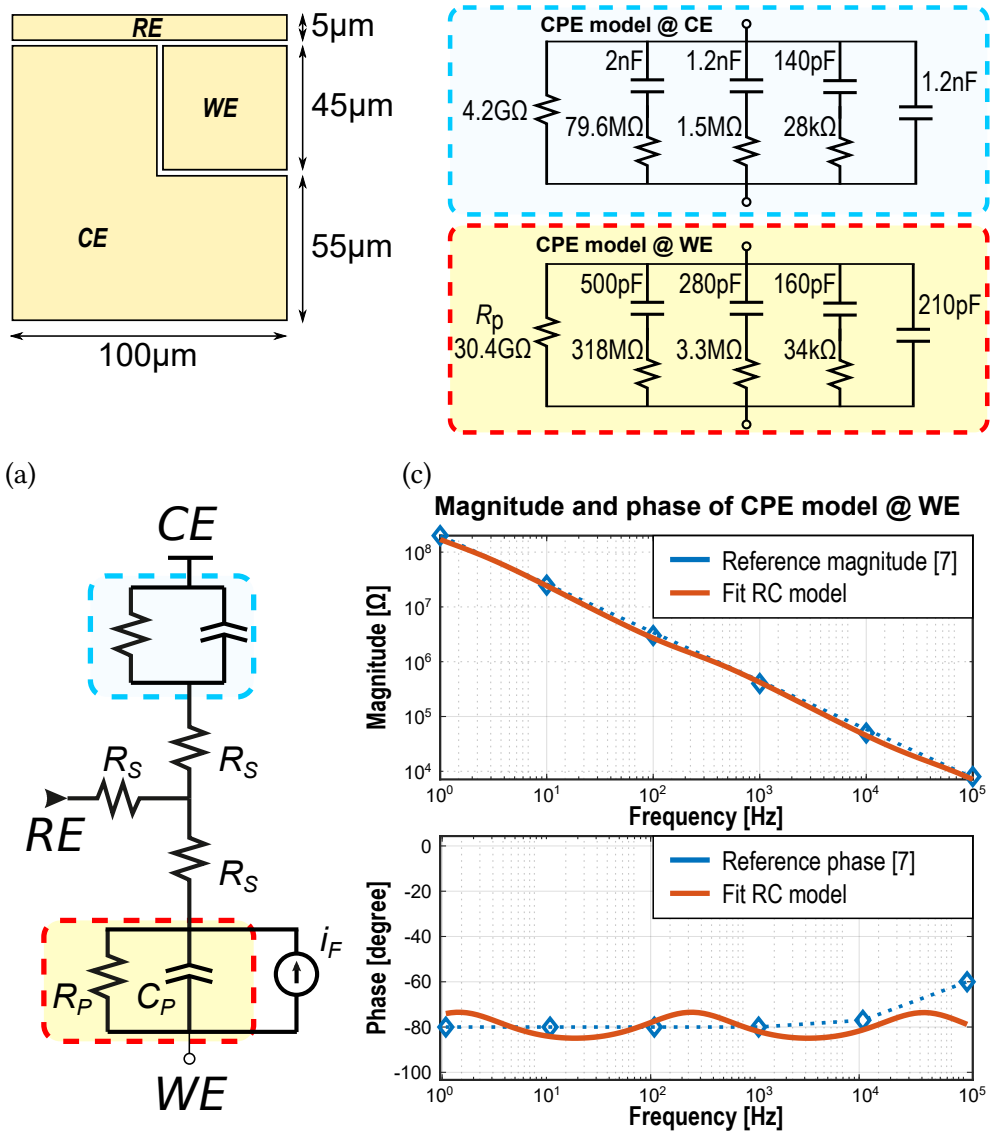


Figure 7.8: Electrode geometries design (a). Sensor interface model at the three electrodes (b) and lumped-element fitting of the CPEs (c). Comparison of the fit model at the working electrode with respect to platinum microelectrodes characterization found in [140] (d).

7.2.2 DDSP architecture and operation

The Direct Digital Sensing Potentiostat (DDSP) here presented is based on the DB-OTA principle, as presented in Section 7.1.2 and its schematic is shown in Fig. 7.9.

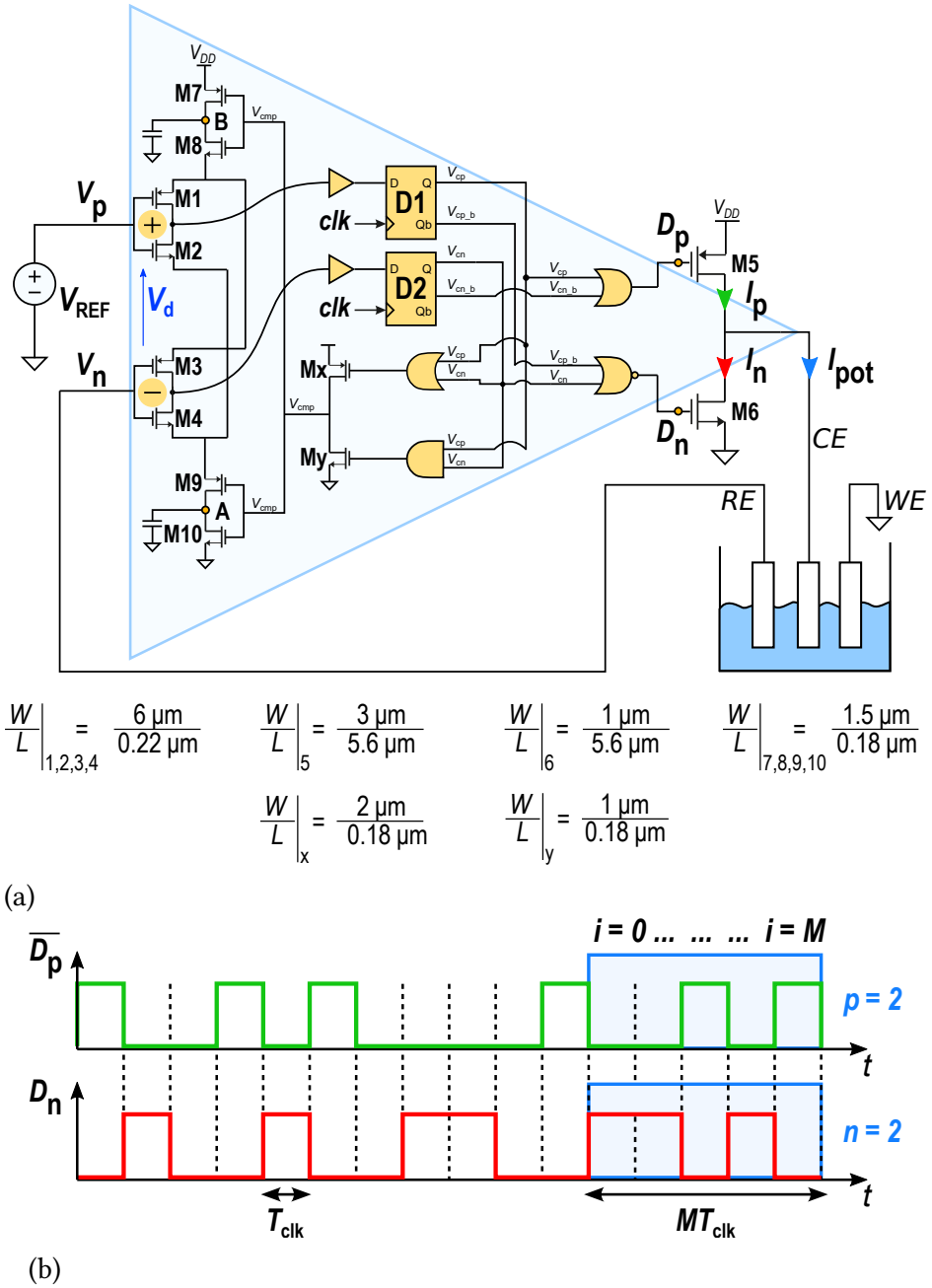


Figure 7.9: Architecture of the Direct Digital Sensing Potentiostat (a) and timing diagram of its digital output stream (b).

Differently from the DB-OTA presented in Section 7.1.2 [130], where the Common Mode (CM) compensation is performed by using a resistor-summing network, or alternatively Muller C elements [131], or eventually a multiplexed-input followed by a CM-compensating series voltage [134], in the DDSP of Fig. 7.9(a) floating inverters [142] are used to keep energy efficiency high.

The positive (v_p) and the negative (v_n) voltage of the differential input, to be connected respectively to the reference voltage V_{REF} and the Reference Electrode (RE), drive the input floating inverters composed of M1-M2 and M3-M4.

The digital regenerated output of these inverters is sampled at constant clock frequency by the D Flip-Flops D1 and D2, respectively. The logic driving the output buffer is equivalent to what seen in Section 7.1.2, so that when D1=0 and D2=1 (D1=1 and D2=0) the sign of v_d is detected to be $v_d = v_p - v_n > 0$ ($v_d \leq 0$ and the three-state buffer composed of M5-M6 is driven to increase (decrease) the output voltage by injecting (sinking) an almost constant current I_P (I_N) to (from) the output CE impedance by turning on M5 (M6) for one clock period T_{clk}, resulting in a positive (negative) charge packet transfer of $I_P T_{clk}$ ($I_N T_{clk}$).

When the value in the flip flops is the same, the differential voltage sign can not be detected and the output stage is kept in high impedance. Indeed, when D1=0 and D2=0 (D1=1 and D2=1) the negative (positive) supply of the floating inverters is connected to node A by M9 (to node B by M8), which parasitic capacitance was, in the previous cycle, pre-discharged to 0 V (pre-charged to V_{DD}) by M10 (M7).

The described behaviour is dynamically biasing the floating inverters to asymmetrically discharge (charge) their outputs depending on the sign of v_d, making the flip-flops resolve in the configuration D1=1, D2=0 or D1=0, D2=1 in the following periods.

The negative feedback configuration of the electrodes in Fig. 7.9(a) makes the RE follow the input V_{REF} due to the charge packets injected into the CE with a ripple error of less than 2.3 mV rms, thanks to the filtering effect of the electrochemical cell itself.

Being the output DDSP stage designed to provide almost constant charge packets, the average output current I_{pot}, equal to the faradaic current I_F, is directly estimated digitally by counting the amount of p (n) pulses at node D_p (D_n) driving the gate of M5 (M6) over the last M clock periods (Fig. 7.9(b)). In terms:

$$I_F = \frac{pI_P - nI_N}{M} \tag{7.5}$$

is the digitised version of the faradaic current obtained without extra A/D fronted, as usually required (see Section 7.1.1), resulting in great saving in terms of area and power.

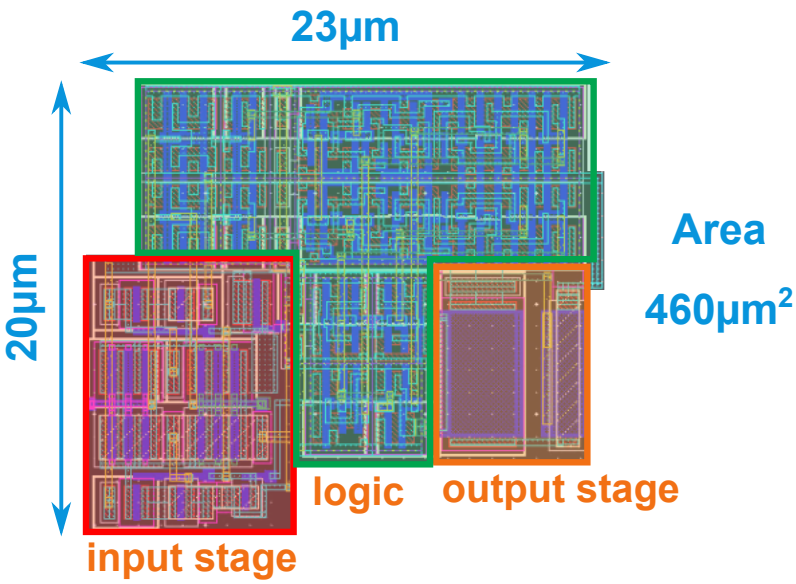


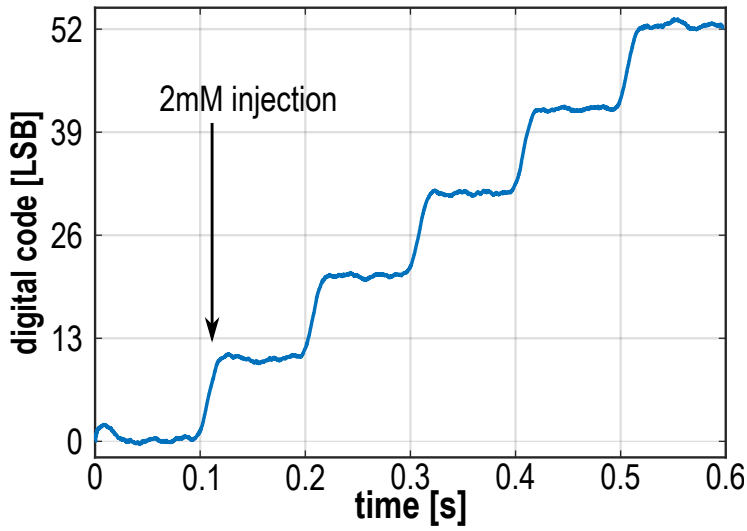
Figure 7.10: DDSP layout with input and output stages highlighted.

7.3 Layout and post-layout simulations

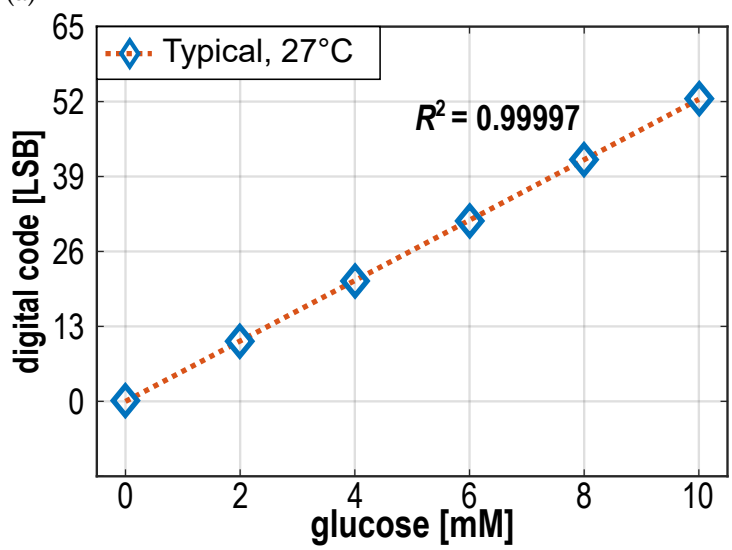
The Layout of the DDSP in 180 nm CMOS technology is reported in Fig. 7.10 and occupies an area of only 460 µm^2. Post-layout simulations have been performed by connecting the potentiostat to the electrochemical cell model developed in Section 7.2.1 and fixing the RE potential at the first oxidation peak of glucose reported in [128], i.e. fixing the WE potential at -0.2 V with respect to the RE, which is equivalent of setting $V_{\mathrm{REF}} = +0.2$ V.

Post layout simulations reveal a tiny DDSP power consumption of 4.7 nW under 0.4 V supply, 50 kHz clock rate, for typical process conditions. The potentiostat current ranges from -22 nA to +33 nA with an input-referred current noise of 65 pA rms, averaged over $M = 3{,}600$ clock periods and including quantization noise, resulting in a dynamic range of 58 dB.

The time-domain potentiostat simulation in CA operation and the resulting chronoamperogram is resported in Fig. 7.11(a), for concentration steps of 2 mM glucose every 100 ms. The related calibration curve in Fig. 7.11(b) reveals a sensitivity of 5.2 LSB/mM with an $R^2 = 0.99997$ evaluated linearity.



(a)



(b)

Figure 7.11: Digital acquisition under 2 mM glucose incremental injections (a) and the related calibration curve (b).

The DDSP operation has been evaluated considering process-related Monte Carlo variations, resulting in a standard deviation for the sensitivity of $\sigma_S = 1.8\,LSB/mM$, represented by the blue cone of Fig. 7.12(a). The worst-case linearity degradation for the code/concentration Monte Carlo samples at $\pm\sigma_S$ is simulated and evaluated as $R^2 = 0.9997$.

Figure. 7.12(a) also reports the calibration curves at ambient temperature and the extreme lower (upper) limit of human body temperature,

i.e. 35°C (40°C). The sensitivity variation in the range 27 °C-40 °C in reported in Fig. 7.12(b). The worst-case linearity degradation is reported from $R^2 = 0.99997$ at 27 °C to $R^2 = 0.9972$ at 40 °C. Process and temperature variations can therefore be compensated by linear calibration, adjusting the coefficients of the digitizing moving average.

The voltage offset distribution under Monte Carlo mismatch variations of the RE electrode is evaluated and reported in Fig. 7.12(c), showing a mean offset $V_{\text{off}} = 3.9\,mV$ with a standard deviation of $\sigma_{\text{off}} = 1.1\,mV$.

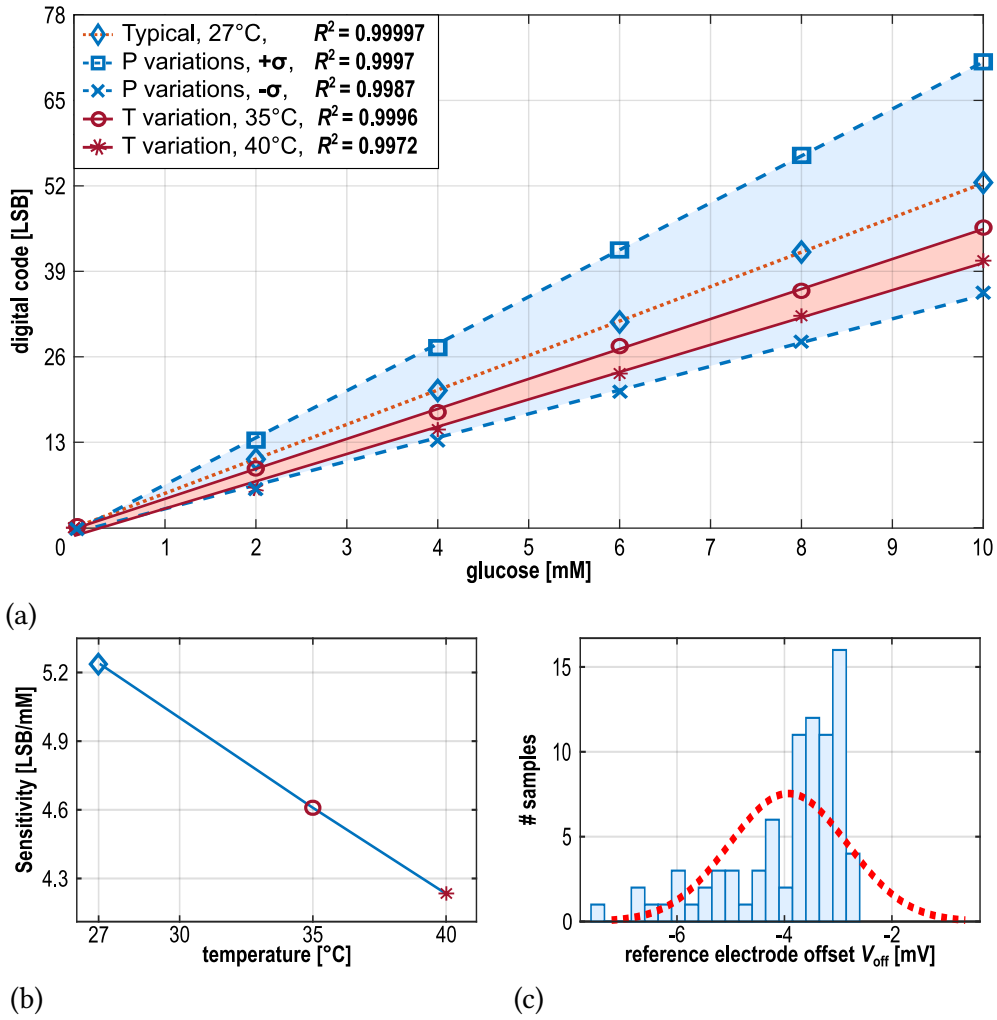


Figure 7.12: Calibration curve under Monte Carlo process (one standard deviation spread) and temperature (ambient and human body temperatures) variations (a) Sensitivity versus temperature (b). RE offset spread under Monte Carlo mismatch (c).

7.4 Comparison

Table 7.1 reports performance comparison of recently-proposed potentiostats for chronoamperometry (CA), cyclic voltammetry (CV), electrochemical impedance spectroscopy (EIS). The DDSP presented in this chapter operate at the lowest supply voltage (3× smaller than [143], [144], 4.5× smaller than [145]) and dissipating the smallest power of 4.7 nW (3,400 × less than [146], [147]) while having the smallest area footprint of 460 μm^2 (150× less than [144], which is also fabricated in a finer technology node).

The presented DDSP reports an input-referred current noise of 65 pA rms, comparable to the one of [146], while having a smaller dynamic range of 58 dB (equal to the one of [143]).

Thanks to its ultra-low power and low voltage operation, very small area and process-temperature-mismatch robustness, the DDSP proves to be an excellent solution and the only viable, to the best of the author's knowledge, to meet the Body Dust strict constraints.

Table 7.1: Potentiostat performance comparison.

	Units	[145]	[146]	[147]	[143]	[144]	DDSP
Method	-	CV,CA,EIS†	CA,CV	CA,CV	CA,CV	CA,CV	CA
Measured	-	yes	yes	yes	yes	yes	no
Current Range	μA	± 0.2	± 5	± 15	$\{-7, +10\}$	± 1.5	$\{-0.022, +0.033\}$
Dyn. Range	dB	104	108	73	58	105	58
Linearity	R^2	-	0.998	-	0.999	0.9990	0.99997
Current Noise	pA (rms)	7.76	41	-	25000	-	65
Bandwidth	Hz	10,000	-	200	50,000	1	7*
Technology	nm	180	180	180	180	65	180
Area	mm^2	0.208	0.78	2.25	3.17	0.07	0.00046
Supply	V	1.8	> 1.1	1.8	1.2	1.2	0.4
Power	μW	311.4	16	73.9	19	25	0.0047
Digital out	-	no	yes	yes	yes	yes	yes

$\star$ Limited by M, traded with noise.

Conclusion

Digital electronics has led, in the last decades, the development of CMOS integrated circuits in finer technologies to increase their performance, reduce area, improve power consumption, translating into performance-cost effectiveness in mass-produced electronics.

At the same time, the design of analog and mixed signals (AMS) blocks has become more and more demanding in terms of effort and design time, while their performance can not keep up with their digital counterpart.

This becomes particularly blatant in applications where ultra low-cost ultra-low power embedded architectures are needed, like Internet of Things (IoT), Internet of Wearables (IoW) and in-vivo biosensing, where the overall processing and sensing power consumption must stay below the micro-watt level, with dimensions below the centimetre scale and cost under the dollar per unit [4].

To meet these requirements, a growing number of architectures have recently been exploiting digitally-intensive solutions to perform traditionally analog and mixed-signals tasks [24], [25].

Hence the motivation to expand the research on digital-in-nature, robust and easily reconfigurable bitstream data converters, together with digital acquisition frontends, as investigated and presented in this thesis. Different configurations of the Relaxation Digital-to-Analog Converter (ReDAC) and a Direct Digital Sensing Potentiostat (DDSP) have been presented, as it is summarized in what follows.

ReDAC-related Contributions

As a first contribution, a complete theoretical analysis of the novel ReDAC has been presented, highlighting the sources of non-idealities, expected energy per conversion, parasitics contribution and general design guidelines.

Next, the first self-calibrated ReDAC implementation based on voltage

controlled oscillators has been proposed and validated by simulations in 40 nm CMOS technology, which occupies a tiny area of 677 μm^2, achieving a competitive 1.08 fJ/(c·s) energy FOM and a self-calibrated linearity of 9.06 ENOB under 0.6 V supply.

The need for a self calibrated hardware implementation has led to two ReDAC prototype on FPGA, reporting 10 bit 10.5 kS/s and 13 bit 514 S/s and exploiting clock-division based digital calibration. The FPGA prototypes allocate only 6 logic elements and are characterized validating by measurement the parasitic error suppression for the first time.

The Radix-Based Digital Correction (RBDC) technique has then been developed as an alternative calibration strategy to avoid the need for clock tuning. A fully synthesizable architecture has been developed and validated in 180 nm CMOS post-layout simulations, achieving comparable performance with respect to other calibration architectures of 9.4 ENOB at 1.45 MS/s. The required RBDC digital area (power) overhead is 5.6× (7.8×, FOM=9.21 fJ/(c.s.)) the one of the ReDAC core block in 180 nm technology, which tough becomes comparable in finer technology nodes thanks to area and power scaling, proving the aim of the digital-intensive approach.

The first silicon implementations of ReDAC converters has been fabricated in 180 nm CMOS technology featuring a DCO-based calibration and embedded in a testing-oriented direct digital synthesizer system. Besides the Single-Ended ReDAC (SE-ReDAC) operating at 10 bit, 880 kS/s, a first differential version (Diff-ReDAC) on 13 bit, 100 kS/s is proposed. The multi-dice characterization of both ReDACs reveals calibration robustness and linearity consistency up to the Nyquist rate, while reporting very good Figure of Merit (FOM) and area-normalised Figure of Merit (FOM_A) compared to other silicon-verified DACs. The ability to keep linearity on a wide supply range and operate at the lowest reported supply of 0.45 V (featuring energy-quality scaling) prove the digitally-intensive ReDAC strategy to achieve ultra-compact, reconfigurable, low-power architectures targeting IoT and IoW interfaces.

ReDAC Achievements and Limitations

Focusing on the presented designs of Relaxation Digital-to-Analog Converters (ReDACs), ultra-low energy per conversion and operation close to the thermal noise limit have been addressed. The developed integrated ReDACs performance are reported in Table C.2, and will be compared to other DAC topologies (see Table C.3) in what follows.

It is not easy to find in literature extensive comparison surveys on D/A converters, nonetheless an insight on ReDACs performance in terms

of energy and accuracy, in relation to the state of the art, is provided in Fig. C.1(a) and Fig. C.2(a) in analogy to what found in the broad work of Murmann [148] on A/D converters, shown in Fig. C.1(b) and Fig. C.2(b).

The plot in Fig. C.1(a) shows how ReDAC designs presented in this thesis lay at the corner between the thermal noise limit and the technological limit, not requiring weighted elements, matched elements or filtering elements, since the ReDAC single (total) capacitance is designed close to the minimum dictated by thermal noise limit, in contrast to DDPM [86], current-steering [123], [149], resistor-string [124], sigma-delta [125] and capacitor-mos [126] DACs. The figure also suggests with an arrow the design direction to be explored with the aim of achieving higher SNDR in ReDACs. Following the "Noise Limited" boundary, the energy per conversion will increase.

Figure C.2(a) shows how the ReDAC architectures in this thesis achieve, on average, competitive Schreier [150] Figure of Merit[1] (FOM) with sample rates ranging from hundreds of kS/s to few MS/s. The plot also highlights how the proposed architecture takes advantage of technology scaling moving from 180 nm (yellow markers) to 40 nm (red markers), validating the digital-based approach and providing insight on how to achieve ReDAC converters of comparable FOM and higher sample rates, as suggested by the arrow in Fig C.2(a).

At the same time, the Schreier [150] Figure of Merit (FOM) versus area, as well as the area-normalised[2] $\mathrm{FOM_A}$ versus power, are employed to sum-up the performance in terms of accuracy, power, bandwidth and area of ReDACs with respect to different DAC architectures and reported in Fig. C.3, proving the ReDAC as an ultra-low area, ultra-low power architecture with best-in-class FOMs.

[1] $\mathrm{FOM} = 10\log_{10}(\frac{2^{2\cdot\mathrm{ENOB}}BW}{P})$

[2] $\mathrm{FOM_A} = \mathrm{FOM} + 10\log_{10}(1/A_\mathrm{F})$, A_F = feature-size normalised area.

Table C.2: Integrated ReDAC Performance Comparison

	[81]	[87]	[106]	[115]	[116]
CMOS Tech. F (nm)	40	40	180	180	180
Type	ReDAC	ReDAC	ReDAC	ReDAC	ReDAC
validation	sim.	sim.	sim.	meas.	meas.
Digital Area ($10^6 F^2$)	0.30	N/A	0.39[a]	0.075	0.075
Area ($10^6 \mu m^2$) / ($10^6 F^2$)	0.00091 / 0.57	0.000677 / 0.42	0.01359[a] / 0.42	0.00503 / 0.15	0.00780 / 0.24
Resolution (bit)	10	10	10	10	13
Sample rate (kS/s)	400	2,000	1,450	880	100
Supply / min.supply (V)	0.6 / N/A	0.6 / N/A	0.7 / N/A	0.65 / 0.6	0.6 / 0.45
INL / DNL (LSB)	0.33 / 0.2	0.72 / 1.27	1.01 / 0.45	1.26 / 0.34	1.07 / 0.96
SFDR / THD (dB)	76.8 / 66.7	62.4 / 62.2	59.3 / 59.2	72.18 / 65.59	77.81 / 77.52
SINAD (dB)	61.0	58.3	58.5	56.09	65.82
ENOB	9.9	9.4	9.4	9.02	10.64
Power (μW)	0.44	1.46	9.15	3.3	0.88
†FOM / ‡FOM$_A$ (dB)	176 / 178	175 / 179	166 / 170	166 / 175	172 / 178

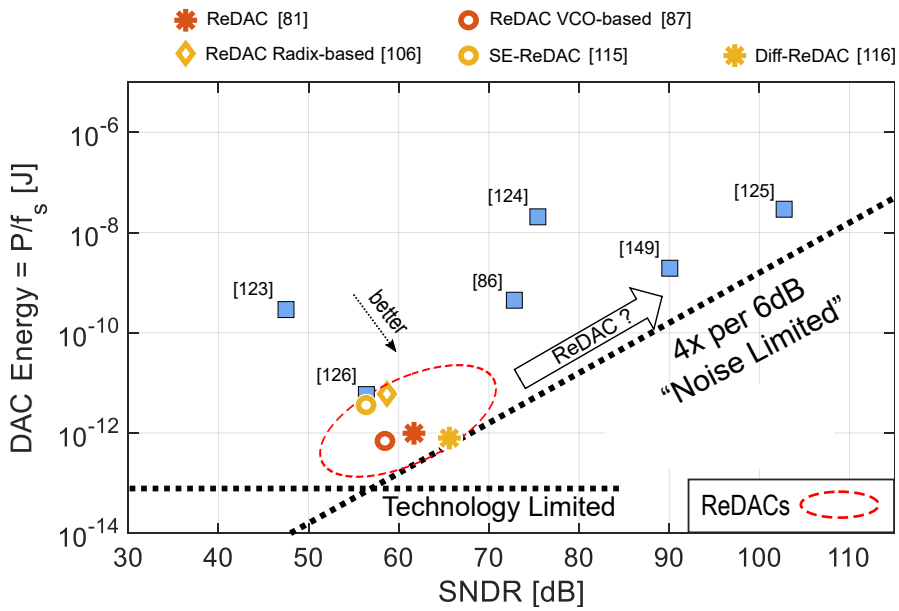
Table C.3: Comparison among different DAC Topologies

	[86]	[126]	[124]	[123]	[125]	[149]
CMOS Tech. F (nm)	40	180	180	350	180	130
Type	DDPM	cap+mos-string	R-string	curr. steer.	$\Sigma\Delta$	curr. steer.
validation	meas.	meas.	meas.	meas.	meas.	meas.
Digital Area ($10^6 F^2$)	0.17	N/A	1	N/A	0.62	N/A
Area ($10^6 \mu m^2$) / ($10^6 F^2$)	0.00127/0.79	0.045[a] / 1.39	0.15 / 4.6	0.014 / 0.11	0.10[b] / 3.08	N/A
Resolution (bit)	12	10	12	9	N/A	6
Sample rate (kS/s)	110	200	72[c]	111	40[d]	2,200
Supply / min.supply (V)	1/0.7	0.6 / N/A	18 / 1.8	3.3 / N/A	1.8 / N/A	1.5
INL / DNL (LSB)	3 / 1	0.56 / 0.32	0.54 / 0.26	1.6 / 0.8	N/A	N/A
SFDR / THD (dB)	85 / 85	71 / N/A	N/A	N/A	N/A	N/A
SINAD (dB)	72	56.43	N/A	48[a]	103[e]	90.25
ENOB	11.6	9.08	N/A	8[a]	16.8	14.7
Power (μW)	50.8	0.85[a]	875[a]	33	700[g]	9,000
†FOM / ‡FOM$_A$ (dB)	160 / 161	165 / 164	N/A	140 / 149	174[f] / 169	172 / N/A

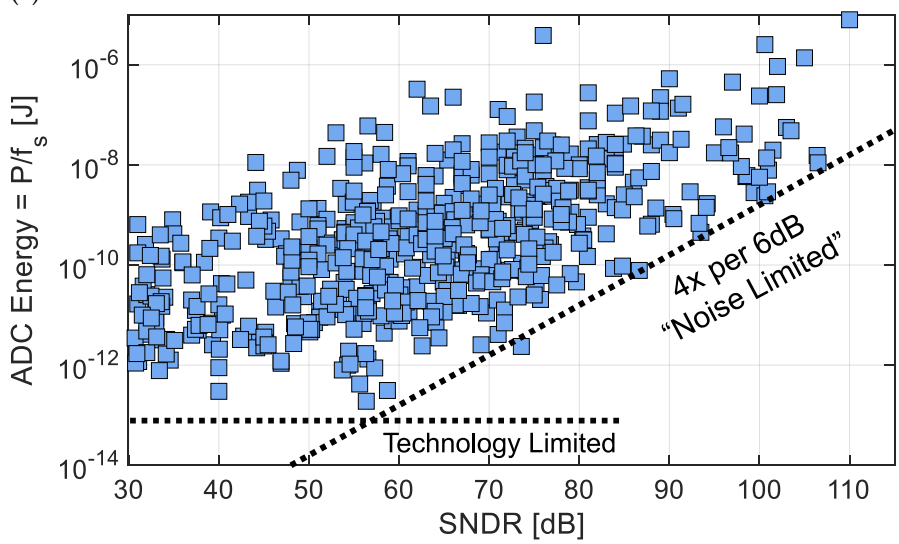
$^{\dagger}\mathrm{FOM} = 10\log_{10}\left(\frac{2^{2\cdot\mathrm{ENOB}}BW}{P}\right)$ $^{\ddagger}\mathrm{FOM_A} = \mathrm{FOM} + 10\log_{10}(1/A_F)$ being A_F the F-normalised area

[a] based on text and figures [b] not including reconstruction filter [c] from row-line time

[d] twice the signal bandwidth [e] A-weighted [f] analog power only.

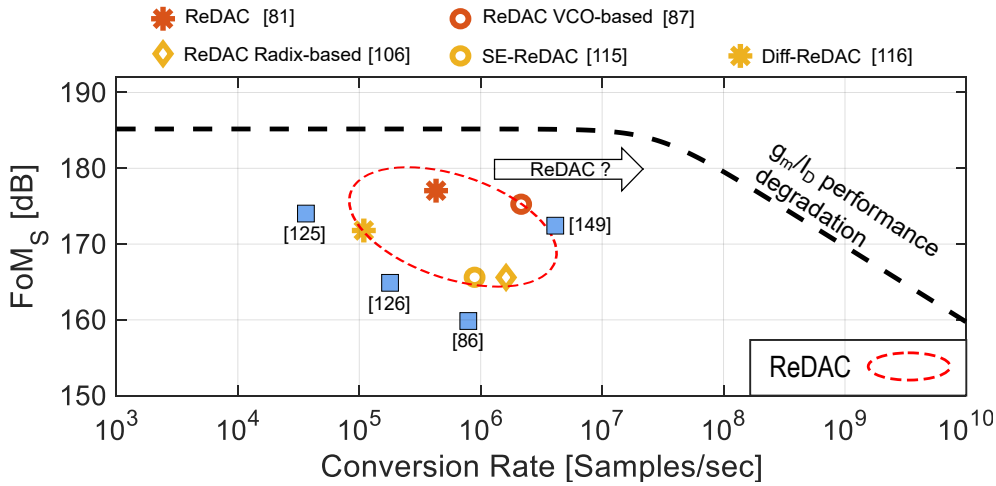


(a)

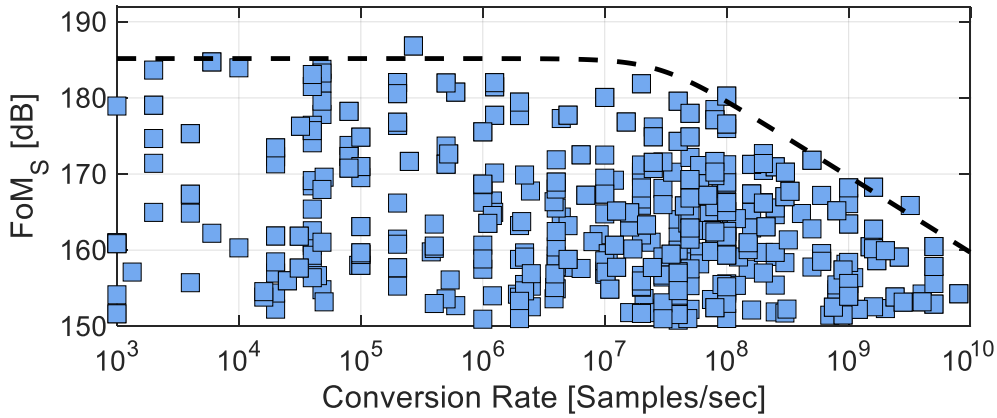


(b)

Figure C.1: Comparison of DAC energies versus SNDR (a) in analogy to the ADC energies versus SNDR in Murmann's [148] survey (b).



(a)



(b)

Figure C.2: Comparison of DAC Schreirer FOMs versus sample rate (a) in analogy to the ADC Schreirer FOMs versus sample rate in Murmann's [148] survey (b).

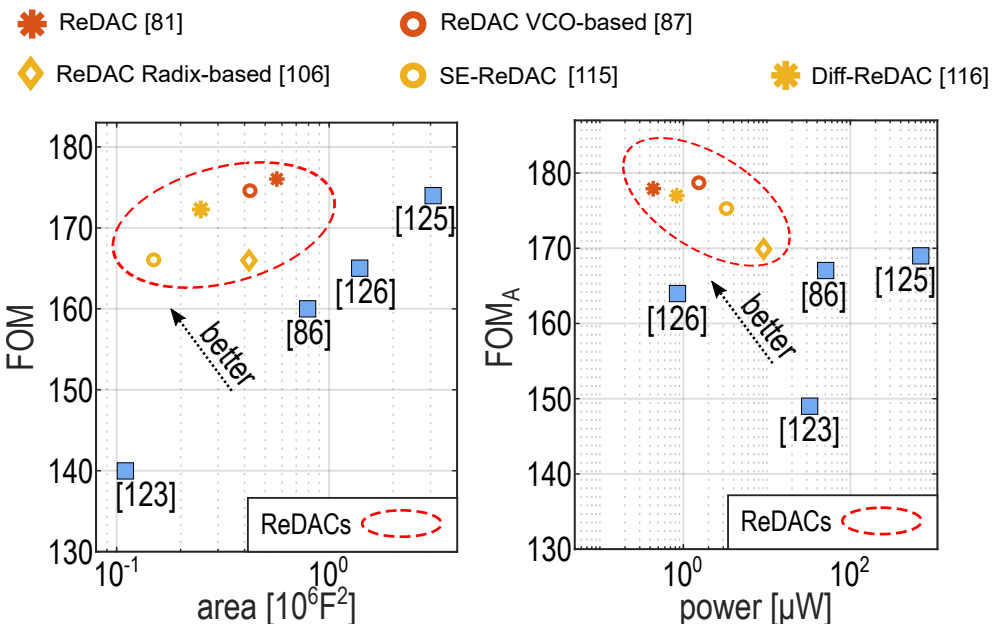


Figure C.3: Comparison of ReDAC with state of the art based on FOM versus area and area-normalised FOM_A versus power.

Some limitations will have to be addressed when targeting ReDACs with higher resolution or higher sample rates. Concerning the ReDAC accuracy, a parasitics error suppression has already been presented to enhance linearity, taking into account the second-order effects in the impulse response of the RC network. In practice, once calibration and the parasitics error suppression have been applied, a residual nonlinearity shows in the INL which can be fit by cubic or quadratic bows (see e.g. the residual nonlinearity in the SE-ReDAC reported in Fig. C.4), which sets an upper bound to the achievable SNDR [148]:

$$SNDR \leq -20 \log \left(\frac{\mathrm{INL_{fit}}}{2^N} \right). \tag{C.6}$$

In the ReDAC this is addressable to the nonlinear loading effect of the three-state buffer, which may be reduced employing body-driven transistors or feedback-enhancing the three-state buffer output impedance.

The accuracy of ReDACs at higher sample rates (tens of MS/s) will inevitably be limited by transition times in the output stream of bits, which is ultimately technology-constrained.

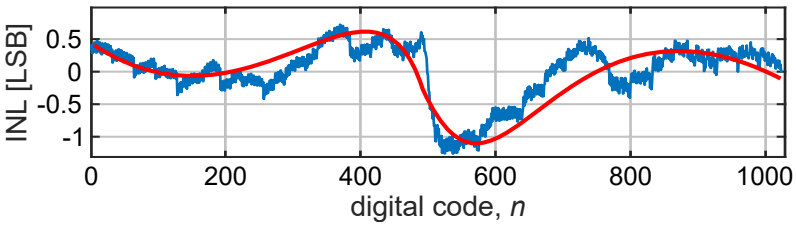


Figure C.4: .

Contributions in Frontends targeting Next-Generation Biosensing

In the context of digital-based frontends for the next-generation biosensing targeting Body Dust, a fully-digital Direct Digital Sensing Potentiostat (DDSP) for electrochemical, non-enzymatic, glucose sensing has been designed and verified in 180 nm post-layout simulations. The architecture reports high linearity under process-mismatch-voltage variations with a power consumption of 4.7 nW (3,400× less then the minimum reported) at the smallest area (150× smallest than the minimum reported) and the lowest supply of 0.4 V, by effectively exploit the Digital-Based Operational Transconductance Amplifier (DB-OTA) concept to join the potentiostat and the A/D conversion functions, conventionally separately implemented in state-of-the-art architectures.

Further contributions which have not been discussed in this thesis, is the experimental characterization of an ultra low-voltage, ultra low-power acquisition frontend from biomedical and audio applications, designed by Crovetti and Toledo [134].

Future developments

There is still a wide margin for research concerning the digital-based approach applied to AMS blocks targeting IoT and next-generation biosensing interfaces, both at the system and at the block-level, including the implementation of the ReDAC architecture as a feedback DAC in SAR or ΣΔ ADCs [29], as well as in digitally assisted calibration architectures. The ReDAC is a promising architecture to reach audio-quality performance (16 bit) without the need for noise shaping, thanks to the consistent Nyquist-rate linearity and the natural filtering of the human hear (A-weighting). The possibility to exploit the ReDAC at higher sample rates (tens of MHz) with possibly lower resolutions (6 bit-8 bit) in short-range

IoT RF transceivers (i.e. Bluetooth, Bluetooth-LE) has to be addressed. The integration of the ReDAC as reference/signal generator in ultra-compact low-power biosensors, as required e.g. by amperometric sensors (CA, CV) and electrochemical impedance spectroscopy (EIS). Finally, a silicon implementation of the digital-based potentiostat is advisable to fully validate its effectiveness in the framework of Body Dust sensing.

Appendix A

Shannon and Shannon-Rack Decoders

As introduced in Chapter 2, after the publication of the first ReDAC implementation [30], the authors found that a condition similar to the one required by linear ReDAC operation, i.e. $T = T^* = \tau \log 2$ (2.4 in Chapter 2), had been exploited by C. E. Shannon in a 1948 [78] Pulse Code Modulation Decoder (Shannon decoder), and later modified by A. J. Rack (Shannon-Rack decoder) to make the decoder less sensitive to the timing jitter. The architectures are briefly described in what follows and highlight the differences with respect to the Relaxation Digital-to-Analog Converter (ReDAC).

Operating Principle

The Shannon and Shannon-Rack decoders fall in the category of cyclic serial DACs [151], as their operation relies on the digital bits of the digital word provided in the correct serial order (LSB-first in this case).

The 4-bit Shannon decoder in Fig. A.1 operates as follows. In the example, the digital word 1011 is converted: the bits of the digital word drive at constant rate, for a small fraction of the period, the switch of the regulated current source injecting a constant charge in the parallel RC network (the vertical axis in Fig. A.1 is the voltage across the RC normalised with respect to the voltage change produced by a single charge pulse). If the

bit corresponding to the current pulse is zero, no charge is injected.

If the time period T between consecutive PCM pulses is chosen so that $T = RC \log 2$, the capacitor voltage at the end of each period is $1/2$ the initial value in the same period. When such condition is met, after the last pulse, the voltage across the RC is sampled and it is proportional to the digital input code.

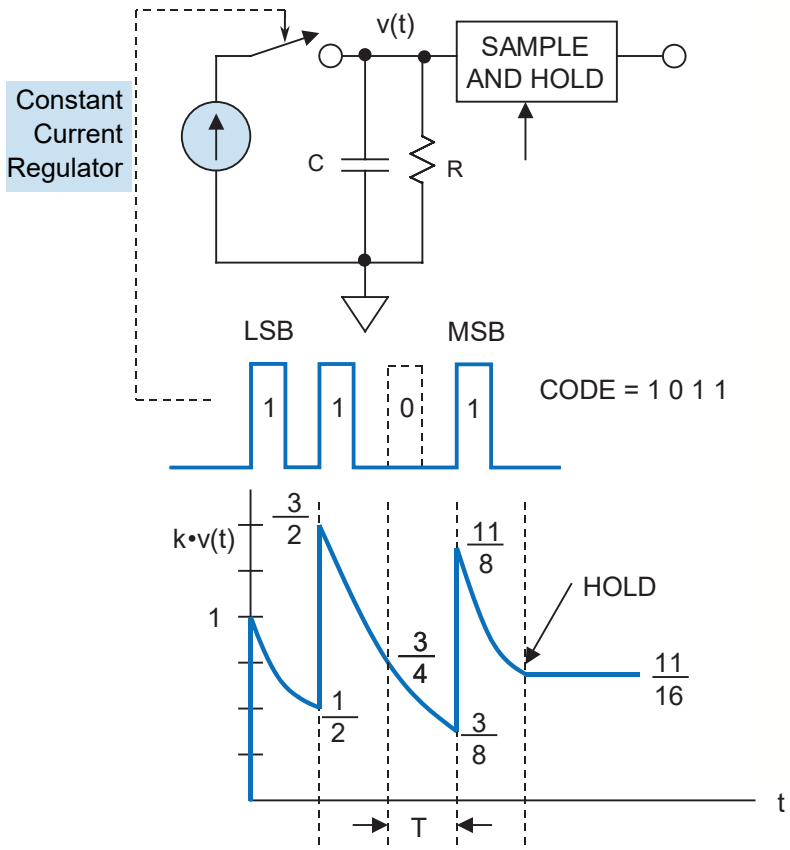


Figure A.1: .

The Shannon-Rack decoder in Fig. A.2 operates according to the same principle: The RLC network is designed to attenuate the output voltage of a factor $1/2$ at each period and, at the same time, resonate at the frequency $f_{\mathrm{RLC}} = 1/T$. The resonance makes the time derivative of the voltage to be zero at the beginning of each pulse, thus reducing the sensitivity of the decoder to timing jitter of the pulses or in the sample and hold circuit.

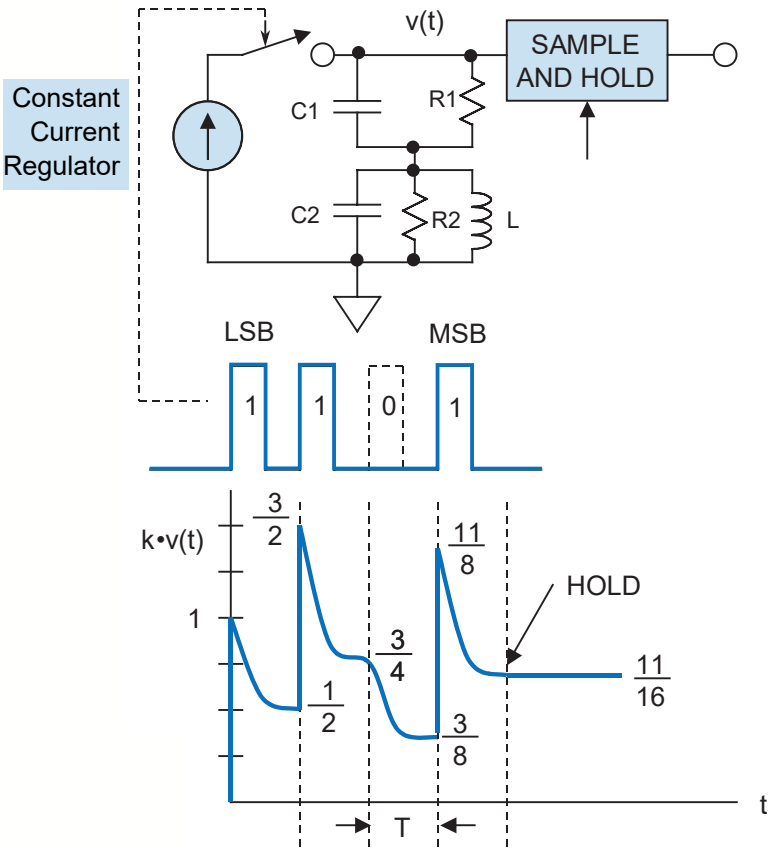


Figure A.2: .

Comparison to the ReDAC

In Fig. A.3(a) and Fig. A.3(b) al possible waveform on seven periods of the ReDAC and the Shannon-Rack decoder, respectively, are shown. Even tough the two architectures exploit similar principles, they differ in several aspects:

- the ReDAC exploit the natural response of the passive network both in charge and discharge, since its resistor can be connected to V_{DD} or 0 V, while the Shannon (Shannon-Rack) decoder exploits only the waveform related to the discharge of the passive network;
- the Shannon (Shannon-Rack) decoder, requires an additional regulated current source which adds complexity and a possible source of nonlinearities.
- to achieve linear operation the Shannon decoder has to meet, in practice, not only the condition $T = \tau \log 2$ but precisely control the

pulse width controlling the constant-current charge of the passive network;

- even if the jitter-related errors at the sampling instant are mitigated by the resonating Shannon-Rack passive network, the jitter related errors related to the constant-current charge pulse are not improved by the technique;
- the Shannon-Rack decoder requires additional inductor which is undesirable in fully integrated solutions.

The described Shannon (Shannon-Rack) decoder drawbacks are certainly mostly related to the available technology and the architecture they were aiming at the time. Nonetheless, their implementation in nowadays integrated circuits would be impractical to meet the area, cost, and power requirements as targeted by the ReDAC architecture.

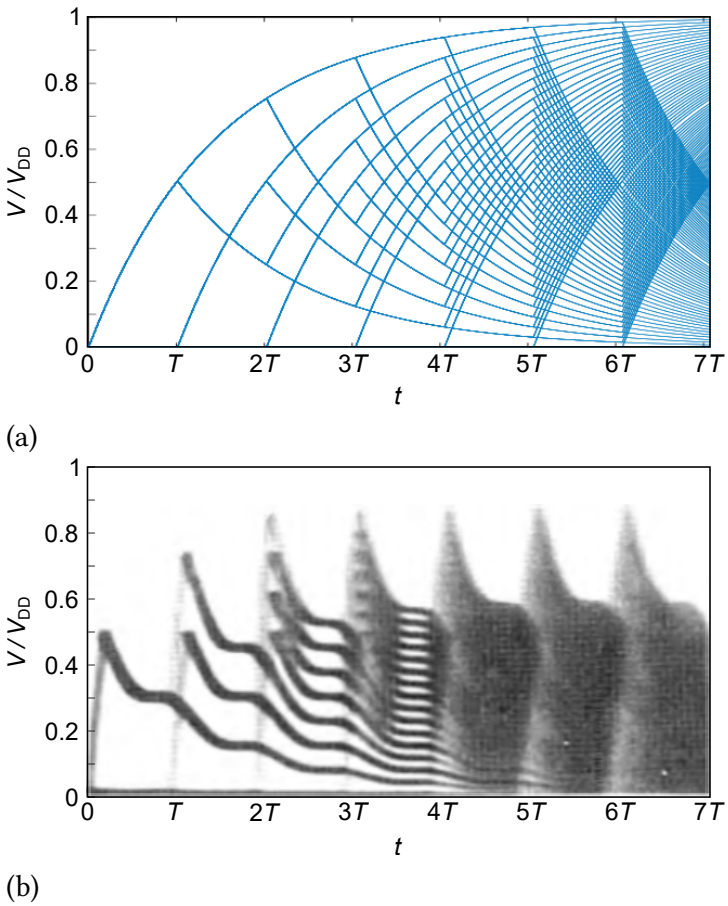


Figure A.3: Superimposed waveforms on 7 periods of the ReDAC converter (a) and of the Shannon-Rack Decoder (b), adapted from [78].

Appendix ***B***

Published Papers and Awards

Journal Papers:

- P. Crovetti, **R. Rubino**, and F. Musolino, "Relaxation digital-to analogue converter," Electronics Letters, vol. 55, no. 12, pp. 685–688, 2019. doi: https://doi.org/10.1049/el.2019.0784.
- P. Crovetti, F. Musolino, O. Aiello, P. Toledo, and **R. Rubino**, "Breaking the boundaries between analogue and digital," Electronics Letters, vol. 55, no. 12, pp. 672–673, 2019.
  doi: https://doi.org/10.1049/el.2019.1622.
- **R. Rubino** S. Crovetti, and F. Musolino, "FPGA-Based Relaxation D/A Converters With Parasitics-Induced Error Suppression and Digital Self-Calibration," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 6, pp. 2494–2507, 2021.
  doi: 10.1109/TCSI.2021.3064419.
- P. Toledo, **R. Rubino**, F. Musolino, and P. Crovetti, "Re-Thinking Analog Integrated Circuits in Digital Terms: A New Design Concept for the IoT Era," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 3, pp. 816–822, 2021.
  doi: 10.1109/TCSII.2021.3049680.

Conference Papers:

- **R. Rubino**, P. S. Crovetti, and O. Aiello, "Design of Relaxation Digitalto-Analog Converters for Internet of Things Applications in 40nm CMOS," in 2019 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), 2019, pp. 13–16.
  doi: 10.1109/APCCAS47518.2019.8953168.

- P. S. Crovetti, **R. Rubino**, and F. Musolino, "Relaxation Digital-to-Analog Converter with Foreground Digital Self-Calibration," in 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020, pp. 1–5.
  doi: 10.1109/ISCAS45731.2020.9180696.

- **R. Rubino**, F. Musolino, and P. Crovetti, "Relaxation Digital-to-Analog Converter with Radix-based Digital Correction," in 2022 IEEE International Symposium on Circuits and Systems (ISCAS), 2022, pp. 1402–1406.
  doi: 10.1109/ISCAS48785.2022.9937502.

- **R. Rubino**, S. Carrara, and P. Crovetti, "Direct Digital Sensing Potentiostat targeting Body-Dust," in 2022 IEEE Biomedical Circuits and Systems Conference (BioCAS), 2022, pp. 280–283.
  doi: 10.1109/BioCAS54905.2022.9948649.

- P. Crovetti, **R. Rubino**, P. Toledo, and F. Musolino, H. Klimach, Y. Chen, A. Richelli "A 0.01mm2, 0.4V-VDD, 4.5nW-Power DC-Coupled Digital Acquisition Front-End Based on Time-Multiplexed Digital Differential Amplification," ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC), Milan, Italy, 2022, pp. 405-408, doi: 10.1109/ESSCIRC55480.2022.9911357.

- S. Adibi, **R. Rubino**, P. Toledo, and P. Crovetti, "Design of an Analog and of a Digital-Based OTA in Flexible Integrated Circuit Technology," in 2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2022, pp. 1–4.
  doi: 10.1109/ICECS202256217.2022.9970904.

- P. Crovetti, **R. Rubino**, A. Abdullah, and F. Musolino, "Emerging Relaxation and DDPM D/A Converters: Overview and Perspectives," in 2022 IEEE 65th International Midwest Symposium on Circuits and Systems (MWSCAS), 2022, pp. 1–6.
  doi: 10.1109/MWSCAS54063.2022.9859310.

- **R. Rubino**, F. Musolino, P. Toledo, Y. Chen, A. Richelli, and P. Crovetti, "A 880 nW, 100 kS/s, 13 bit Differential Relaxation-DAC in 180 nm," in 2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), 2023.
- **R. Rubino**, F. Musolino, P. Toledo, Y. Chen, A. Richelli, and P. Crovetti, "A 5,030 µm2-area, 3.3 µw-power, 880 ks/s, 10-bit Relaxation Dac in 180 nm," *Currently submitted to:* IEEE Transactions on Circuits and Systems II: Express Briefs, 2023.

Awards

- *Gold Leaf Certificate*, for the paper entitled "A 880 nW, 100 kS/s, 13 bit Differential Relaxation-DAC in 180 nm,", awarded to the top 10% papers submitted to the *Ph.D Research in Microelectronics and Electronics (PRIME)* conference, Valencia, Spain, 2023.

Supervised M.Sc. Thesis:

- Andrea Malacrino. "Progetto di un oscillatore in tecnologia CMOS a 65 nm per applicazioni Internet of Things: Design of a 65 nm technology CMOS oscillator for Internet of Things applications.", 2020. Supervisors: Paolo Crovetti, Roberto Rubino.
- Gabriel Steven Romero Rondon. "Design and silicon implementation of virtual voltage reference circuits.", 2022. Supervisors: Paolo Crovetti, Roberto Rubino.
- Sogand Adibi. "Design of a digital-based OTA in flexible integrated circuit technology.", 2022. Supervisors: Paolo Crovetti, Roberto Rubino.
- Andrea De Gregorio. "Design of an Ultra-Low-Power Digital-Based Potentiostat for Wearable Biosensors", 2023. Supervisors: Paolo Crovetti, Roberto Rubino, Danilo Kaddouri.

Acronyms

A/D analog-to-digital. 15, 19, 27, 53, 54, 58, 73, 92, 97, 123, 133, 136, 137, 147, 153, 159

ADC Analog-to-Digital Converter. xiii, 6, 14–16, 19, 58, 66, 67, 87, 92, 159

AI Artificial Intelligence. 23

AMS analog and mixed signals. 9, 13, 29, 66, 97, 151, 159

ASICs Application-Specific Integrated Circuits. 24, 66

BAN body area networks. 10

BD Body Dust. 21, 27, 133, 134, 136, 142, 143, 150, 159, 160

BWA Bynary Weighted DAC with Attenuation capacitor. 51

CA chronoamperometry. 12, 135, 142, 147, 150, 160

CBW Conventional Bynary Weighted capacitors DAC. 51

CE Counter Electrode. 134, 136, 142, 143, 146

CM Common Mode. 139, 146

CMOS complementary metal-oxide semiconductor. 4, 23, 26, 29, 83, 93, 94, 97, 98, 110, 126, 134, 136, 151, 152

CPE constant phase element. xvii, 143, 144

CV cyclic voltammetry. 12, 98, 135, 150, 160

D/A digital-to-analog. 15, 19, 53, 67, 81, 84, 92, 98, 152

DAC Digital-to-Analog Converter. xiii, 1, 6, 15, 16, 19, 26, 29, 32, 38, 51–54, 66, 74, 81, 83–85, 87, 98, 105, 115, 118, 121, 130, 152, 153, 159, 161

DB-OTA Digital-Based Operational Transconductance Amplifier. 27, 133, 139, 145, 146, 159

DC direct-current. 105

DCO digitally controlled oscillator. 26, 39, 97, 98, 101, 102, 120, 121, 152

DDPM Dyadic-Digital Pulse Modulator. 19, 66, 81, 118, 153

DDSP Direct Digital Sensing Potentiostat. xvii, 27, 133, 142, 145–148, 150, 151, 159

DM Differential Mode. 139

DNL diferential nonlinearity. 33–35, 42, 44, 51, 60, 78, 94, 108, 114, 121, 127

DPWM Digital Pulse-Width Modulation. 19, 66, 81

DSP Digital Signal Processor. 93

EC electro-chemical. 134–136

ECG electrocardiography. 12, 134

EDA Electronic Design Automation. 24

EEG electroencephalography. 12, 134

EIS electrochemical impedance spectroscopy. 12, 98, 135, 150, 160

EMG electromyography. 12, 134

ENOB Effective Number Of Bits. 26, 77, 78, 81, 94, 114–116, 118, 127, 129, 130, 152

FFT Fast Fourier Transform. 81

FOM Figure of Merit. 26, 94, 97, 118, 130, 152, 153

FPGA Field Programmable Gate Array. 26, 45, 65–67, 73, 74, 81, 98, 114, 126, 152

FSM finite-state machine. 92, 109

GBW gain-bandwidth product. 105

GPIO General Purpose Input Output. 74

HDL Hardware Description Language. 66, 74

I/O input-output. 74

IC Integrated Circuit. 97, 113, 114

ICs Integrated Circuits. 2, 65

IMU integrated motion unit. 14

INL integral nonlinearity. 33, 34, 39, 51, 60, 78, 89, 94, 114, 127, 158

IoT Internet of Things. xiii, 1, 4, 15, 19, 23, 24, 26, 97, 98, 151, 152, 159, 160

IoW Internet of Wearables. 10, 24, 26, 97, 151, 152

LSB least-significant bit. 33–35, 38, 39, 42, 44, 45, 60, 70, 89, 94, 102, 105, 108, 109, 114, 120, 121, 127, 161

LUT lookup table. 100

LVDS low-voltage differential signaling. 74

MCU microcontroller. 4

MEMS Micro Electro Mechanical Systems. 23

MiM Metal-insulator-Metal. 93, 108, 121

MPU microprocessor. 4, 93

MPW Multiple Project Wafer. 24

MSB most-significant bit. 31, 85, 92, 121

OA operational amplifier. 21

OTA operational transconductance amplifier. 21, 133, 139

PB prototyping board. 74

PBS phosphate-buffered saline. 143

PCB printed circuit board. 74, 113, 114, 126

PMU power management unit. 8

PoC Point of Care. 10

PPG photoplethysmography. 12, 134

PVT process-voltage-temperature. 20, 33

RBDC Radix-Based Digital Correction. 26, 84, 85, 87, 89, 91–94, 96, 152

RC resistor-capacitor. 19, 30, 31, 37, 40–42, 45, 53, 60, 66, 72, 74, 84, 93, 94, 102, 108, 120, 143, 158, 161, 162

RE Reference Electrode. xvii, 136, 142, 143, 146, 147, 149

ReDAC Relaxation Digital-to-Analog Converter. 19, 20, 26, 29, 30, 33–35, 38–45, 51–54, 57, 59–61, 65–67, 69, 70, 73–75, 77, 79, 81, 83, 84, 87, 89, 91–94, 96–98, 100, 102, 105, 108–111, 113–116, 118, 120, 121, 123, 126, 127, 129, 130, 151–153, 158–161, 163, 164

RF radio-frequency. 160

RFID Radio-Frequency Identification. 2

rms root-mean-square. 38, 39, 102, 114, 127, 146, 147, 150

ROM read-only memory. 100

RX receiver. 4

SAR Successive Approximation Register. 14, 85, 111, 123, 159

SE Single-Ended. 26, 98, 100, 102, 108–111, 113–116, 118, 120, 152, 158

SFDR Spurious-Free Dynamic Range. 77, 78, 94, 114, 116, 129

SHA Sample-and-Hold Amplifier. 98, 105, 110, 121

SINAD Signal-to-Noise and Distortion Ratio. 127, 129

SiP System in Package. 24

SMT Surface Mounted. 74

SNDR Signal-to-Noise and Distortion Ratio. 77, 94, 114, 116, 153, 158

SNR Signal-to-Noise Ratio. 77

SoC System on Chip. 24

THD Total Harmonic Distortion. 77, 94, 116, 127, 129

two-cap two-capacitor. 84, 85, 87

TX transmitter. 4

VCO voltage controlled oscillator. 39, 53–55, 58–60, 66, 84, 92

VHDL Very High Speed Integrated Circuits Hardware Description Language. 93

WE Working Electrode. 134, 136, 142, 143, 147

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