Reduction of CM Conducted Emission With a Small Dummy Leg and the Delay Compensation Technique

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***Abstract*—Passive EMI filters are usually placed at the input of power circuits to attenuate the conducted emission delivered. However, their volume may not be negligible, especially when targeting power automotive applications. The output delay compensation technique may or may not reduce the CM conducted EMI at low frequency, as a fine alignment of the output voltage phases should be achieved. This paper aims at improving the already proposed technique by exploiting a small dummy leg. In such a way, switching losses and cost of the auxiliary circuit required to implement the delay compensation technique can be reduced. From the circuit analysis, it was found that the small dummy leg can achieve a 40 dB CM EMI reduction up to 5 MHz, with one seventh the switching losses of a traditional auxiliary leg.**

***Index Terms*—ElectroMagnetic Interference (EMI), common mode conducted EMI, delay compensation technique, SiC power transistors, small dummy leg.**

I. Introduction

With the rising demand for e-mobility, power electronic circuits for automotive applications are expected to meet the strict specifications in terms of efficiency, reliability, thermal management, and weight. In this context, Silicon carbide (SiC) power transistors have been found to be a valid alternative to standard MOSFET and IGBT switches. Due to their low on-resistance and small parasitic capacitances, they result in a higher power density than IGBT and MOSFET when exploited in dc-dc converters and inverters. However, because of the low transition time of current and voltage switching waveforms, electromagnetic interference (EMI) delivered by SiC-based power circuits is expected to increase. This poses a challenge to power designers, as EMC regulations for automotive equipment are stricter than those related to commercial and industrial grade appliances.

Amongst the several EMC standards to meet, conducted emission test aims to assess the disturbances, which are conducted back onto the power lines, to be within given limits [1]. As the test setup consists of three conductors, i.e., the two power lines and the reference plane, conducted EMI are usually analyzed referring to their common-mode (CM) and differential-mode (DM) components. The former is mainly related to the parasitic capacitances between the switching nodes and the metal case, the latter to the high frequency impedance of the input capacitors.

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Mitigation techniques addressing conducted EMI can be divided into those reducing the source and those effective along the propagation path [2]. Passive EMC filters, as those proposed in [3], [4], refer to the second category. Such filters introduce further DC losses, weight, and reduce the power density of the overall design, as their volume can be up to 20 % of the overall design [5]. When targeting high power applications, the CM choke typically results to be the largest component of the filter, as its volume should be enough to avoid core saturation [6], [7].

To reduce the volume of the EMI filter, solutions based on the CM source reduction have been proposed too. Amongst them, the spread spectrum technique, in which the switching frequency is modulated according to a triangular, sinusoidal or random pattern, allows one reduce the envelope of the CM EMI spectrum. However, its effectiveness is typically limited to a 10 dB reduction of the CM spectrum [8].

The CM voltage at the neutral of a three phase electrical machine can be minimized by inserting a fourth leg complemented with an output low pass filter [9]. By modifying the sinusoidal modulation of the inverter, e.g., by exploiting an active zero SPWM, one can achieve an ideally zero neutral voltage at the switching frequency [10]. The auxiliary leg is typically made up of the same power switches exploited for the actual inverter, resulting in a quite expensive solution. Moreover, switching losses of the additional leg may not be negligible. This technique focuses on reducing the CM voltage on the electrical machine, but its effectiveness can be strongly limited by a not proper alignment between the output voltage phases [11]. Indeed, due to dead time, timing mismatch, parameter spread and different switching trajectories of the involved power transistors, a delay mismatch typically exists between the output voltage phases [12]. Such a mismatch affects the high frequency common mode current injected into the parasitic capacitances coupling the output switching nodes of Voltage Source Inverters (VSIs) with the heat sink, which is ground connected.

To address such an issue, the output delay compensation technique was investigated in several works to reduce the CM EMI [12]–[15]. By finely aligning the complementary commu-

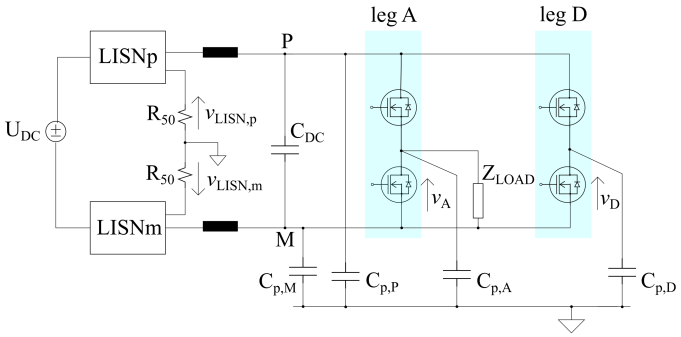

Fig. 1. Setup exploited to evaluate the conducted EMI of the A and D complementary-commutated legs.

tations of two half bridges, one can reduce the common mode current injected into the parasitic capacitances. A model to quantify the contribution of such a delay to the CM spectrum and an open loop compensation technique was proposed in [13]. However, its application is limited to inverters for BLDC motors, in which the modulation scheme is different from the space vector one typically exploited in VSIs.

In this work, the effectiveness of an auxiliary leg combined with the delay compensation technique is further investigated referring to SiC hard-switched half bridges. With respect to previous works, the adjustment of the output delay is applied to a low capacitance auxiliary leg. In such a way, the switching losses and the cost of the additional leg can be significantly reduced. The CM EMI reduction at low frequency was found to be similar to that obtained with an auxiliary leg equals to the other legs, provided that the output voltage slopes of the dummy leg are adjusted too.

The paper is organized as follows. In Sect. II, a model to predict the CM EMI of two complementary switched legs is recalled. The effects of the output voltage alignment and slope compensation are discussed in Sect. III, and in Sect. IV the effectiveness of a small auxiliary leg is assessed. Concluding remarks are reported in Sect. V.

II. CM EMI in a two complementary commutated legs

The circuit shown in Fig. 1 was considered to analyze the effectiveness of the auxiliary leg. Leg A, which represents an actual leg of a VSI, is connected to an inductive load. Leg D is the dummy one, and it is switched complementary to leg A. Two Line Impedance Stabilization Networks (LISNs) are connected between the DC supply ($U_{\rm DC}$) and the two legs under test. Parasitic capacitances amongst the equipment under test and the reference ground have been considered too. They include the capacitances which couple the output nodes of the two legs ($C_{\rm p,A}, C_{\rm p,D}$) and the nodes of the power supply rails ($C_{\rm p,P}, C_{\rm p,M}$) to the metal case. Focusing the analysis on the CM conducted EMI, the circuit shown in Fig. 1 can be simplified in the model shown in Fig. 2. Node P and node M are virtually short circuited, as the impedance of the DC link is assumed to be zero. The two LISNs have been substituted

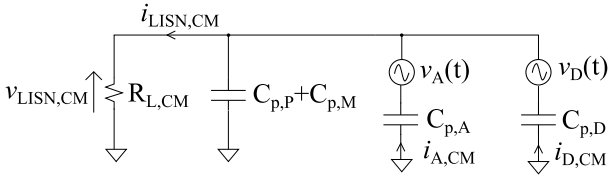

Fig. 2. Model of the circuit shown in Fig. 1 to evaluate the CM EMI of leg A and D.

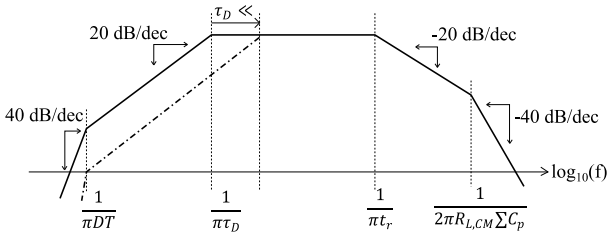

Fig. 3. Envelope of the CM EMI spectrum according to the model shown in Fig. 2 for ideally trapezoidal $v_{\rm A}, v_{\rm D}$ voltages.

with one half the receiver impedance, i.e., $R_{\rm L,CM} = 25\,\Omega$. The CM voltage is defined from the LISN output voltages $v_{\rm LISN,p}$ and $v_{\rm LISN,m}$ (see Fig. 1) as

$$v_{\rm LISN,CM}(t) = \frac{(v_{\rm LISN,p}(t) + v_{\rm LISN,m}(t))}{2} \tag{1}$$

Finally, the two legs have been modeled by two independent voltage sources equal to the output phase voltages ($v_{\rm A}, v_{\rm D}$), which drive the $C_{\rm p,A}, C_{\rm p,D}$ capacitances.

By applying the superposition of effects in the $j\omega$ domain, the contribution of $V_{\rm A}(j\omega)$ to the common mode voltage ($V_{\rm LISN,CM}(j\omega)$) can be evaluated as

$$V_{\rm LISN,CM}(j\omega)|_{V_{\rm A}} = H(j\omega)V_{\rm A}(j\omega), \tag{2}$$

where $H(j\omega)$ is the transfer function of the high pass filter, which is equal to

$$H(j\omega) = \frac{j\omega R_{\rm L,CM}C_{\rm p,A}}{1 + j\omega R_{\rm L,CM}(C_{\rm p,P} + C_{\rm p,M} + C_{\rm p,A} + C_{\rm p,D})}. \tag{3}$$

The $v_{\rm D}(t)$ voltage has period T, and it is equal to $v_{\rm A}(t)$ except for a $T/2 + \tau_D$ time delay. Thus, the overall CM voltage can be expressed as [13]

$$V_{\rm LISN,CM}(j\omega) = H(j\omega)\left(1 + e^{-j\omega(\frac{T}{2}+\tau_D)}\right)V_{\rm A}(j\omega). \tag{4}$$

For the sake of simplification, the output phase voltages have been approximated by trapezoidal waveforms. Assuming a 50% duty cycle and rise time equals to fall time (t_r), the envelope of the $V_{\rm A}(j\omega), V_{\rm D}(j\omega)$ magnitude is characterized by two poles at frequency $2/(\pi T)$ and $1/(\pi t_r)$. Although $v_{\rm A}(t), v_{\rm D}(t)$ are not actually trapezoidal, as their spectrum can be more realistically approximated by a multi slope one [16], it is worth noticing that the use of a trapezoidal approximation results in an upper bound for the CM EMI spectrum. By denoting with $\sum C_{\rm P}$ the sum of the parasitic capacitances connected to the reference ground, i.e., $C_{\rm p,P}, C_{\rm p,M}, C_{\rm p,A}, C_{\rm p,D}$, the envelope of CM voltage spectrum at the receiver side can

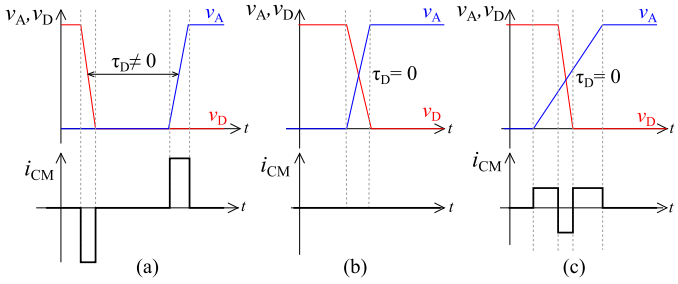

Fig. 4. Effects of (a) output voltage misalignment and (c) different slopes on the common mode current at the receiver side. With the complementary edges aligned and having the same slopes, CM EMI can be ideally zeroed (b).

be obtained from (4), as shown in Fig. 3. The delay contribution $D(j\omega) = 1 + e^{-j\omega(\frac{T}{2}+\tau_D)}$ introduces an additional breakpoint at $1/(\pi\tau_D)$. As a result, the frequency region with constant $|V_{\rm CM}(j\omega)|$ is delimited by $1/(\pi\tau_D)$ and the lowest between $1/(\pi t_R)$ and $1/(2\pi R_{\rm L,CM}\sum C_{\rm p})$. By decreasing $\tau_{\rm D}$, the related breakpoint moves to higher values in the asymptotic CM EMI spectrum, as shown by the dashed-dot line in Fig. 3. Thus, low frequency CM components can be lowered provided that a fine alignment of $v_{\rm A}(t), v_{\rm B}(t)$ transitions is achieved.

III. Delay and Slope Compensation

The analysis presented in the frequency domain is reflected in the time domain as follows. For $f << 1/(2\pi R_{\rm L,CM}\sum C_{\rm P})$, the transfer function reported in (3) can be approximated by its numerator. Thus, the CM current measured at the receiver side ($i_{\rm LISN,CM}$) is the sum of currents flowing in $C_{\rm p,A}, C_{\rm p,D}$, as shown in Fig. 2. Such a scenario is sketched in Fig. 4(a) and (b), in which the effect of the output voltage delay ($\tau_{\rm D}$) is shown. For $|\tau_{\rm D}| > 0$ (Fig. 4(a)), the negative peak of $i_{\rm CM,A}(t)$ is not aligned with that of $i_{\rm CM,D}(t)$, and these contributions do not cancel out in $i_{\rm LISN,CM}$. On the contrary, with $\tau_{\rm D} \approx 0$, the two current pulses are centered, and the resulting $i_{\rm LISN,CM}$ is approximately zero. Ideally, with $i_{\rm CM,A}(t) = -i_{\rm CM,D}(t)$, i.e.,

$$C_{\rm p,A}\frac{dv_{\rm A}(t)}{dt} = -C_{\rm p,D}\frac{dv_{\rm D}(t)}{dt}, \tag{5}$$

the CM EMI at low frequency are null. This result can be obtained provided that (5) is verified, meaning that the rise time of $v_{\rm A}(t)$ should equal the fall time of $v_{\rm D}(t)$, and vice versa. Such an assumption is not true in actual facts, and it should be taken care of when exploiting transistors with different parasitic capacitances. Indeed, the currents injected in $C_{\rm p,A}, C_{\rm p,D}$ will no longer cancel each other despite the two edges are perfectly aligned, as shown in Fig. 4(c). Recalling the circuit shown in Fig. 1, the slopes of the output voltage of leg A are briefly discussed. With a positive load current, i.e., the high side transistor is in the first quadrant when it is turned on, the rising and the falling edges of $v_{\rm A}(t)$ are triggered by the turn on and the turn off of the high side switch [17]. At the turn on of such transistor, $v_{\rm A}(t)$ raises when the low side free wheeling diode turns off, and the output capacitance of the low side transistor charges to $U_{\rm DC}$. When the high side switch exits the triode region at its turn off, $v_{\rm A}(t)$ falls, until the low side free wheeling diode turns on. The $v_{\rm A}(t)$ transitions occur when the high side switch is in the Miller's region, as its $C_{\rm GD}$ capacitance discharges through the gate resistance. By neglecting the switching loop parasitic inductance, the $v_{\rm DS}$ slopes at the turn on and at the turn off can be approximated as

$$\left.\frac{dv}{dt}\right|_{\rm ON} = \frac{V_{\rm DRV,ON} - (V_{\rm th} + \frac{I_{\rm LOAD}}{g_{\rm FS}})}{C_{\rm gd}R_{\rm G,ON}} \tag{6}$$

and

$$\left.\frac{dv}{dt}\right|_{\rm OFF} = \frac{(V_{\rm th} + \frac{I_{\rm LOAD}}{g_{\rm FS}}) - V_{\rm DRV,OFF}}{C_{\rm gd}R_{\rm G,OFF}}, \tag{7}$$

where $R_{\rm G}$ is the gate resistance, $g_{\rm FS}$ is the transistor transconductance, $V_{\rm th}$ is the threshold voltage, $I_{\rm LOAD}$ is the load current, and the transistor gate to source voltage is driven between $V_{\rm DRV,OFF}$ and $V_{\rm DRV,ON}$ [18], [19]. On the contrary, the auxiliary leg is characterized by zero load current. In this case, the rising edge of $v_{\rm D}(t)$ is triggered by the turn on of the high side transistor, and the falling edge by the turn on of the low side switch. Thus, the absolute value of the $v_{\rm D}(t)$ slopes can be derived according to (6) for both transients. As the negative and the positive slopes of $v_{\rm A}(t)$ are different (see (6) and (7)), then also those of $v_{\rm D}(t)$ should be different. To sum up, (5) can be achieved by adjusting both the output delay and the slopes of the dummy leg. As far as τ_D is concerned, it can be digitally controlled by delaying or bringing forward the input signal of gate driver of the dummy leg with respect to that of the main leg, as discussed in [13]. Regarding the slope adjustment, several techniques have been proposed in literature to control the dv/dt of SiC transistors. In [20] the use of the Miller capacitance is proposed to achieve the desired dv/dt limitation. Active Gate Drivers (AGDs) [18], [21], [22], in which the gate current/resistance/voltage is modulated during the transient to achieve a given dv/dt whilst minimizing switching losses, are also a possible way to address the slope compensation issue. Amongst the parameters which are typically under the designers' control, an effective way to modify the voltage slope consists in modifying the gate resistance [23]. By exploiting a variable resistance gate drivers, as that proposed in [24], one can modify on the fly the source and sink resistance. Indeed, by recalling (6) and (7), the voltage slew rate decreases by increasing the gate resistance. As far as the dummy leg driven by a traditional driver is concerned, the gate resistors of the high side and low side switches can be adjusted separately to achieve (5).

It should be noticed that what the analysis proposed so far assumes $v_{\rm A}(t), v_{\rm D}(t)$ to be ideal trapezoidal waveforms. However, the dv/dt during commutations of hard switched power transistor is not constant. Moreover, oscillations superimposed onto the switching voltages, which are caused by the resonance of parasitic inductances with the output capacitances of power switches, may appear [25]. For such reasons, cancellation of CM current will not be perfectly achieve, especially at high

TABLE I
PARAMETER VALUES OF THE ANALYZED CIRCUIT.

Parameter	Value	Parameter	Value
Supply voltage U_{DC}	400 V	Load current I_{LOAD}	10 A
$C_{p,P}, C_{p,M}$	44 pF	$C_{p,A}, C_{p,D}$	19.5 pF
PCB stray inductance	16.4 nH	Gate resistance	7 Ω
Leg A switches	[26]	Small leg D switches	[27]
C_{OSS}, leg A	200 pF	C_{OSS}, leg D, small	26 pF

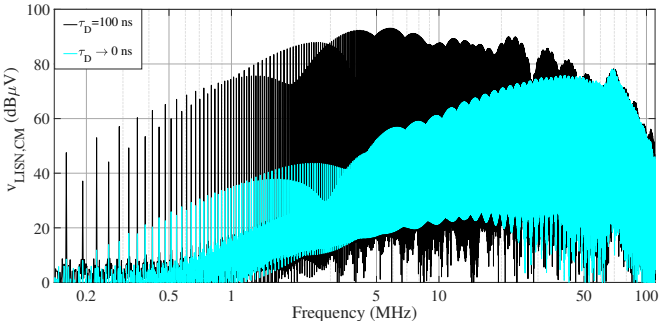

Fig. 5. Frequency spectra of CM EMI with the auxiliary leg made up of the same transistors of the actual leg. With a proper alignment of the output voltages ($\tau_{\mathrm{D}} \rightarrow 0$), LF components are strongly reduced.

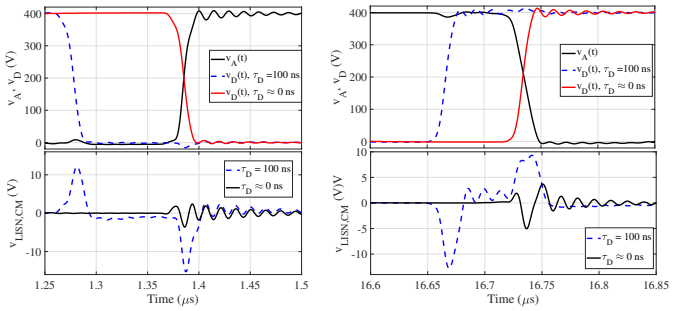

Fig. 6. Time domain waveforms obtained with the auxiliary comprised of the same transistors of the actual leg. Phase voltages are on the top, CM voltage at the LISN on the bottom for the two transitions.

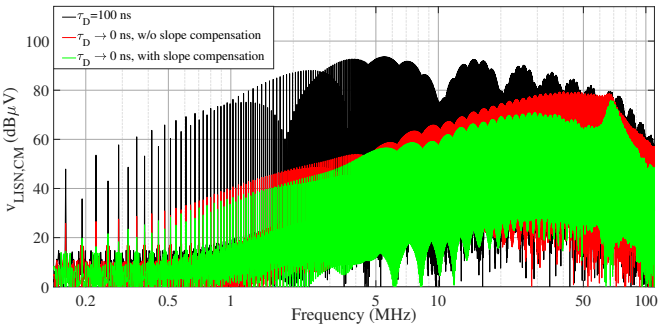

Fig. 7. Frequency spectra of CM EMI with the auxiliary leg made up of the small transistors. Both a proper alignment of the output voltages ($\tau_{\mathrm{D}} \rightarrow 0$) and slope compensation are required to minimize LF components.

frequency. Thus, the proposed technique is expected to be mainly effective at low frequency.

IV. CIRCUIT ANALYSIS

In order to assess whether a small dummy leg can reduce the CM EMI, the circuit shown in Fig. 1 was analyzed with the parameters reported in Table I. As the supply voltage is 400 V, HV LISN should be exploited, thus the corresponding model discussed in [28] has been included in the setup. Parasitic capacitances causing the CM EMI have been estimated from the area of nodes coupled to the ground-connected heat sink through a thermal gap pad (ε_{r}=2.3 and 0.225 mm thick). Regarding the parasitic inductances included in the power switching loop, the contribution of PCB traces has been obtained from a 3D FEM simulation. A 220 μF film capacitor has been selected as DC link, and the legs are commutated at 32 kHz with a 50 % duty cycle. The parameter values and the selected SiC transistors are reported in Table I. It should be noticed that switches exploited for the small dummy leg are characterized by an output capacitance (C_{OSS}) which is approximately one seventh of that of leg A.

A. Dummy leg equal to leg A

Prior to introduce the small dummy leg D, simulations have been carried out with leg A and D comprised of the same transistors. By regulating the driving signals of power transistor such that τ_{D}=100 ns, the corresponding CM EMI are shown in Fig. 5. It is worth noticing that the envelope is in agreement with that of the model (see Fig. 3). Poles and zeros can be evaluated as $1/\pi DT$ = 20 kHz, $1/\pi\tau_{\mathrm{D}}$ = 3 MHz, $1/\pi t_r$ = 18 MHz, and $1/2\pi R_{\mathrm{L,CM}} \sum C_{\mathrm{p}}$ = 44 MHz. Time domain waveforms are shown in Fig. 6 for the two phase voltages (top) and $v_{\mathrm{LISN,CM}}$ (bottom) in dashed lines. The waveforms at rising edge of v_{A} are on the left, those at the falling edge on the right. With τ_{D}=100 ns, the common mode voltage is not null close to each phase transition, as shown in Fig. 4(a). Moreover, oscillations at 70 MHz are superimposed onto the switching waveforms. These oscillations are reflected on the CM EMI too, as it is shown from the peak at the oscillation frequency in the CM frequency spectrum. On the contrary, with $\tau_{\mathrm{D}} \approx 0$ ns, the low frequency components of the CM spectrum are reduced by 40 dB, in agreement with the dot dashed line in Fig. 3. In such a case, $v_{\mathrm{LISN,CM}}(t)$ is reported in Fig. 6 by solid lines, and it is non null only close to $v_{\mathrm{A}}, v_{\mathrm{D}}$ transitions. It should be noticed that the CM voltage is not exactly zero, as predicted in Fig. 4(b), because of the different slopes between leg A and leg D. Oscillations do not cancel out each other, and the HF components of the spectrum are not zeroed. As a result, with $\tau_D \rightarrow 0$ low frequency CM EMI are effectively reduced by applying the proposed technique, and high frequency ones are marginally affected.

B. Small dummy leg

The delay compensation technique was then asserted in case of a small dummy leg. With voltage transitions misaligned by τ_{D}=100 ns, the CM EMI spectrum, which is shown in Fig. 7, is in agreement with that of the model, as discussed in Sect. II. As in Fig. 6, the CM voltage in the time domain

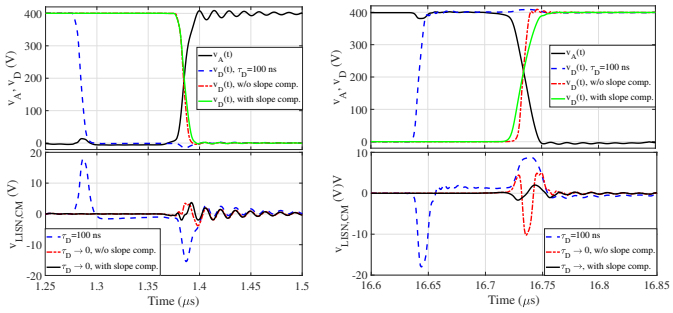

Fig. 8. Time domain waveforms obtained with the auxiliary comprised of the small transistors. Phase voltages are on the top, CM voltage at the LISN on the bottom for the two transitions (left and right sides).

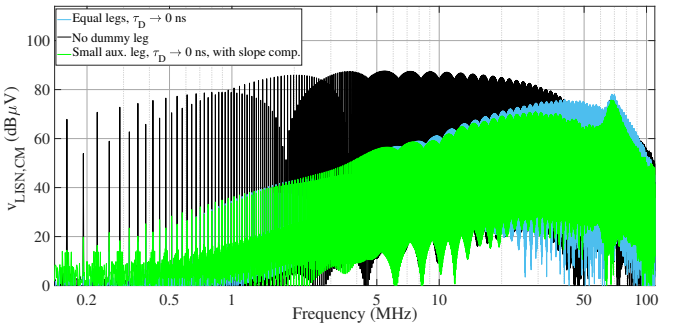

Fig. 9. Comparison between CM EMI spectra for no auxiliary leg, auxiliary leg equal to the actual one and small dummy leg. The latter two spectra are characterized by the same envelope at LF.

is characterized by two peaks in correspondence of $v_{\mathrm{A}}, v_{\mathrm{D}}$ edges, as shown in Fig. 8 by dashed lines. By modifying the timing of the SiC driving signals, output voltage alignment is achieved, resulting in the in-between spectrum shown in Fig. 7. As it can be noticed by the waveforms shown in Fig. 8 by dashed dot lines, the CM voltage is reduced, but it is not completely canceled. Besides the contribution of oscillation, one can notice from the right plots in Fig. 8 that the v_{A} fall time (23 ns) is much higher than the v_{D} rise time (9 ns). Therefore, (5) can not be achieved. By modifying the gate resistances up to 40 and 130 Ω for the low side and high side transistors of leg D, waveforms shown in Fig. 8 by solid lines can be obtained. With such a slope compensation, CM EMI can be further reduced, as shown in Fig. 7 by the lowest spectrum.

C. Comparison

The use of the auxiliary leg, either small or made of the same transistors of the leg A, was then compared with the case of no auxiliary leg exploited. Figure 9 reports the CM spectra for no dummy leg and for the two dummy legs with the output delay compensated. It is worth noticing that with the dummy leg, either small or big, CM conducted EMI are effectively reduced by more than 40 dB at 1 MHz. At low frequency the small auxiliary leg with slope compensation results in the same CM attenuation that of a big dummy leg. For frequencies higher than 30 MHz, the slope compensation is effective in reducing the CM spectrum further, as a better CM current cancellation can be achieved. However, frequency components at 70 MHz, which are related to the ringing superimposed onto the switching waveforms, are not affected by the proposed technique. Table II compares the three cases in terms of CM EMI at different frequencies, efficiency, and power dissipation of the auxiliary leg. The efficiency of the system is marginally affected by the use of the dummy leg, as the power dissipated in the dummy leg is much smaller than that provided to the load. To sum up, a small dummy leg can achieve the same CM reduction, but with one seventh of the power dissipation with respect to an auxiliary leg equals to the VSI legs.

TABLE II
COMPARISON BETWEEN SOLUTIONS

Parameter	No aux leg	Aux leg big	Aux leg small
CM EMI @ 160 kHz	67.8 dBμV	11.8 dBμV	14.4 dBμV
CM EMI @ 1 MHz	80.6 dBμV	35.5 dBμV	36.3 dBμV
CM EMI @ 10 MHz	87.1 dBμV	60.6 dBμV	59.1 dBμV
CM EMI @ 40 MHz	75 dBμV	75 dBμV	68.2 dBμV
Efficiency	97.8 %	97.67 %	97.8 %
Aux leg power dissipation	-	1.52 W	0.22 W

V. CONCLUSION

This paper proposed the use of a small dummy leg to reduce the LF CM EMI delivered by power switching circuits. By finely aligning the commutations of the auxiliary leg with those of the actual one, the HF current injected into the parasitic capacitances can be canceled out. Power switching losses and cost can be reduced by exploiting transistors with small capacitances, provided that gate resistances are adjusted to obtain the same slopes of the actual leg. The analysis carried out on a single main leg resulted in a 40 dB CM EMI reduction for frequencies lower than 5 MHz when a small dummy leg is exploited. Such a dummy leg can be applied to circuits with an odd number of half bridges, e.g., three phases VSIs, so that the CM injected current can be minimized at each transition of the main legs.

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