Simulation Analysis of the Bit Error Induced by EMI on Galvanically Isolated Data-Link Embedded in an Automotive Battery Management IC

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***Abstract*— In this paper, the susceptibility to electromagnetic interference (EMI) of a battery management system (BMS) used in electric vehicles is addressed. In particular, the effects of EMI on the BMS vertical interface (VIF), i.e., the galvanically isolated data link between different BMS modules are analyzed by transistor-level simulations with reference to direct power injection (DPI) and bulk current injection (BCI) test conditions for the first time. Based on the simulations, the DPI and BCI susceptibility levels of two different VIF architectures are estimated, and different failure mechanisms are highlighted.**

Keywords*— *Electric Vehicle (EV), Battery Management System (BMS), Vertical Interface (VIF), Electromagnetic Compatibility (EMC), Transistor-level simulation, Integrated Circuit EMC, Electromagnetic Interference (EMI), Direct Power Injection (DPI), Bulk Current Injection (BCI)

I. INTRODUCTION

Battery packs based on Lithium-ion (Li-ion) and Lithium-Polymer (LiPo) electrochemical technologies have become the go-to option for Electric Vehicles (EVs) and Hybrid Electric Vehicles (HEVs) due to their high energy density and power capabilities [1]. However, these batteries can be permanently damaged and can lead to life-threatening hazards such as fires and explosions if they are over-discharged, overcharged, or operated at excessive temperatures [2]. Thus, the development of an electronic battery management system (BMS) that can detect and respond to these critical conditions is necessary for the safe operation of these vehicles.

A typical BMS, depicted in Fig. 1, consists of several front-end modules that acquire crucial information like cell voltages and temperatures, as well as a digital control unit that runs specific management algorithms. The front-end integrated circuits (ICs) in the BMS must operate accurately and reliably in a harsh electromagnetic environment, where radiated and conducted interference is generated by the electric powertrain, on-vehicle electronics, and other information and communication equipment.

Electromagnetic Interference (EMI)-induced failures in the BMS are a major safety threat and have been addressed in recent EMC literature [3]-[5] at system level with reference to standard DPI and BCI tests [6]. These studies suggest that most critical EMI susceptibility issues are related to the vertical interface (VIF), i.e. the galvanically isolated data link

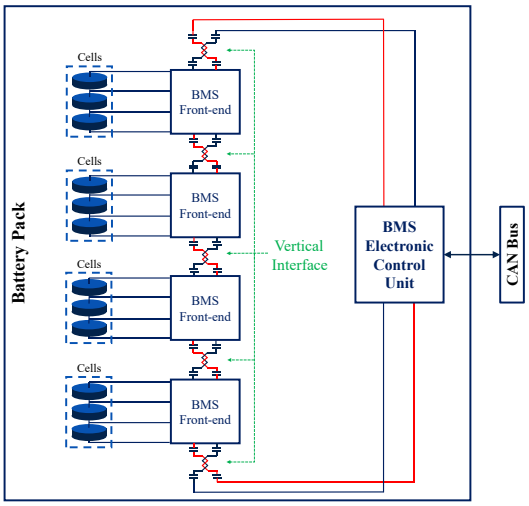

Fig. 1. A typical battery management system (BMS) structure.

which is responsible for the communication and exchange of information between different BMS front-end ICs and between BMS front-end ICs and the master BMS Electronic Control Unit (ECU), which coordinates the operation of the BMS modules, estimates the battery's state of charge, state of health, and other critical parameters, and interacts with on-vehicle electronics.

While the BMS susceptibility to EMI has been investigated so far at system level [3]-[5], in this work the susceptibility to EMI of the most critical VIF block is tackled by transistor level simulations aiming to highlight the main failure mechanisms and to provide IC designers more insight and a practical simulation framework to design VIFs which are intrinsically immune to EMI for next-generation BMS ICs. For this purpose, two different VIF structures are investigated using direct power injection (DPI) and bulk current injection (BCI) simulations. The susceptibility levels of the two VIFs are estimated, and different EMI-induced failure mechanisms are highlighted. This work is considered as a preliminary work and oriented to support the VIF IC design in the near future.

The rest of the paper is organized as follows: in Section II, the vertical interface structure is presented. In Section III the BCI and DPI simulation setup is introduced and the simulated DPI and BCI susceptibility levels of two VIF architectures are presented. Section IV is devoted to the discussion of failure

mechanisms, benchmark parameters, and related results. Finally, in Section V, some conclusions are drawn.

II. The Vertical Interface

This paper examines the immunity of a BMS used in electric vehicles to electromagnetic interference (EMI) by analyzing the susceptibility of the galvanically isolated VIF introduced to exchange data between different BMS modules. In this section, the working principle of the VIF and two different VIF ICs are presented.

A. VIF Structure and Operation

The VIF implements a differential, capacitively isolated, bi-directional communication at 4Mbit/s based on a proprietary protocol, which is illustrated in Fig. 2. In detail, a positive 62.5ns-long differential pulse followed by a negative one encodes a logic "1", while a negative differential pulse followed by a positive one encodes a logic "0". A 125ns idle time between each transmitted bit is required to ensure proper reception by the receiver. The BMS VIF transceivers considered in this paper are comprised of a transmitter, a receiver, an ESD protection circuit, and a digital block that converts the transmitted signal into digital bits. Inside the receiver, there are comparators acting as the first part to generate transmitted bits, a transmission resistor connecting the ISOP and ISOM nodes during the receiving mode, and a common-mode voltage generator.

In this work, a first VIF IC (VIF#1 in the following) and a newer design (VIF#2) are considered and compared. Fig. 3 depicts the schematic view of VIF#1 and VIF#2. Some important differences between two structures are as follows:

- A different comparator circuit with higher common-mode input range is adopted in the receiver of VIF#2.
- The comparator's threshold voltages are different for VIF structures: V_{th} is about 250mV and 50mV for VIF#1 and VIF#2, respectively.
- Different overvoltage-overcurrent protections are adopted.
- Different input electrostatic discharge (ESD) structures are considered.

III. DPI and BCI Simulations

To evaluate the susceptibility to EMI of the VIF structures, VIF#1 and VIF#2 are simulated in similar conditions. For this purpose, two identical VIF modules, one operating as a transmitter and the other as a receiver, are connected by a differential communication line (twisted pair), which is capacitively coupled to each transceiver by two 2.2nF capacitors. The transmitter generates a signal that passes through the communication lines and is applied to the input of two comparators in the receiver. Here, the two comparators

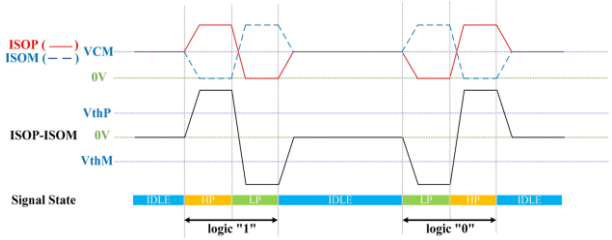

Fig. 2. Waveform of the data bits in vertical interface communication.

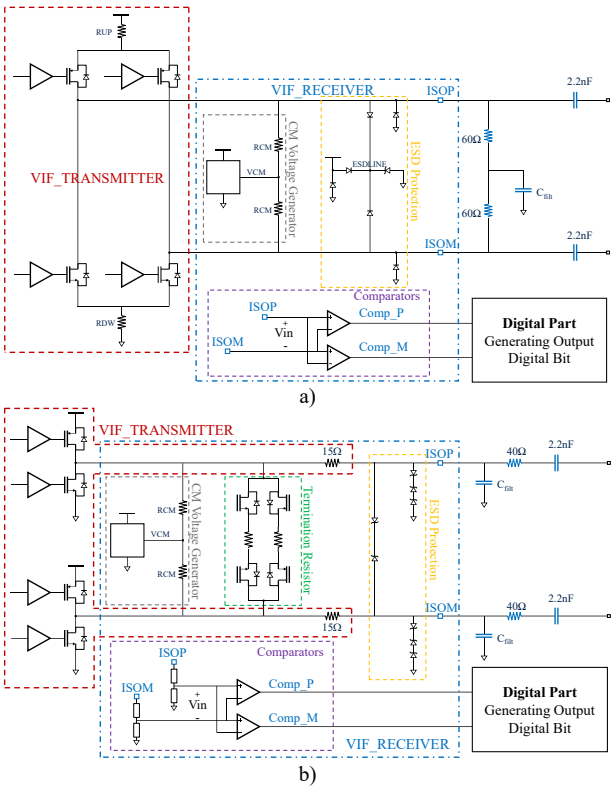

Fig. 3. Schematic view of a) VIF#1 and b) VIF#2.

start toggling when the input differential signal crosses their threshold voltages, which are equal in magnitude and with opposite sign as shown in Fig.2. Fig. 4 shows the input signal of the comparators before and after RF signal injection and the injected RF signal in time domain. Positive and negative threshold voltages are indicated as V_{thP} and V_{thM} respectively. The output of the comparators is processed with a digital block to extract the received binary data.

A. DPI Simulation Procedure

The susceptibility of the VIF module is estimated by DPI transistor-level transient simulations, introducing a lumped element model of the DPI injection network prescribed by the IEC 623132-4 standard [6], as shown in Fig. 5a. A 1µs simulation time from the application of RF power is

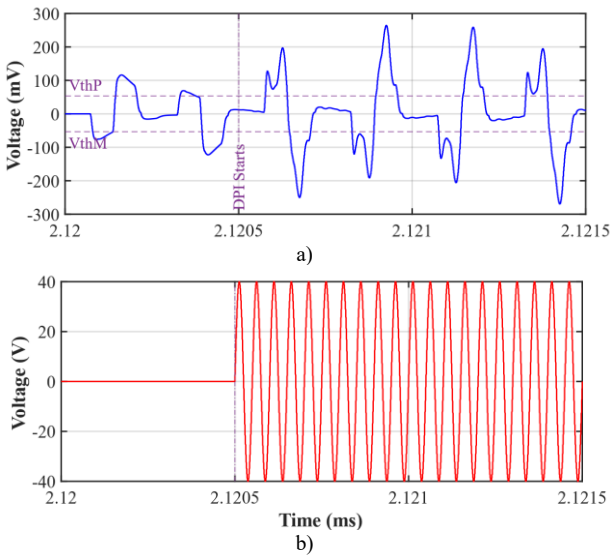

Fig. 4. Time domain waveform for a) Differential comparators' input signal and b) RF source

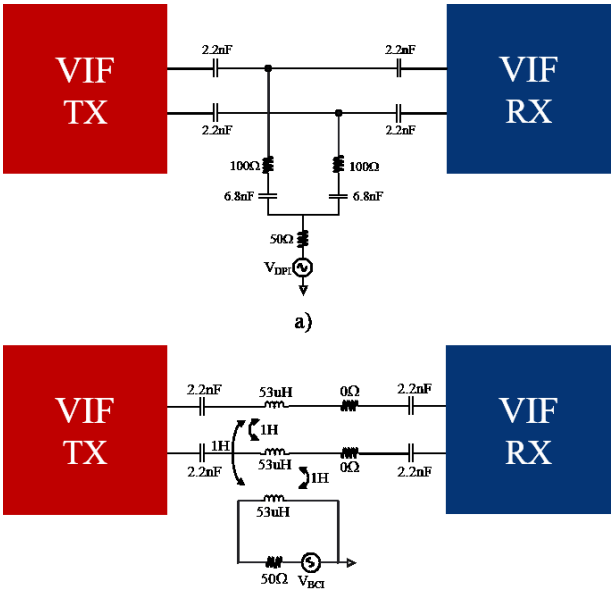

Fig. 5. Simulation test bench for a) DPI and b) BCI.

considered to have at least one complete period of the injected RF signal, even at the lowest EMI frequency. At each frequency, the test has been repeated for different phases of the RF disturbance, and the worst phase condition is considered in the assessment of the immunity level.

For each frequency ranging from 1MHz to 1GHz, DPI simulations are performed by increasing with 1.5dB-steps the injected RF incident power P_{DPI}, related to the peak amplitude V_{DPI} of the sine wave voltage source as:

$$V_{DPI} = \sqrt{8 \cdot 50\Omega \cdot P_{DPI}} \quad (1)$$

until the maximum test level (36 dBm) is reached or a failure (i.e., a mismatch between the digital bit generated at the transmitter's input and the receiver's output) is observed. In this case, the minimum level of RF incident power that leads to the failure is recorded as the DPI immunity level for the specific simulation frequency.

B. BCI Simulation Procedure

The immunity level of the VIF structure is also tested by transistor-level transient simulations reproducing BCI immunity tests performed in compliance with ISO 11452-4 (substitution method) [7]. The lumped-element BCI injection circuit is depicted in Fig. 5b, in which the V_{BCI} RF voltage corresponding to the injected bulk current has been estimated on the basis of the calibration procedure described in ISO 11452-4 for the substitution method [7] as:

$$V_{BCI} = 3 \cdot 50\Omega \,.\, I_{BCI} \quad (2)$$

The frequency range for this simulation is limited to 1MHz-400MHz, based on the standard. This simulation setup does not account for the propagation effects in the wiring harness, which represents a worst-case scenario [8].

C. DPI and BCI Simulation Results

The susceptibility level of the two VIF modules extracted from DPI and BCI simulations is depicted in Fig. 6. A clear correlation between the DPI and BCI simulation results can be observed. It can be also observed that both the VIF architectures are more susceptible to low frequency EMI,

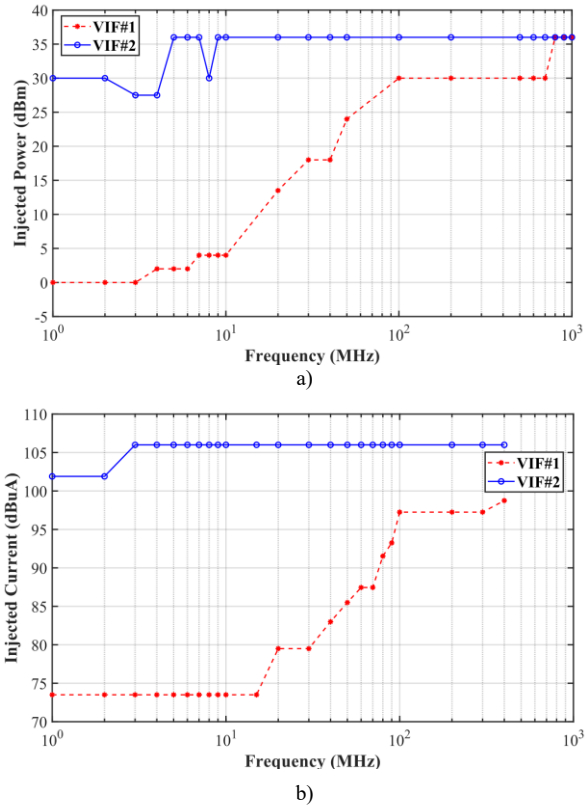

Fig. 6. Susceptibility level to EMI for VIF#1 and VIF#2 acquired from a) DPI simulations and b) BCI simulations.

where for VIF#1 the DPI (BCI) failure level is as low as 0dBm (73.5dBµA) below typical automotive requirements, while for VIF#2 the DPI (BCI) failure level reaches 27.5dBm (101.9dBµA).

IV. Investigation Of Failure Mechanisms And Results

To gain more insight into the failure mechanisms observed in the previous simulations and to discuss how close the VIF is to the failure condition even when no failure is observed, several benchmark parameters are defined in this section. Since a good correlation between BCI and DPI results has been observed in the previous Section, this investigation has been performed with reference to DPI tests only.

A. Benchmark Parameters

In order to discuss the signal integrity at the receiver, several parameters are extracted from the input differential signal of the comparators. The reason is that the comparators are the first step for regenerating the transmitted digital bits and the signal integrity at the input of the comparators is therefore critical. Three signal integrity benchmark parameters are introduced and depicted in Fig. 7 on a simulated input differential signal of the comparators. The parameters' description is as follows:

- **ΔInt** is the mean value of comparator input differential signal exceeding the threshold voltages, as highlighted in Fig.7a and is defined as:

$$\Delta Int = \frac{\int_{TF}^{TL} |v_{in} - V_{th}| \, dt}{|TL - TF|} \quad (3)$$

where v_{in} is the input differential signal of the comparators, V_{th} is the positive threshold V_{thP}

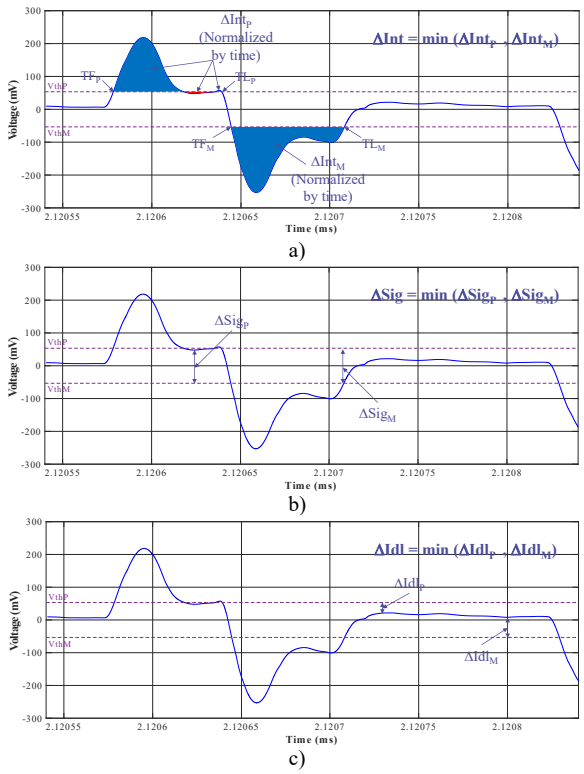

Fig. 7. A simulated input differential signal of the comparators visualizing a) ΔInt b) ΔSig c) ΔIdl.

(negative threshold V_{thM}) for high (low) differential pulses, and TF, TL are the first and last threshold crossing of the signal in each pulse. A large ΔInt ensures that the comparator is well driven above the threshold for a sufficient time to be properly triggered at each signal pulse.

- **ΔSig** refers to the distance between V_{thP} (V_{thM}) and the maximum (minimum) of the signal during a low (high) pulse, which indicates the margin towards the opposite threshold crossing (i.e. V_{thP} at the low state and V_{thM} at the high state).
- **ΔIdl** is the minimum distance between the signal and the thresholds (V_{thM}, and V_{thP}) during the idle time (see Fig. 2) and it is introduced to monitor the behavior of the differential signal during the idle time, in which the signal level should remain between the positive and negative threshold voltages to avoid spurious commutations.

The signal integrity parameters introduced above should be positive, and the closer they are to zero, the closer the transmission is to a failure condition. For ΔInt in particular, it can be said that if ΔInt is very close to zero (below 5mV) the transmission is very close to a failure, but if it is higher than this range, it is far enough from the failure condition and it doesn't matter how high it is.

Evaluating and monitoring such parameters during DPI tests makes it possible to discuss whether EMI failures are simply related to the digital signal integrity at the receiver, or if different failure mechanisms, e.g., related to EMI-induced malfunctions in analog and digital front-end circuitry, whose susceptibility to EMI was reported in previous work [10-14], are excited.

B. *Phase Shifting Effect on DPI Simulation Results*

To get more insight into failure mechanisms, the results of DPI simulations performed on both the VIF transceivers (VIF#1 and VIF#2) at the highest injection power (36dBm, i.e., 40V sine wave peak amplitude) are reported. Fig. 8 shows two examples of how different initial phases can change the differential signal in time domain for a low (5MHz) and a high (40MHz) frequency.

Fig. 9 highlights how phase shifting affects the results. The signal integrity benchmark parameters defined in Section IV (a) are calculated. It is observed that the value of parameters in lower frequency strongly depends on the initial phase while the RF signal frequency increases (above 30MHz) the results are no longer dependent on the initial phase.

C. *Failure Mechanisms*

Fig. 10 shows the benchmark parameters for VIF#2 across the bandwidth calculated at the highest injection power. All introduced benchmark parameters, are calculated with respect to the worst-case phase relation between the RF disturbance and the transmission clock.

Fig.10a shows that EMI-induced failures in VIF#2 can be observed at low frequency, which is consistent to what observed in Fig.6. For the same frequencies, it can be observed that the signal integrity parameters introduced in Section IV (a), which are reported in Fig.10b-d, are either negative or closer to zero, confirming a strong correlation between the differential signal integrity and the observed DPI failures.

Similar calculations and plots are reported for the VIF#1 architecture in Fig. 11. The pass/fail plot in Fig.11a shows that

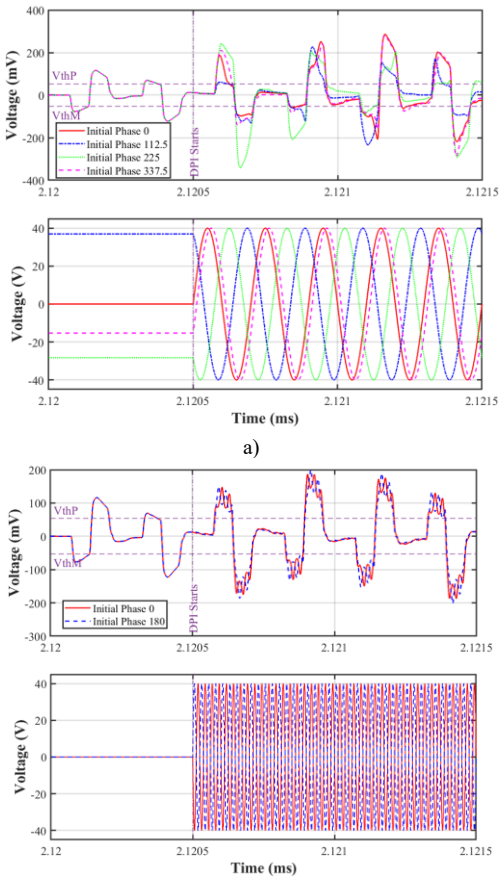

Fig. 8. Time domain waveforms showing RF signal and input differential signal with different phases at a) 5MHz and b) 40MHz.

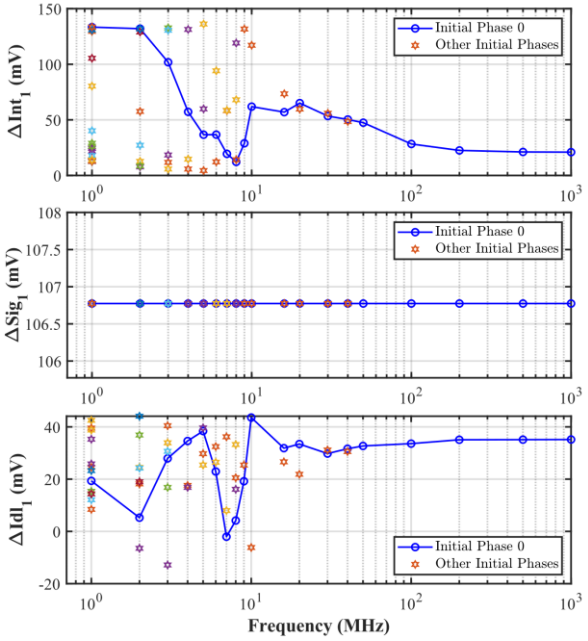

Fig. 9. Pass or fail report and benchmark parameters calculation for VIF#2 at 36dBm direct injected power

VIF#1 structure is very susceptible to EMI at the highest power injection level and only performed correctly at 800MHz-1GHz bandwidth. Also in this case, failures are well correlated to values of the signal integrity parameters in Fig.11b-d which are negative or approaching zero.

Based on these simulations, the correlation between differential mode signal integrity and failures suggests that the operation of these circuits is mainly impaired by the differential mode component of the received signal at the input of the comparators, that is corrupted by EMI due to the conversion of common mode into differential mode interference [9]. This CM to DM conversion can be due to imbalances in the structure and/or rectification phenomena in the ESD protections.

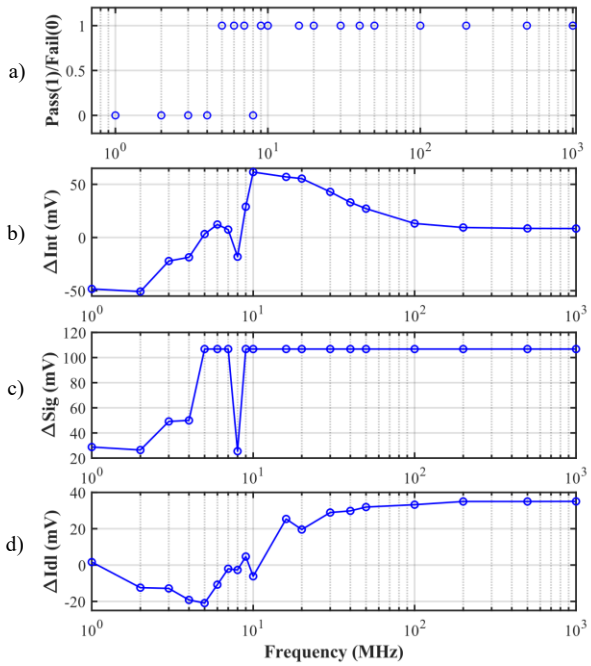

Fig. 10. Pass or fail report and benchmark parameters calculation for VIF#2 at 36dBm direct injected power

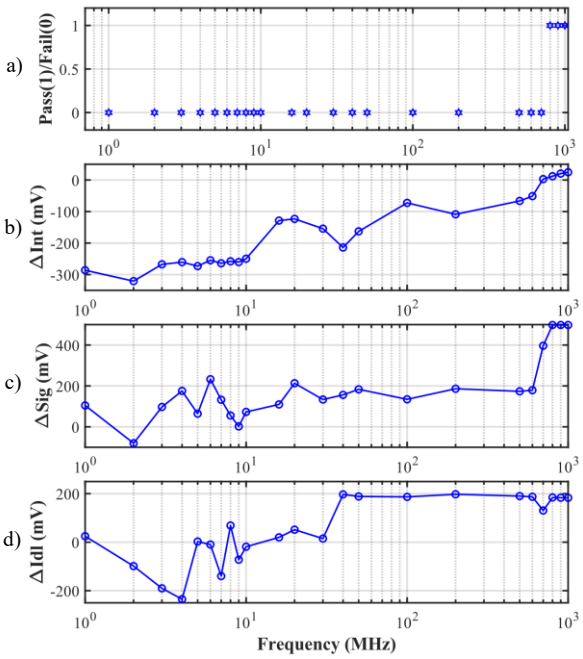

Fig. 11. Pass or fail report and benchmark parameters calculation for VIF#1 at 36dBm direct injected power

It should be noted that whenever the parameters are passed, comparators operate in a way that the output digital bit is correctly generated and future research on the VIF immunity can be focused on the mechanisms leading to the conversion of common-mode into differential-mode interference in the VIF transceivers.

V. Conclusion

This paper presents an assessment of the susceptibility to EMI of the VIF isolated communication module used in BMS for electric vehicles. Two different VIF structures, VIF#1 and VIF#2, are proposed and simulated using direct power injection (DPI) and bulk current injection (BCI) techniques. The specific susceptibility levels of the VIF are highlighted, and the EMI-induced failure mechanisms are investigated by introducing signal integrity benchmark parameters to discuss the quality of the received signal. Simulation results, which will be validated by comparison with DPI/BCI experiments in the near future, show that VIF#2 outperforms VIF#1 in terms of EMI robustness, and that EMI-induced failures can be mainly correlated to the integrity of the differential input signal at the receiver. The study provides insights that can be used to support the VIF IC design, suggesting that the conversion of common mode to differential mode interference is the most critical effect that needs to be addressed to achieve immunity.

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