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Design of a 1st-order Continuous-Time $\Sigma\Delta$ modulator with a Digital-Based Floating-Inverter Integrator

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Abstract. This paper proposes the design and simulation of an ultra-low-power (ULP) digital-based 1st-order continuous-time Sigma-Delta (CT-$\sum\Delta$) modulator for Internet of Things (IoT) applications. Simulation results in a 180-nm standard CMOS technology, demonstrating that the overall modulator consumes only 47 nW, which is considerably low compared to the state-of-the-art. The CT-$\sum\Delta$ modulator, operating at a supply voltage of 0.4 V and at a 500Hz bandwidth, achieves a spurious-free dynamic range (SFDR) of 54 dB and a signal-to-noise-and-distortion ratio (SNDR) of 47.41 dB, corresponding to an effective number of bits (ENOB) of 7.6 bits and to a Schreier Figure-of-Merit (FOMS) of 147.678-dB. To the best of the author's knowledge, the overall results do not showcase a significant improvement in the field of CT-$\sum\Delta$. Nonetheless, it is crucial to emphasize that we are at the forefront of pioneering a new approach, and these results stand as the current best achievements.

Keywords: IoT, analog and mixed-signal circuits, Digital-based (DB) CT-$\sum\Delta$ Analog-to-digital converters (ADCs).

1 Introduction

This paper addresses the challenges in analog and mixed-signal integrated circuit (IC) design posed by energy and scaling constraints in the context of IoT applications. To meet the demands of IoT applications in terms of size and power efficiency, new amplifier topologies have been proposed so far [1-5]: in particular, floating-inverter amplifiers (FIA), in which a CMOS inverter is powered by a floating reservoir capacitor have been introduced in [4], and fully digital-based Operational-Transconductance-Amplifier (DB-OTA) based on digital standard cells have been demonstrated to achieve nanowatt-range power in sub-kHz applications [3].

In this paper, the FIA concept is exploited to further enhance the energy efficiency of a DB-OTA and a floating-inverter digital-based Operational Transconductance Amplifier (FI-DBOTA) is introduced to design a digital-based continuous-time 1st-order Sigma-Delta modulator (DB-CT-$\sum\Delta$) for IoT applications.

2 First- order continuous-time Sigma-Delta modulator (CT-$\sum\Delta$) and FI-DB-OTA

The architecture of the proposed 1st-order DB-CT-$\sum\Delta$ is illustrated in Fig. 1. The main blocks of the circuit are a four-input DB-FIA (depicted as INV block powered by CMC's output), in which two inputs are connected to the external differential input terminals and two inputs provide a negative feedback path to the output, a pair of RC low-pass filters, an inverter chain block, which contains three inverters, a common-mode compensation (CMC) block as in a DB-OTA, and an output stage including a D-flip flop.

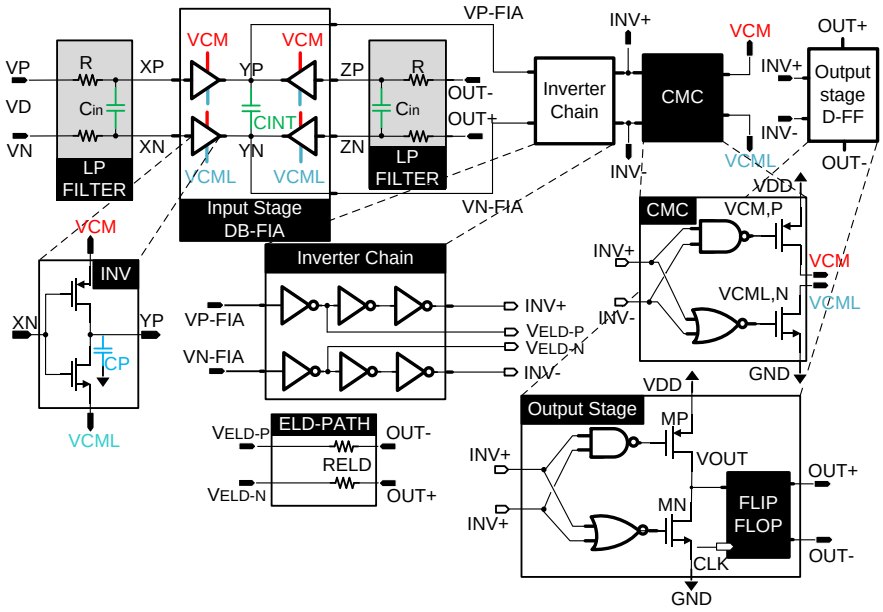


Fig. 1. Schematic of 1st-Order CT-$\sum\Delta$, FI-DBOTA Inverter chain and additional feedback path to output, CMC circuit, Output stage, D-FF.

Similar to other digital-based operational-transconductance-amplifiers (DB-OTAs) [2-3, 7-8], VD (VD=VP-VN) is dynamically amplified. More specifically, the source of the PMOS (NMOS) devices of the input FIA are alternatively connected to the supply node (ground node) to dynamically bias the floating inverter stage. The primary idea is to digitally amplify analog input signal by rejecting the common-mode (CM) component of the input voltage. Then, the amplified signal is digitized through inverter chain (made up by three inverters) to yield a fully digital control signal (INV+, INV-) to the CMC and to the output stages. According to the digital finite-state machine (FSM) whose state-transition graph of the DB-FIOTA is illustrated in Fig. 2(a), the system evolves through four states corresponding to (INV+, INV-) = (0,0), (1,1), (1,0), (0,1). It is worth noting that FSM continuously oscillates through states (0,0), (1,1) effectively compensating the CM voltage. Then, in the transition from (0,0) to (1,1) and

vice versa, the system transitions through states (0,1) or (1,0) according to the sign of the input differential voltage (whenever VD ≠ 0) and in these two states the output stage is driven to charge (state (1,0)) or discharge (state (0,1)) the output node accordingly. In CMC state (0,0), (1,1) (refer to Fig. 2 (b, e)), both transistors in the output stage are off and the VOUT node is kept in high impedance and the output capacitance voltage remains constant. In particular, in discharge (0,0) (charge (1,1)) mode, the NOR (NAND) gate connects VCML (VCM) node to ground (VDD) terminal. More specifically, this mechanism provides a dynamic biasing to the DB-FIA. In states (0,1) and (1,0) VCM (VCML) are isolated from the power supply and ground until the subsequent (1,1) or (0,0) state, so that the inverters in the DB-FIA stage are floating and are progressively operated in the near- and sub-threshold regions, thus providing an extremely energy efficient amplification as in [4] (refer to Fig. 2 (f)).

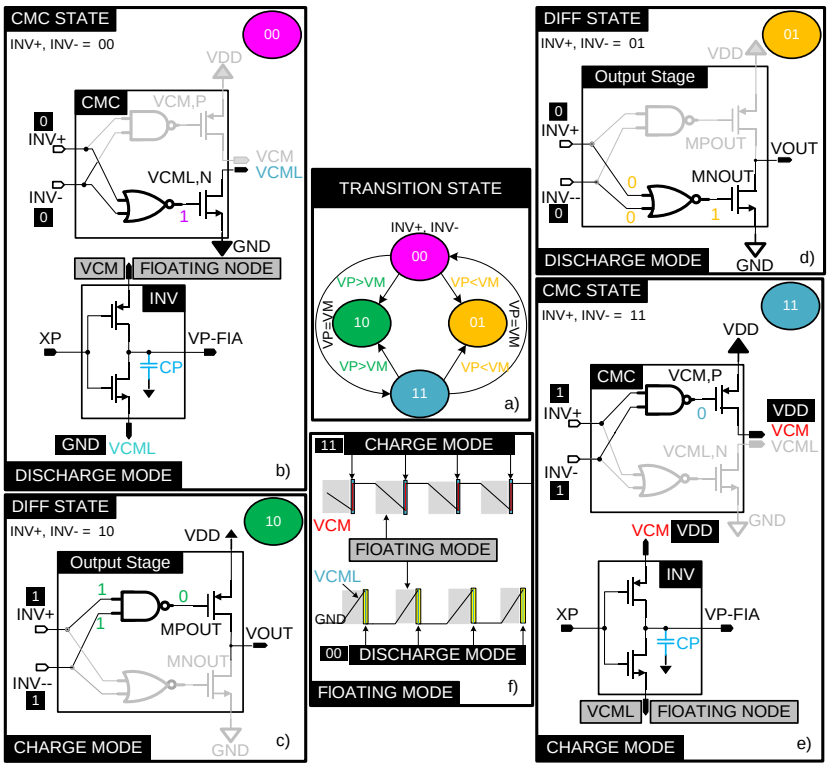


Fig. 2. State transition diagram, schematic of CMC and output stage in four states.

An important observation is that devised architecture has superiority over same topologies in terms of power efficiency for some reasons that explained as follows. First, variable VGS in FIA lead INV's transistors to work in near- and sub-threshold region (VGS<Vth), thereby yielding very high transconductance efficiency g_m/I_D. Second, floating-mode architecture is designed to simultaneously avoid any direct static path

from supply voltage to ground (as depicted in Fig. 2 (f)). According to Fig. 2 (c, d), when (INV+, INV-) = (1,0) and ((0,1)), VP-FIA is above (below) and VN-FIA is below (above) the inverter chain trip point, a positive (negative) input differential voltage is detected and the it follows that the differential input voltage which is belong to VD>0 (VD<0) and the output stage is activated accordingly. That is, the NAND (NOR) gate output is applied to the MPOUT (MNOUT) transistor to increase (charge) or decrease (discharge) the output node.

The operation of the INV and CMC blocks within the FI-DBOTA is better illustrated in Fig. 3. According to the schematic (Fig.3 (a)), the internal waveforms associated with the CMC's output voltage (VCM, VCML) are depicted in Fig. 3(b).

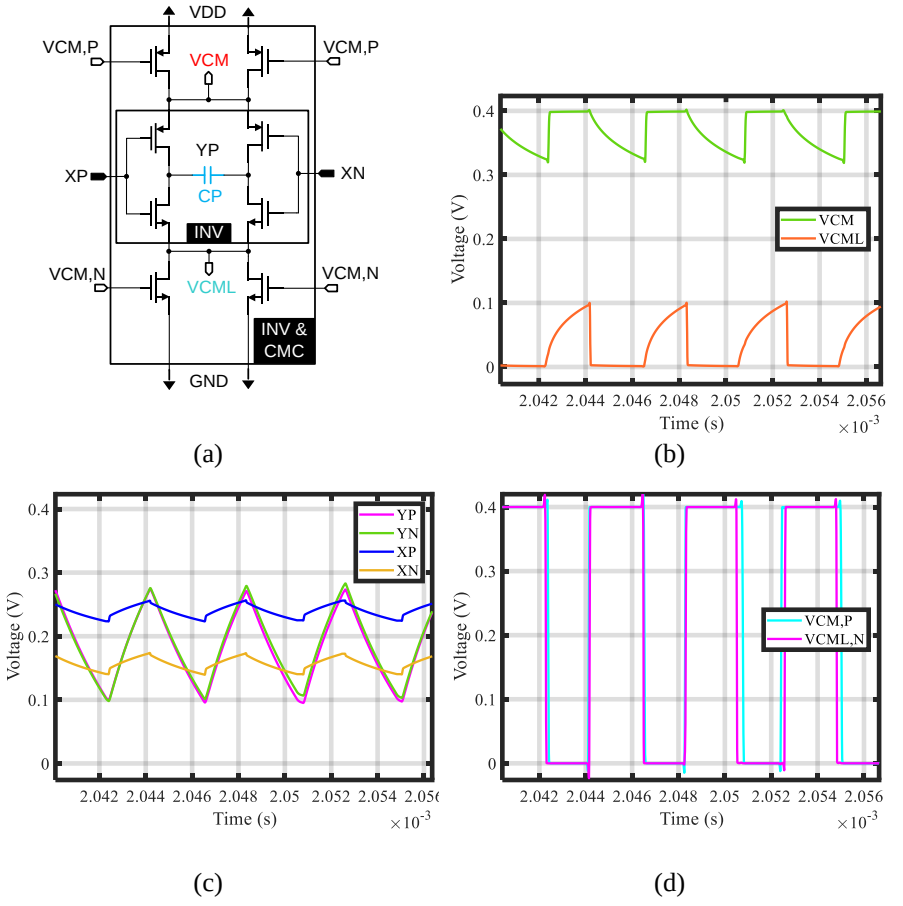


Fig. 3. a) INV and CMC schematic, b) waveform of CMC block (VCM, VCML), c) input of FIA and summing node of four FIA, d) digital gate-controlled voltage of CMC block.

Furthermore, it showcases transient response of the input voltage of FIA (XP, XN) along with its output (YP, YN) (refer to Fig. 3(c)). Additionally, the control voltages of the CMC, denoted as VCM,P and VCML,N are shown in Fig. 3(d). Additionally, the control voltages of the CMC, denoted as VCM,P and VCML,N are shown in Fig. 3(d).

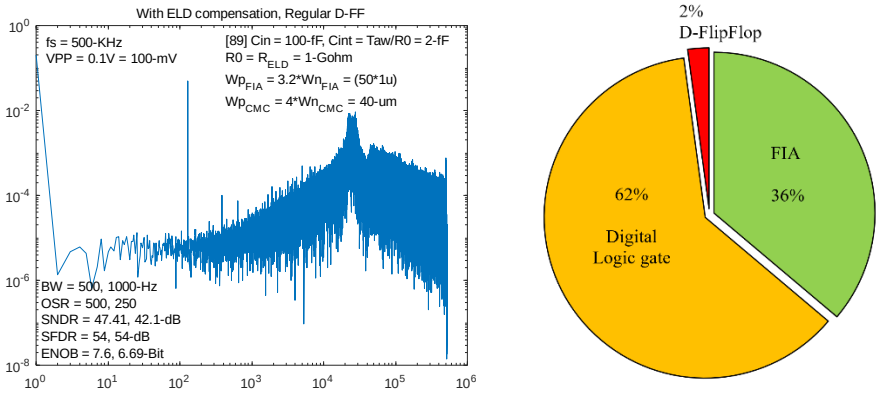
3 Results

The proposed $\sum\Delta$ modulator has been simulated using TSMC 180-nm technology. It is notable that the simulation is performed including device noise modeling (noise BW of 1-MHz). As indicated in Table. 1, which outlines the performance of the several state-of-art inverter-based CT-$\sum\Delta$ modulators, to best author's knowledge proposed modulator showcases its most compelling attributes in terms of power consumption (47-nW). In detail, the DB-FIOTA modulator power can be divided into two distinct sections primarily centered on the most consuming components (FIA, digital logic gates, and D-Flipflop). The frequency response spectrum illustrating noise shaping is depicted in Fig. 4.

Table 1. Performance summaries and comparison of state-of-the-art results.

Ref	This Work	[6]	[7]	[8]
fs [MS/s]	0.5	6.4	3.2	0.384
BW [kHz]	0.5	50	25	8
OSR	500	64	64	24
SNDR [dB]	47.41	68.5	74	80
SFDR [dB]	54	82.6	NA	NA
ENOB [Bit]	7.6	11.08	12	13
Power [nW]	17 (FIA) +29 (digital)+ 1 (D-Flipflop) = 47	26300	3e5	108.8e6
Tech [nm]	180	130	180	40
Supply [V]	0.4	0.3	0.5	1, 0.7
FOM_S [dB]	147.678	161.3	153.2	168.2

Compared to prior CT-$\sum\Delta$ modulators presented in recent literature in Table. 1, the DB-FIOTA power is 50X lower than lowest power dissipation in [7]. However, it is noteworthy to highlight that there is substantial headroom for improvement in overall performance particularly concerning parameters such as linearity (SNDR, ENOB).



a) b)

Fig. 4. a) Frequency spectrum of FI-DBOTA, b) Power consumption distribution pie-chart of overall architecture.

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