Analysis, Design and Experimental Assessment of a High Power Density Ceramic DC-Link Capacitor for a 800 V 550 kVA Electric Vehicle Drive Inverter

Analysis, Design and Experimental Assessment of a High Power Density Ceramic DC-Link Capacitor for a 800 V 550 kVA Electric Vehicle Drive Inverter

Davide Cittanti, *Member, IEEE,* Fausto Stella, *Member, IEEE,* Enrico Vico *Student Member, IEEE,* Chaohui Liu, Jinliang Shen, Guidong Xiu, and Radu Bojoi, *Fellow, IEEE*

***Abstract*—The drive inverter is a crucial component of an electric vehicle (EV) powertrain, being responsible for the DC/AC power conversion between the battery and the electric motor. The increasing demand for lower weight and higher conversion efficiency is opening new challenges, encouraging the adoption of new technologies (e.g., wide bandgap semiconductor devices). In particular, the DC-link capacitor typically represents the bulkiest inverter component, posing a strict limitation to the achievable converter power density and thus being subject to great pressure for improvement. In this context, novel ceramic capacitor technologies (e.g., PLZT) promise superior performance with respect to well established film-based solutions, featuring both higher specific capacitance and higher RMS current capability. Therefore, this paper focuses on the analysis, sizing, design and experimental assessment of a PLZT-based ceramic DC-link capacitor for next-generation EV drive inverters, including a comparative assessment with a state-of-the-art film-based solution. In particular, in view of the non-linear behavior of the PLZT capacitance value with respect to the DC-bias voltage and the amplitude of the excitation, a novel correlation between the effective large-signal capacitance and the peak-to-peak voltage ripple is derived experimentally, providing useful information for the DC-link capacitor sizing (i.e., not available from the capacitor manufacturer). For verification purposes, a full-scale DC-link capacitor prototype for a SiC MOSFET 800 V, 550 kVA, 20 kHz drive inverter is realized, demonstrating superior power density (i.e., ≈ two thirds smaller and ≈ one third lighter than a corresponding film-based solution). Finally, the inverter prototype is also exploited to validate experimentally the proposed DC-link peak-to-peak voltage ripple estimation procedure, based on the newly obtained large-signal capacitance characterization.**

***Index Terms*—three-phase inverter; DC-link capacitor; ceramic capacitors; film capacitors; electric vehicles (EVs)**

I. Introduction

During the last decade, as a result of government policies, technological development and consumer demand, electric vehicles (EVs) have rapidly become more and more attractive with respect to traditional internal combustion engine (ICE) vehicles. At present, the automotive industry is increasingly demanding lighter and more efficient EV powertrains, leading to considerable technological challenges [1].

D. Cittanti, F. Stella, E. Vico and R.Bojoi are with the Dipartimento Energia "G. Ferraris", Politecnico di Torino, Torino, 10129 Italy (e-mail: davide.cittanti@polito.it, fausto.stella@polito.it, enrico.vico@polito.it, radu.bojoi@polito.it)

C. Liu, J. Shen and G. Xiu are with the National New Energy Vehicle Technology Innovation Center (NEVC), Beijing, 102676 China (e-mail: liuchaohui@nevc.com.cn, shenjinliang@nevc.com.cn, xiuguidong@nevc.com.cn)

Manuscript received Month Day, Year; revised Month Day, Year.

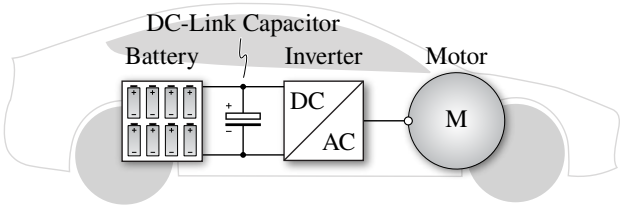


Fig. 1. Schematic overview of an electric vehicle (EV) powertrain, including the battery, the DC-link capacitor, the drive inverter and the electric motor.

An EV powertrain normally consists of a battery system, a traction inverter and an electric motor, as shown in Fig. 1. Being responsible for the full DC/AC power conversion between the battery and the electrical machine, the traction inverter is a crucial component and is thus subject to great pressure for improvement [1]–[3]. The main requirements of an automotive-grade inverter can be summarized in high power density (both volumetric and gravimetric), high conversion efficiency over a wide load range [4], high voltage operation (due to the ongoing shift to 800 V battery architectures [5], [6]), high temperature capability, and high switching frequency (to provide sufficient control margin and reduce PWM-induced losses in high-speed, low-inductance machines with several pole pairs typically adopted in automotive [7]–[9]).

While all mentioned requirements are progressively being addressed with the increasing adoption of modern wide bandgap (WBG) semiconductor devices, such as silicon carbide (SiC) MOSFETs and gallium nitride (GaN) HEMTs [10]–[12], and the adoption of multi-level inverter architectures [5], [12], [13], the achievable volumetric/gravimetric power density of modern EV drive inverters is still hindered by the DC-link capacitor. In fact, the sizing of state-of-the-art film-based DC-link capacitors is mostly unaffected by the higher switching frequencies enabled by WBG devices, as the limiting design criterion is typically the RMS current stress (i.e., unaffected by the switching frequency). Moreover, multi-level inverter topologies leave unaltered both DC-link RMS current and voltage ripple with respect to traditional two-level inverters [13], therefore being unable to reduce the DC-link capacitor size.

In this context, high-voltage ceramic capacitor technology (e.g., CeraLink® from TDK [14]) promises superior performance with respect to film-based solutions, featuring higher specific capacitance, higher RMS current capability, higher maximum temperature operation, lower equivalent series inductance (due to the smaller package), and decreasing

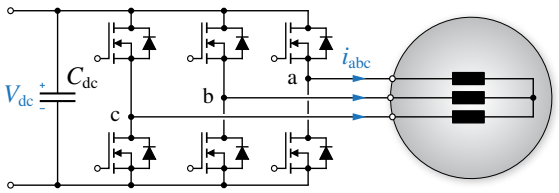


Fig. 2. Schematic overview of the considered two-level drive inverter system.

resistance with frequency (i.e., effectively benefiting from higher frequency operation). Although highly disregarded until recently, ceramic technology represents a key enabler for next-generation EV drive inverters, theoretically allowing for a significant performance leap in terms of gravimetric and volumetric power density [15], [16].

Lately, several research activities have been focused on improving the loss modeling accuracy of class II ferroelectric multi-layer ceramic capacitors (MLCCs) [17]–[22]. However, except for [15], [16], not enough attention has been dedicated to PLZT technology. Also, while several papers have described the sizing and design of three-phase inverter DC-link capacitors [23]–[25], according to the authors' best knowledge only few works focus on ceramic-based solutions [26], which nonetheless do not fully address the performance benefits unlocked by ceramic technology. Moreover, even though the authors in [15] and [16] provide a comparative performance assessment of different capacitor technologies suitable for EVs (including PLZT ceramic capacitors), the analysis is not validated with the design of a drive inverter DC-link.

Therefore, the main goal of this paper is to analyze, size, design and assess experimentally a high power density full-ceramic DC-link capacitor for a two-level EV drive inverter (cf. Fig. 2), meanwhile providing a comparison with a traditional state-of-the-art film-based solution. In particular, **the main contributions of this work can be summarized as:**

- a quantitative performance evaluation and comparison of automotive-grade film and ceramic capacitor technologies;
- a straightforward extension of the traditional sizing procedure of a two-level inverter DC-link capacitor, taking into account the frequency-dependent RMS current capability of ceramic technology;
- the experimental characterization of the electrical and thermal performance of a PLZT ceramic capacitor sample under large-signal excitation, deriving a novel relation between the peak-to-peak voltage ripple amplitude and the large-signal equivalent capacitance (crucial to the DC-link sizing, but not provided by the capacitor manufacturer);
- the design, realization and experimental assessment of a high power density full-ceramic DC-link capacitor.

In particular, this paper extends the work presented in [27], providing additional details, focusing on a different (more realistic) case study and bringing in added value, namely the experimental assessment of the full-ceramic DC-link capacitor and the validation of the newly derived relation between peak-to-peak voltage ripple amplitude and large-signal capacitance value. All experimental tests have been performed exploiting a $800\,\mathrm{V}$ $550\,\mathrm{kVA}$ $20\,\mathrm{kHz}$ EV traction inverter prototype integrating the designed full-ceramic DC-link capacitor.

This paper is structured as follows. In Section II the most suitable DC-link capacitor technologies for automotive application are described and a quantitative performance comparison among them is carried out. In Section III the stresses and the sizing criteria for a three-phase two-level inverter DC-link capacitor are briefly recalled, and the adopted DC-link design procedure is outlined. In Section IV a PLZT ceramic capacitor sample is experimentally characterized under large-signal operating conditions and a novel relation between peak-to-peak voltage ripple amplitude and effective capacitance is derived. In Section V a full-ceramic DC-link capacitor prototype for a SiC MOSFET $800\,\mathrm{V}$, $550\,\mathrm{kVA}$, $20\,\mathrm{kHz}$ EV drive inverter is sized, designed and constructed for verification purposes. In Section VI the DC-link capacitor prototype is assessed experimentally in terms of peak-to-peak voltage ripple exploiting a full-scale $550\,\mathrm{kVA}$ inverter operated at different DC-link voltage, output current and modulation index values. The experimental results are then compared with the proposed large-signal model-based estimations. Finally, Section VII summarizes and concludes this work.

II. Automotive DC-Link Capacitor Technologies

Automotive DC-link capacitors require high RMS current capability (i.e., low equivalent series resistance and high thermal conductivity), high specific capacitance, high maximum temperature operation, high self-resonance frequency (i.e., low equivalent series inductance), and high reliability (i.e., long mean time between failures). While electrolytic capacitors excel in terms of specific capacitance (i.e., energy density), they do not achieve acceptable performance in terms of the remaining criteria [28], therefore they are typically not adopted in high-voltage automotive drive inverters.

This section discusses the main features of film and ceramic capacitors for automotive DC-link application, providing a quantitative performance benchmark for both technologies.

A. Film Capacitors

Film capacitors are typically realized by interleaving plastic/polymer films (dielectrics) with metal foils (electrodes) [29], as illustrated in Fig. 3(a). The employed dielectric materials are non-polar and have low relative permittivity ($\varepsilon_\mathrm{r} \approx 2$–$3$), leading to lower capacitance density with respect to electrolytic capacitors. Nevertheless, they show little temperature dependence and are thus suited for high temperature operation, typically up to 100–$125\,^\circ\mathrm{C}$. Additionally, the self-healing properties of

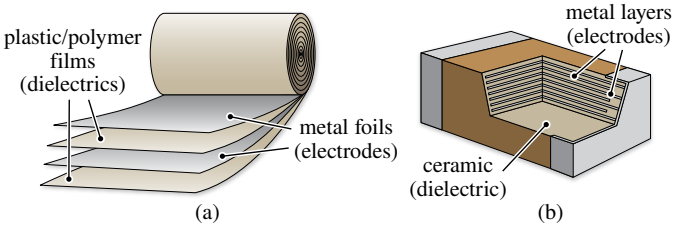


Fig. 3. Overview of the typical internal structure of (a) film capacitors and (b) multi-layer ceramic capacitors (MLCCs).

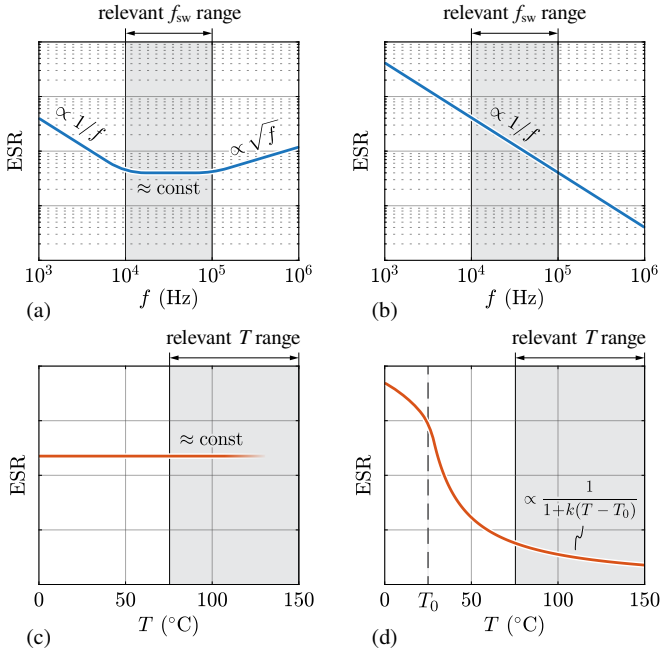


Fig. 4. Qualitative overview of the typical (a)–(b) frequency dependence and (c)–(d) temperature dependence of the equivalent series resistance (ESR) for (a),(c) film capacitors and (b),(d) PLZT ceramic capacitors. The relevant switching frequency and operating temperature ranges for automotive inverter DC-link applications (i.e., 10–100 kHz, 75–150 °C) are highlighted.

film capacitors substantially improve their reliability, making them a desirable choice in automotive applications. On the negative side, the equivalent series resistance (ESR) of film capacitors tends to be approximately constant with frequency in the 10–100 kHz range (cf. Fig 4(a)), after which the ESR starts increasing $\propto \sqrt{f}$ due to AC skin effect (i.e., depending on the thickness of metal foils and contacts) [29]. Therefore, the power losses and the RMS current capability of film-based DC-link capacitors are typically either unaltered or negatively affected by an inverter switching frequency increase. Further drawbacks of film capacitors in traction drive applications can be identified in their relatively high equivalent series inductance (i.e., due to the large physical size of high-power DC-link capacitors), which leads to low self-resonance frequencies and thus limits the frequency operating range of the capacitor itself, and their limited allowed self-heating temperature rise (i.e., $\approx$ 10–20°C) [29], which hinders their RMS current capability and potentially requires active thermal management.

B. Ceramic Capacitors

The typical structure of a ceramic capacitor is illustrated in Fig. 3(b), where ceramic dielectric layers with large relative permittivity (i.e., ε_r up to 10 000) are alternated with metal electrodes. Due to their structure, these capacitors are also known as multilayer ceramic capacitors (MLCCs), and can be classified into three main categories: class I, class II, and lead–lanthanum–zirconate–titanate (PLZT) capacitors [1]. In general, all ceramic capacitors feature higher specific RMS current capability than film capacitors and can operate at higher temperatures (i.e., up to 150 °C) [15]. Moreover, due to their inherent small size (i.e., the brittleness of the dielectric material limits the package dimensions) ceramic capacitors are characterized by low equivalent series inductance and are thus more suited for high-frequency applications. On the other hand, the upper limitation to the capacitor size requires the paralleling of tens/hundreds of units to achieve the required DC-link capacitance in traction inverter applications, posing substantial design and realization challenges to ensure symmetrical current sharing and to minimize the overall stray inductance [16].

Class I ceramic capacitors (e.g., C0G) employ a linear dielectric material with relatively low permittivity (i.e., $\varepsilon_r \approx 20$–40) and feature low temperature and DC voltage bias dependencies, trading excellent capacitance stability for a low capacitance/energy density. These characteristics make class I capacitors most suited for power electronics applications where constant capacitance is required, such as filters and/or resonant converters.

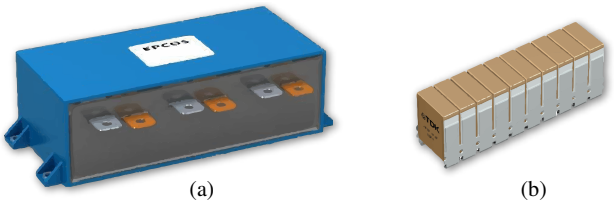
On the contrary, class II ceramic capacitors (e.g., X7R, X6R) can achieve much higher capacitance densities (i.e., suitable for DC-link applications), however they are characterized by a significant capacitance drop with increasing DC voltage bias and operating temperature, due to the employed non-linear ferroelectric dielectric materials. Furthermore, mainly due to the rigidity of the ceramic dielectric material, these capacitors can easily crack when they are subject to sufficient mechanical and thermal stresses, leading to possible short circuits between terminals. This aspect significantly affects the overall reliability of these components in harsh and vibrating environments, such as automotive applications, therefore they are not well suited for EV traction drive DC-links.

PLZT capacitors (e.g., CeraLink® from TDK [14]) represent emerging and promising candidates for automotive DC-link applications, since they employ an antiferroelectric dielectric material characterized by a permittivity increase with the DC voltage bias [30], [31]. In particular, this feature allows to store a higher amount of energy in nominal operating conditions (i.e., at rated voltage) with respect to class II capacitors. Moreover, the PLZT dielectric withstands and favours high temperature operation (i.e., up to 150 °C, with ESR decreasing approximately linearly with temperature, cf. Fig. 4(d)) and the copper electrodes provide enhanced electrical and thermal dissipation performance, enabling an unmatched specific RMS current capability. Additionally, the ESR of PLZT capacitors approximately decreases $\propto 1/f$, as shown in Fig. 4(b), allowing for a further RMS current capability increase with increasing inverter switching frequency (i.e., $I_{\mathrm{RMS}} \propto \sqrt{f_{\mathrm{sw}}}$), as opposed to film capacitors. Concerning reliability, the internal structure of PLZT capacitors consists in the equivalent series connection of two MLCCs [14] and enables the capacitor operation in case of a first crack (i.e., short circuit) in the dielectric, thus achieving higher reliability levels than other ceramic capacitor technologies. It is also worth noting that, even though the ESR of PLZT capacitors decreases with temperature (cf. Fig. 4(d)), above 75 °C the capacitance value shows a negative temperature coefficient, allowing for the natural balancing of the current among paralleled capacitors and thus avoiding thermal runaway [15]. All together, these features clearly indicate that PLZT capacitors represent the most suited ceramic-based candidates for EV traction drive

TABLE I
SPECIFICATIONS OF THE CONSIDERED BENCHMARK CAPACITORS.

	Film	Ceramic
Manufacturer	EPCOS (TDK)	TDK
Part Number	B25655P9127K151	CeraLink® FA10
Rated Voltage	900 V	900 V
Rated Capacitance	120 µF	1.3 µF*
Rated RMS Current	120 A	32 A
Maximum Temperature	105 °C	150 °C
Volume	554.4 cm^3	2.0 cm^3
Weight	800 g	11.5 g

*small-signal value at 800 V, used for DC-link sizing.



(a) (b)

Fig. 5. Highlight of the considered 900 V benchmark capacitors (not to scale): (a) EPCOS B25655P9127K151 [33], (b) TDK CeraLink® FA10 [34].

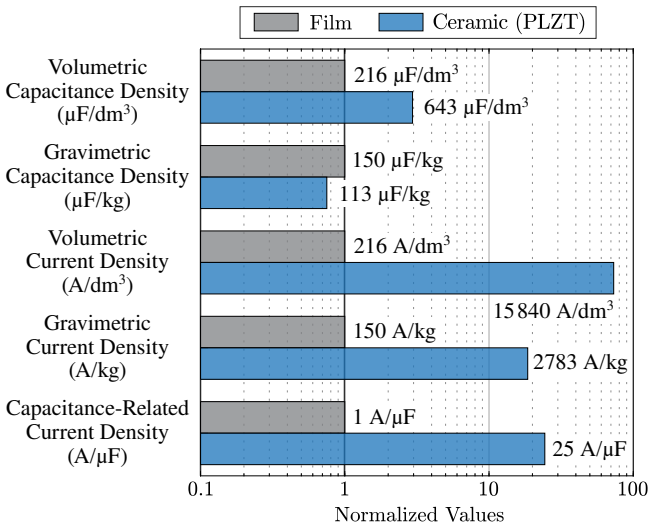


Fig. 6. Specific performance comparison between the selected benchmark film and ceramic (PLZT) capacitors. The specific performance indicators are normalized with respect to the film capacitor values and are shown in logarithmic scale.

DC-links. Therefore, CeraLink® technology from TDK will be considered as ceramic capacitor benchmark in the following sections. Dedicated performance comparisons between class II and PLZT ceramic capacitors can be found in [15], [16], [32].

C. Performance Comparison

In order to provide a quantitative comparative analysis between automotive film and ceramic (PLZT) DC-link capacitors, two commercially available high-performance 900 V solutions are considered as technology benchmarks, as reported in Table I and Fig. 5. Due to the very different parameter absolute values of the two capacitor models, the capacitance and RMS current values are expressed in relative terms to provide useful specific performance indicators, which are illustrated in Fig. 6. Since the PLZT capacitor features a variable capacitance that is positively correlated with the amplitude of the excitation, the manufacturer's datasheet provides different rated capacitance values for different applications (e.g., DC-link, snubber, etc.) [14]. In the present case, the small-signal capacitance value is considered, since it represents a worst-case (i.e., minimum) capacitance value for DC-link applications, where a relatively small voltage ripple is superimposed to a comparatively large DC bias voltage [14].

It is observed that the PLZT ceramic solution strongly outperforms the film one according to all specific performance indicators except for the gravimetric capacitance density, which results comparable. In particular, the ceramic solution excels in terms of RMS current carrying capability, which typically represents the limiting design criterion for film-based automotive DC-link capacitors. Therefore, it is evident that PLZT ceramic technology has the potential to significantly enhance the performance of EV traction inverter DC-links.

III. DC-Link Capacitor Sizing Procedure

The DC-link capacitor of a three-phase two-level inverter must simultaneously satisfy two main design criteria [24]: it must comply with the maximum RMS current stress determined by the application, which generates losses and affects the capacitor temperature rise, and it must ensure a predefined maximum peak-to-peak voltage ripple, which increases the peak voltage applied to the semiconductor devices and alters the ideal operation of the converter (i.e., the AC phase voltages).

Disregarding the switching frequency phase current ripple, the RMS current flowing into the DC-link capacitor can be expressed analytically as [35]

$$I_{\mathrm{C_{dc},RMS}} = I\sqrt{M\left[\frac{\sqrt{3}}{4\pi}+\cos^2\varphi\left(\frac{\sqrt{3}}{\pi}-\frac{9}{16}M\right)\right]}, \quad (1)$$

where I is the peak phase current value, $M = 2V/V_{\mathrm{dc}}$ is the inverter modulation index (i.e., $0 \le M \le 2/\sqrt{3}$ in linearity), φ is the load power factor angle, V is the reference peak phase voltage value and V_{dc} is the DC-link voltage. Remarkably, (1) is not affected by the inverter pulse-width modulation (PWM) strategy [35]. $I_{\mathrm{C_{dc},RMS}}$ is illustrated in normalized form (i.e., divided by the peak phase current I) in Fig. 7 as function of M and φ. The worst-case value of (1) is found for $\varphi = 0$ and $M = 10\sqrt{3}/9\pi$, obtaining:

$$I_{\mathrm{C_{dc},RMS,max}} = \frac{5}{2\sqrt{3}\pi}\, I \approx 0.46\, I. \quad (2)$$

The DC-link capacitor peak-to-peak charge ripple $\Delta Q_{\mathrm{C_{dc},pp}}$ (i.e., the high-frequency current-time area) is directly proportional to the voltage ripple $\Delta V_{\mathrm{dc,pp}}$ and provides a straightforward relation to size the DC-link capacitance value C_{dc} through its definition:

$$\Delta Q_{\mathrm{C_{dc},pp}} = C_{\mathrm{dc}}\, \Delta V_{\mathrm{dc,pp}}. \quad (3)$$

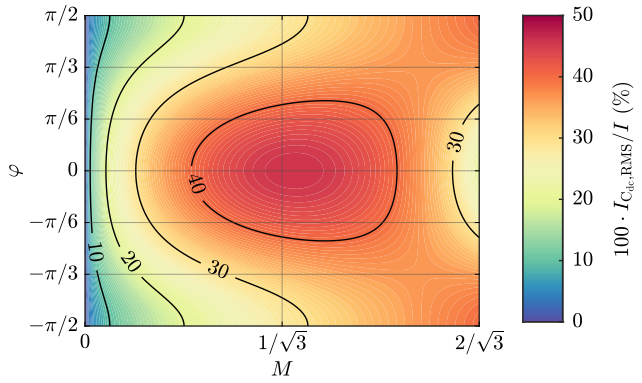


Fig. 7. Normalized DC-link capacitor RMS current $I_{\mathrm{C_{dc},RMS}}$ as function of the inverter modulation index M and the load power factor angle φ. The normalization factor is the peak phase current I.

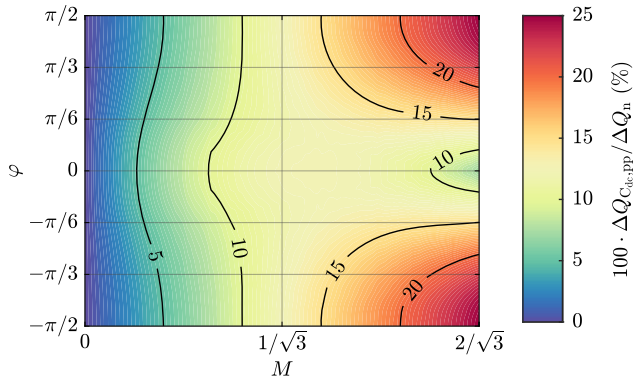


Fig. 8. Normalized DC-link capacitor peak-to-peak charge ripple $\Delta Q_{\mathrm{C_{dc},pp}}$ as function of the inverter modulation index M and the load power factor angle φ assuming SVPWM. The normalization factor is $\Delta Q_{\mathrm{n}} = I/f_{\mathrm{sw}}$.

Unfortunately, a general analytical expression of $\Delta Q_{\mathrm{C_{dc},pp}}$ valid for all operating conditions cannot be derived, as the maximum peak-to-peak value of the charge ripple within a fundamental period depends on M, φ and the selected modulation strategy, changing expression abruptly [36]. Therefore, $\Delta Q_{\mathrm{C_{dc},pp}}$ is calculated numerically considering space vector modulation (SVPWM) [37] and is illustrated in Fig. 8, where it is normalized with respect to $\Delta Q_{\mathrm{n}} = I/f_{\mathrm{sw}}$. The worst-case value of $\Delta Q_{\mathrm{C_{dc},pp}}$ is found for $M = 2/\sqrt{3}$ and $\varphi = \pm\pi/2$, obtaining [36]

$$\Delta Q_{\mathrm{C_{dc},pp,max}} = \frac{1}{4}\,\frac{I}{f_{\mathrm{sw}}}, \tag{4}$$

which is also independent of the PWM strategy.

The DC-link capacitance C_{dc} required by the application is obtained as the value that satisfies both the RMS current and peak-to-peak voltage ripple constraints, as:

$$C_{\mathrm{dc}} = \max\left[C_{\mathrm{dc,I_{RMS}}},\, C_{\mathrm{dc},\Delta V_{\mathrm{pp}}}\right]. \tag{5}$$

The expression of $C_{\mathrm{dc},\Delta V_{\mathrm{pp}}}$ can be directly derived from (3) and (4) assuming a specified value of $\Delta V_{\mathrm{dc,pp,max}}$, as

$$C_{\mathrm{dc},\Delta V_{\mathrm{pp}}} = \frac{\Delta Q_{\mathrm{C_{dc},pp,max}}}{\Delta V_{\mathrm{dc,pp,max}}} = \frac{1}{4}\,\frac{I}{f_{\mathrm{sw}}\,\Delta V_{\mathrm{dc,pp,max}}}, \tag{6}$$

whereas the expression of $C_{\mathrm{dc,I_{RMS}}}$ requires additional definitions and specific assumptions, which are provided in Appendix A. Therefore, considering the maximum RMS current stress $I_{\mathrm{C_{dc},RMS,max}}$ and assuming as a worst-case (i.e., conservative) scenario that the total DC-link RMS current stress features a single harmonic component at $f = f_{\mathrm{sw}}$, the expression of $C_{\mathrm{dc,I_{RMS}}}$ is obtained by manipulating (14):

$$C_{\mathrm{dc,I_{RMS}}} = C^* \,\frac{I_{\mathrm{C_{dc},RMS,max}}}{I^*_{\mathrm{RMS}}} \left(\frac{f^*}{f_{\mathrm{sw}}}\right)^{\alpha/2} \sqrt{\frac{T_{\mathrm{max}} - T^*_{\mathrm{a}}}{T_{\mathrm{max}} - T_{\mathrm{a}}}}, \tag{7}$$

where C^*, I^*_{RMS}, f^* and T^*_{a} are respectively the capacitance, the RMS current capability, the test frequency and the ambient temperature values provided in the manufacturer's datasheet, T_{max} is the maximum capacitor operating temperature (i.e., $T = T^* = T_{\mathrm{max}}$), T_{a} is the considered ambient temperature, and $\alpha \approx 0$ for film capacitors (i.e., ESR approximately independent of f_{sw} in the considered frequency range, cf. Fig. 4),

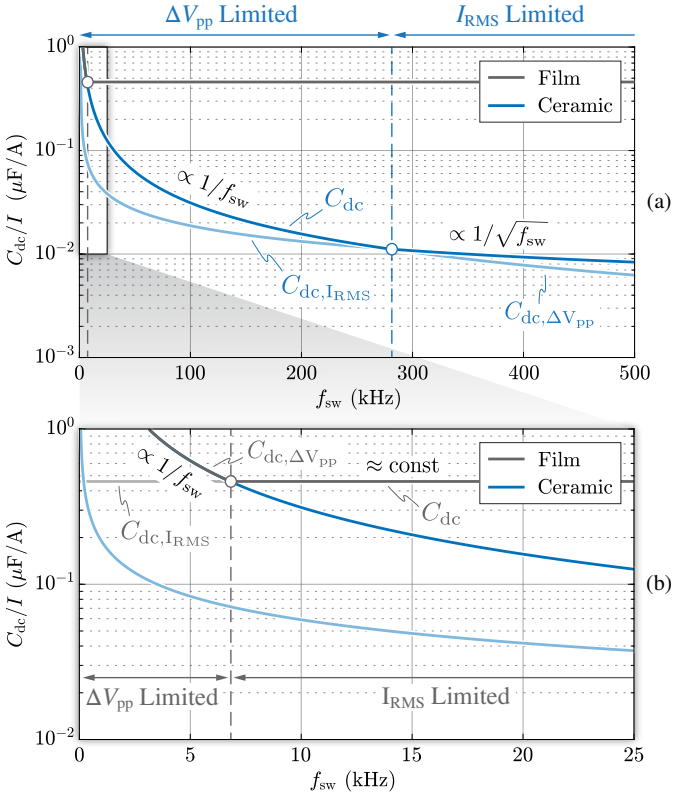


Fig. 9. DC-link capacitance C_{dc} requirement normalized with respect to the peak phase current I as function of the inverter switching frequency f_{sw} and the capacitor technology (i.e., film and PLZT ceramic, cf. Fig. 5), assuming $V_{\mathrm{dc}} = 800\,\mathrm{V}$, $\Delta V_{\mathrm{dc,pp,max}} = 10\,\% \cdot V_{\mathrm{dc}}$ and $T_{\mathrm{a}} = 85\,^{\circ}\mathrm{C}$. (a) $0 \le f_{\mathrm{sw}} \le 500\,\mathrm{kHz}$ and (b) $0 \le f_{\mathrm{sw}} \le 25\,\mathrm{kHz}$. The two regions where the DC-link capacitor sizing is respectively dominated by $C_{\mathrm{dc},\Delta V_{\mathrm{pp}}}$ (ΔV_{pp} limited) and by $C_{\mathrm{dc,I_{RMS}}}$ (I_{RMS} limited) are highlighted for both technologies.

whereas $\alpha \approx 1$ for CeraLink® capacitors (cf. Fig. 4).

The DC-link capacitance requirement for the considered film and PLZT ceramic technologies is shown in Fig. 9 in normalized form (i.e., divided by the peak phase current I) as function of the inverter switching frequency f_{sw}, assuming $V_{\mathrm{dc}} = 800\,\mathrm{V}$, $\Delta V_{\mathrm{dc,pp,max}} = 10\,\% \cdot V_{\mathrm{dc}}$ and $T_{\mathrm{a}} = 85\,^{\circ}\mathrm{C}$. It is observed that, depending on the value of f_{sw}, the main factor limiting the DC-link sizing is either the voltage ripple requirement (at low frequency) or the RMS current stress (at

high frequency). Moreover, while for film capacitors the RMS current criterion tends to dominate the sizing for $f_{sw} > 7\,\text{kHz}$ (cf. Fig. 9(b)), CeraLink® technology allows for a large capacitance reduction if higher switching frequency values can be exploited (cf. Fig. 9(a)). It is also worth highlighting that for both technologies, once the RMS current limit is reached, the DC-link capacitance decreasing trend either stops (for film technology) or slows down substantially (for ceramic technology). In particular, due to the reduction of ESR $\propto 1/f$ in CeraLink® capacitors, a non negligible DC-link reduction can still be obtained for higher switching frequencies.

IV. Experimental Characterization of PLZT Ceramic Capacitor Technology

To assess the validity of the assumptions adopted within the drive inverter DC-link sizing procedure of Section III, electrical and thermal measurements are performed on a 900 V 390 nF (i.e., rated small-signal value C^*) CeraLink® FA3 capacitor sample [34], for reasons of testing simplicity.

Fig. 10 shows the schematic of the adopted experimental setup. The device under test (DUT) is used as the DC-link of a SiC MOSFET synchronous buck converter operated at constant duty cycle (i.e., $d = 0.5$) and is completely decoupled from the DC power supply by means of a large inductance, such that the AC component of the current switched by the buck converter entirely flows through the DUT. Therefore, the capacitor is subject to a symmetric square wave current with amplitude $I_o/2$ and frequency f_{sw} (cf. Fig. 11), leading to the following stress expressions:

$$I_{RMS} = \frac{I_o}{2}, \quad \Delta Q_{pp} = \frac{1}{4}\frac{I_o}{f_{sw}}. \tag{8}$$

Notably, all three degrees of freedom of the realized experimental setup (i.e., the DC voltage bias V_{dc}, the output load current I_o and the switching frequency f_{sw}, cf. Fig. 10) are exploited to perform a wide range of tests and assess the performance of the selected capacitor under small- and large-signal excitation.

A. Peak-to-Peak Voltage Ripple

The equivalent capacitance C_{eq} value of CeraLink® capacitors varies with the amplitude of the excitation (i.e., voltage ripple) [14], due to the hysteretic behaviour of the utilized antiferroelectric PLZT dielectric. Therefore, the first experimental tests aim at assessing the peak-to-peak voltage ripple performance of the DUT as function of the imposed charge ripple (i.e., varying the output current according to (8)). Notably, no such relation is provided by the capacitor manufacturer, although it is of utmost importance to accurately size the DC-link capacitance.

Fig. 12(a) and Fig. 12(b) show the peak-to-peak voltage ripple ΔV_{pp} and the equivalent capacitance $C_{eq} = \Delta Q_{pp}/\Delta V_{pp}$ obtained experimentally as functions of the peak-to-peak charge ripple ΔQ_{pp} and the DC voltage bias V_{dc}. The tests are carried out by performing short switching burst periods at $f_{sw} = 25\,\text{kHz}$, in order not to heat up the DUT during the measurements and keep its temperature approximately constant (i.e., $T \approx T_a = 23\,^\circ\text{C}$). It is observed that the voltage ripple

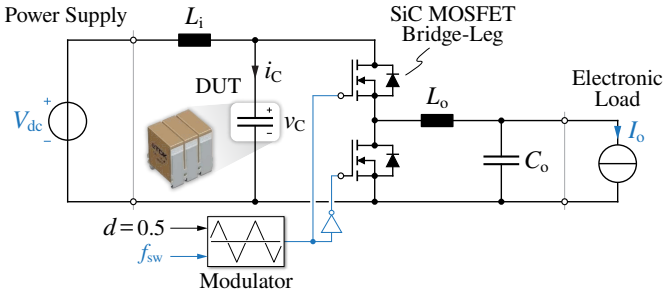


Fig. 10. Equivalent circuit schematic of the adopted experimental setup for the performance assessment of a CeraLink® FA3 capacitor (i.e., 900 V, 0.39 µF) [34]. The bridge-leg employs Wolfspeed C3M0032120K SiC MOSFETs (1200 V, 32 mΩ) and the values of the filtering elements are $L_i = L_o = 64\,\text{mH}$, $C_o = 66\,\mu\text{F}$. The operating conditions of the device under test (DUT) can be changed by varying V_{dc}, I_o and f_{sw}.

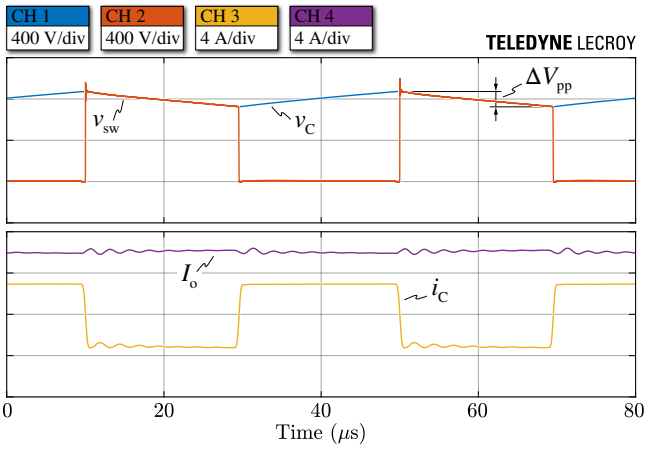


Fig. 11. Experimental waveforms obtained with $V_{dc} = 800\,\text{V}$, $f_{sw} = 25\,\text{kHz}$ and $I_o = 6\,\text{A}$. v_C and i_C are the DUT voltage and current, respectively, v_{sw} is the bridge-leg switching node voltage and I_o is the output current.

does not rise linearly with the charge ripple excitation (cf. Fig. 12(a)), leading to an increase in C_{eq} for higher ripple amplitudes (cf. Fig. 12(b)). Furthermore, it is shown that the DC bias voltage significantly impacts the C_{eq} value, highlighting the antiferroelectric behaviour of the DUT.

By expressing C_{eq} as function of ΔV_{pp}, Fig. 12(c) is obtained. Remarkably, the large-signal relation $C_{eq}(\Delta V_{pp})$ provides crucial information for the correct design of a PLZT-based DC-link capacitor, not available in the manufacturer's datasheet. Focusing on the curve obtained at $V_{dc} = 800\,\text{V}$, it is observed that for low values of ΔV_{pp} the measured equivalent capacitance is below the rated small-signal capacitance value $C^* = 390\,\text{nF}$. Despite the capacitance increase with the amplitude of the excitation, C_{eq} remains below C^* in the selected design point (i.e., $\Delta V_{dc,pp,max} = 10\,\% \cdot V_{dc} = 80\,\text{V}$, cf. Section V), resulting in a $\approx 11\,\%$ capacitance mismatch.

B. RMS Current Capability

To verify the current scaling laws introduced in Appendix A and used to derive (7), thermal measurements are performed at $V_{dc} = 800\,\text{V}$ to assess the DUT temperature rise as function of the RMS current stress I_{RMS} and the switching frequency f_{sw}. A thermal camera is employed to monitor the capacitor

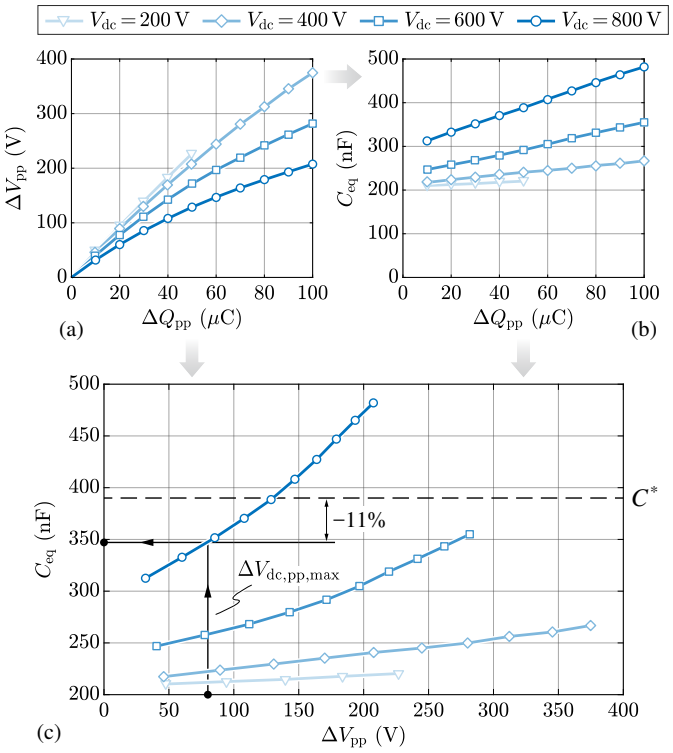


Fig. 12. Experimental (a) peak-to-peak voltage ripple ΔV_{pp} and (b) equivalent capacitance $C_{\mathrm{eq}} = \Delta Q_{\mathrm{pp}}/\Delta V_{\mathrm{pp}}$ as functions of the peak-to-peak charge ripple $\Delta Q_{\mathrm{pp}} = I_{\mathrm{o}}/4 f_{\mathrm{sw}}$ at $f_{\mathrm{sw}} = 25\,\mathrm{kHz}$, $T_{\mathrm{a}} = 23\,^{\circ}\mathrm{C}$ and variable DC bias voltage V_{dc}. C_{eq} is also illustrated in (c) as function of ΔV_{pp}: the maximum peak-to-peak voltage ripple defined by the application is highlighted (i.e., $\Delta V_{\mathrm{dc,pp,max}} = 10\,\% \cdot V_{\mathrm{dc}} = 80\,\mathrm{V}$, cf. Section V), showing that C_{eq} is $\approx 11\,\%$ lower than the rated small-signal capacitance value $C^* = 390\,\mathrm{nF}$ [34].

temperature rise with respect to the ambient (i.e., $T_{\mathrm{a}} = 23\,^{\circ}\mathrm{C}$). The results are reported in Fig. 13. It is immediately observed that the temperature rises approximately $\propto I_{\mathrm{RMS}}$ (i.e., instead of $\propto I_{\mathrm{RMS}}^2$), suggesting that the capacitor ESR decreases linearly with the temperature rise. This can be easily inferred by simplifying the temperature dependence expression of the ceramic capacitor (cf. Fig. 4(d)), under the assumption of high values of k or T, such that $k\,(T - T_0) \gg 1$:

$$\frac{R_{\mathrm{ESR}}(T)}{R_{\mathrm{ESR}}(T_0)} = \frac{1}{1 + k\,(T - T_0)} \approx \frac{1}{k\,(T - T_0)}. \tag{9}$$

Furthermore, Fig. 13 shows that halving the switching frequency leads to a $\approx \sqrt{2}$ increase of the temperature rise, which is strictly related to capacitor losses (i.e., $\propto$ ESR). Since the capacitor ESR is inversely proportional to the temperature rise according to (9), compensating for this effect (i.e., multiplying by $\sqrt{2}$) allows to see that the switching frequency halving leads to the doubling of the ESR (and losses) for a fixed capacitor temperature. This successfully verifies the small-signal $R_{\mathrm{ESR}} \propto 1/f$ trend also for large-signal excitation levels.

V. Design Case Study: 550 kVA Inverter

In this section, the capacitor sizing procedure described in Section III is applied to a specific case study and a full-ceramic DC-link prototype is designed and realized. The

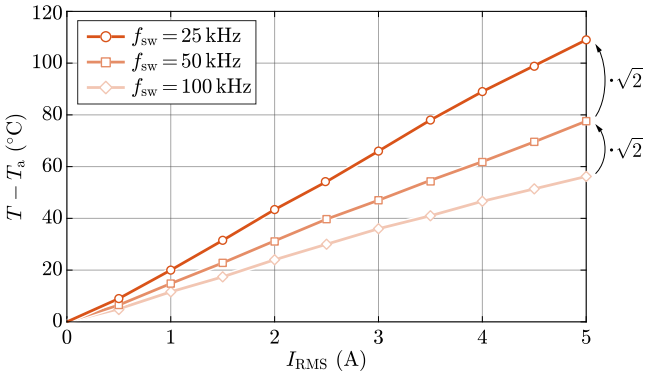


Fig. 13. Experimental capacitor temperature rise as function of the RMS current stress I_{RMS} at $V_{\mathrm{dc}} = 800\,\mathrm{V}$, $T_{\mathrm{a}} = 23\,^{\circ}\mathrm{C}$ and variable switching frequency f_{sw}.

TABLE II
Inverter Specifications and Nominal Operating Conditions.

Parameter	Description	Value
S	Apparent Power	550 kVA
I	Peak Phase Current	795 A
V_{dc}	DC-Link Voltage	800 V
f_{sw}	Switching Frequency	20 kHz

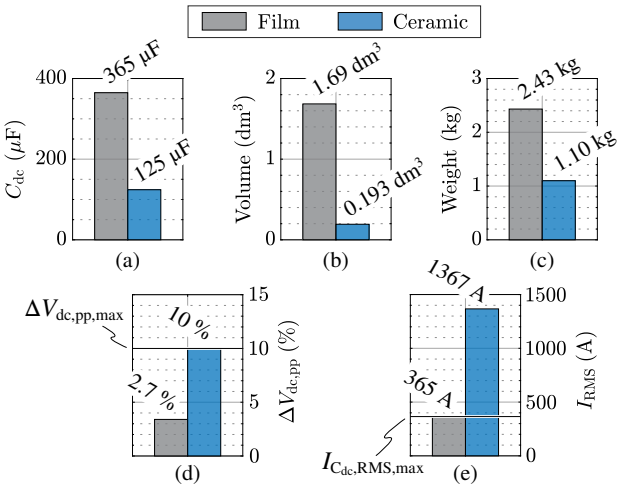


Fig. 14. Film vs. PLZT ceramic DC-link capacitor sizing according to the procedure outlined in Section III, considering the specific performance indices illustrated in Fig. 6 and assuming $\Delta V_{\mathrm{dc,pp,max}} = 10\,\% \cdot V_{\mathrm{dc}}$, $T_{\mathrm{a}} = 85\,^{\circ}\mathrm{C}$ and the inverter specifications reported in Table II. (a) DC-link capacitance C_{dc}, (b) volume, (c) weight, (d) normalized peak-to-peak voltage ripple $\Delta V_{\mathrm{dc,pp}}$, (e) RMS current capability I_{RMS}. The film capacitor size is determined by the RMS current stress (I_{RMS} limited), whereas the PLZT ceramic capacitor size is dictated by the required peak-to-peak voltage ripple (ΔV_{pp} limited).

target specifications and nominal operating conditions of the considered three-phase drive inverter are reported in Table II.

A. DC-Link Capacitor Sizing

A film-based and a PLZT ceramic-based DC-link solutions are sized according to the procedure outlined in Section III, considering the specific performance indices illustrated in Fig. 6, the inverter specifications reported in Table II and

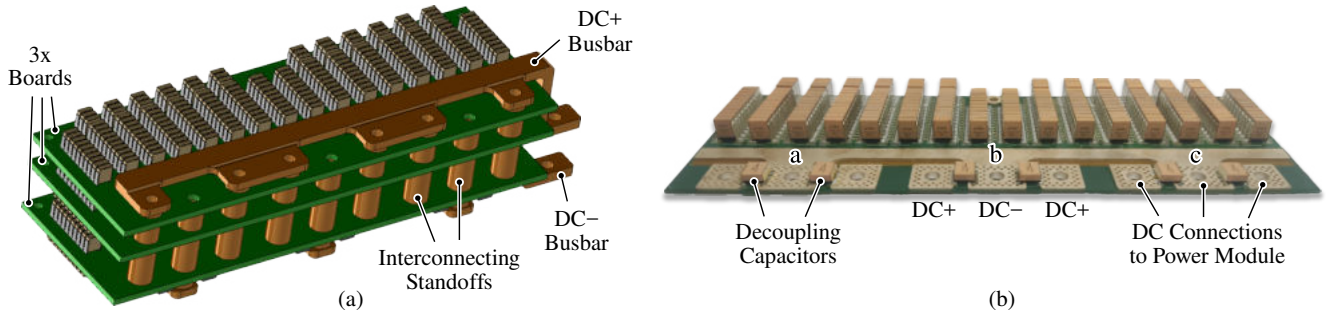


Fig. 15. (a) 3D design view of the full-ceramic DC-link concept and (b) bottom view of the DC-link board directly connected to the power modules.

assuming a target maximum peak-to-peak voltage ripple $\Delta V_{\mathrm{dc,pp,max}} = 10\,\% \cdot V_{\mathrm{dc}} = 80\,\mathrm{V}$ and an inverter internal ambient temperature $T_{\mathrm{a}} = 85\,^{\circ}\mathrm{C}$. Exploiting expressions (5), (6) and (7), the sizing results in terms of capacitance, volume, weight, peak-to-peak voltage ripple and RMS current capability are reported in Fig. 14. In particular, the minimum required capacitance values for the film and the PLZT ceramic capacitor technologies are $365\,\mu\mathrm{F}$ and $125\,\mu\mathrm{F}$, respectively. Notably, since no large-signal experimental characterization (cf. Section IV) had been performed at the time of the DC-link sizing, the small-signal capacitance value provided by the manufacturer was assumed as a worst-case scenario (i.e., being the effective capacitance value strictly increasing with the amplitude of the excitation) and was thus exploited for the sizing of the DC-link. Unfortunately, as shown in Fig. 12, this assumption translates in an overestimation of the actual DC-link capacitance by $\approx 11\,\%$ when assuming $V_{\mathrm{dc}} = 800\,\mathrm{V}$ and $\Delta V_{\mathrm{dc,pp,max}} = 80\,\mathrm{V}$, effectively leading to a DC-link undersizing. This further supports the relevance of the large-signal $C_{\mathrm{eq}}(\Delta V_{\mathrm{pp}})$ relation derived in Section IV.

As expected from Section II-C, it is observed that the CeraLink® solution achieves significantly superior theoretical performance with respect to the film-based solution, in terms of both DC-link volume and weight. Remarkably, the large reduction in weight and volume is to be mainly attributed to the high specific RMS current capability of PLZT ceramic technology, and not to its high volumetric/gravimetric capacitance density. In fact, since the RMS current limit is not encountered up to very high f_{sw} values (cf. Fig. 9), the inverter switching frequency increase allows to significantly reduce the total capacitance requirement. This is not the case for the film-based solution, which encounters the RMS current limit at relatively low frequency (i.e., $\approx 7\,\mathrm{kHz}$, cf. Fig. 9), after which no significant benefits are obtained by a f_{sw} increase.

B. DC-Link Capacitor Realization

A full-ceramic DC-link capacitor prototype, illustrated in Fig. 15, is designed and constructed for verification purposes. It consists of three identical double-side $800\,\mu\mathrm{m}$ thick copper PCBs housing several $900\,\mathrm{V}$ CeraLink® capacitors in parallel, achieving a total small-signal capacitance of $128\,\mu\mathrm{F}$ (i.e., slightly higher than the minimum required value of $125\,\mu\mathrm{F}$, cf. Fig 14). The complete capacitor assembly consists of 80 FA10 B58035U9255M001 [34] ($1.3\,\mu\mathrm{F}$ each), 60 FA3 B58035U9754M062 [34] ($0.39\,\mu\mathrm{F}$ each) and 6 LP B58031U9254M062 [38] ($0.13\,\mu\mathrm{F}$ each). In particular, the 6 capacitors belonging to the LP series are placed only on the bottom board in correspondence of the DC terminals of the power modules as shown in Fig. 15(b) (cf. decoupling capacitors), with the specific purpose of minimizing the commutation loop inductance. It should be noted that the capacitors are mounted on both top and bottom sides of the two lower boards, whereas the third board features capacitors only on the top side, as shown in Fig. 15(a).

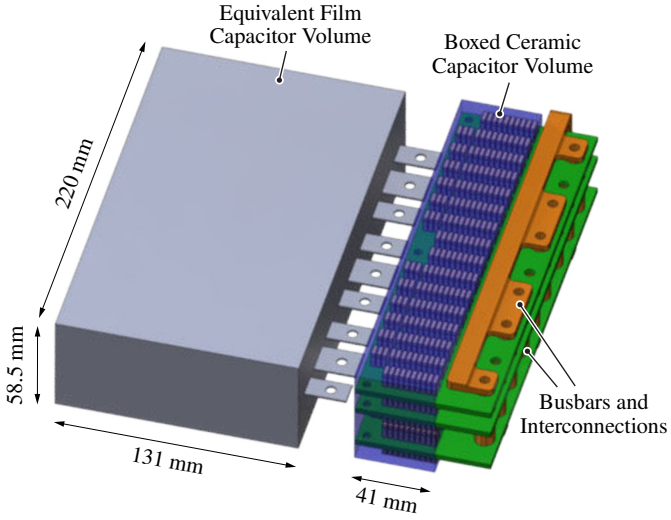


Fig. 16. 3D model comparison between the designed full-ceramic (PLZT) DC-link capacitor assembly and the performance-equivalent film-based solution.

Excluding busbars and interconnections to the power modules, the total weight of the full-ceramic DC-link capacitor assembly is $1.73\,\mathrm{kg}$, whereas its total boxed volume is $0.53\,\mathrm{dm}^3$ (i.e., $220\,\mathrm{x}\,41\,\mathrm{x}\,58.5\,\mathrm{mm}$), as shown in Fig. 16. It can be noticed that these weight and volume figures are well above the ones achievable theoretically (cf. Fig. 14), respectively by ≈ 1.6 times and ≈ 2.7 times. While the weight increment is directly associated with the addition of the thick-copper PCB (i.e., not considered in the analysis), the volume increment can be mostly attributed to the clearance and creepage requirements (i.e., determining the physical distance between devices). It is worth noting that the volume of the assembly could be significantly reduced by exploiting dielectric molding compounds and industrial manufacturing techniques.

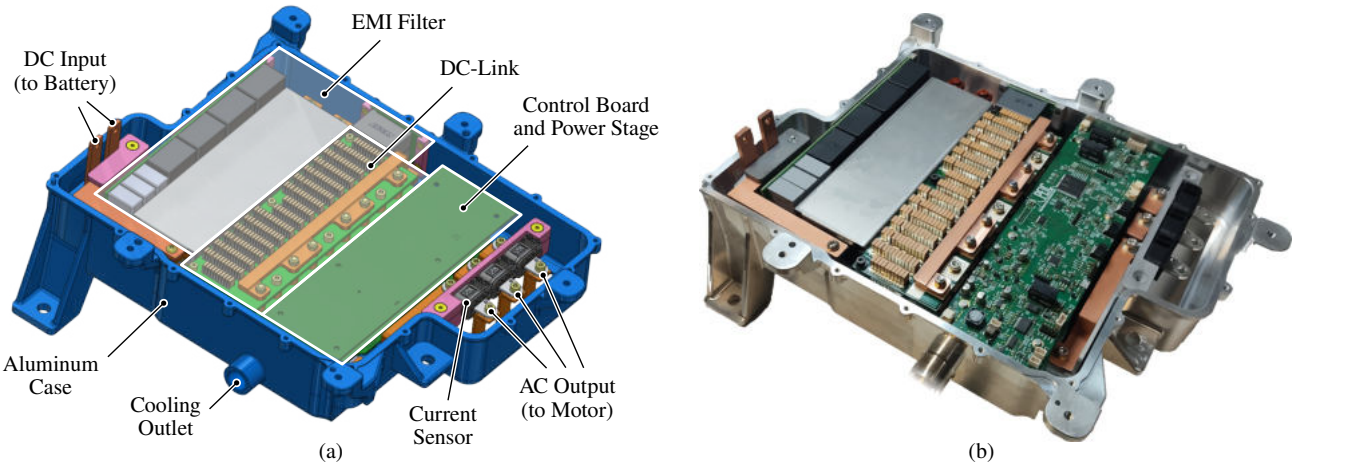


Fig. 17. (a) 3D design view of the realized 800 V 550 kVA EV traction inverter and (b) prototype view. The system consists of the power semiconductor stage (with control board and liquid-cooled heatsink), the DC-link capacitor assembly and a DC-side EMI filter enclosed in a waterproof IP 67 aluminum case [39].

Nevertheless, despite the inefficient space usage, the realized solution features 69 % lower volume and 29 % lower weight than the theoretical film-based counterpart (i.e., $1.69\,\mathrm{dm}^3$, $2.43\,\mathrm{kg}$), also illustrated in Fig. 16 for visual comparison.

C. Drive Inverter System Overview

The complete three-phase drive inverter prototype integrating the designed DC-link capacitor has been presented in [39] and is shown in Fig. 17. The system consists of the power semiconductor stage, the DC-link capacitor assembly and a DC-side EMI filter, all enclosed in a waterproof IP 67 aluminum case. In particular, the power stage features three separate half-bridge $1200\,\mathrm{V}$ $2.1\,\mathrm{m\Omega}$ SiC MOSFET automotive power modules from Danfoss (i.e., DP660B1200T105606). These power modules are actively cooled leveraging an integrated direct cooling technology and a custom heatsink, enabling high current operation (i.e., up to the rated $795\,\mathrm{A}$). Additionally, the DC-side EMI filter is designed to comply with the CISPR 25 class 3 electromagnetic interference (EMI) standard, ensuring that the inverter DC-side current/voltage ripple does not reach the rest of the system (i.e., the battery). Notably, the drive inverter prototype of Fig. 17 features full closed-loop control, achieved with a purposely developed control board.

VI. Experimental Assessment

To validate the proposed full-ceramic DC-link sizing procedure (cf. Section III) and design (cf. Section V), the DC-link peak-to-peak voltage ripple is assessed exploiting the $800\,\mathrm{V}$ $550\,\mathrm{kVA}$ inverter prototype in Fig. 17.

The equivalent circuit schematic of the adopted experimental setup is illustrated in Fig. 18. Leveraging the embedded high-bandwidth ($\approx 1\,\mathrm{kHz}$) closed-loop current control, the inverter has been tested on a three-phase inductive load (i.e., $\varphi \approx \pi/2$) featuring an inductance equal to $105\,\mu\mathrm{H}$ and a saturation current value of $400\,\mathrm{A}$. For reasons of consistency among all measurements, an AC fundamental frequency of $400\,\mathrm{Hz}$ has been set to achieve adequate inverter modulation index values.

Several tests have been performed, varying the peak phase current I from $0\,\mathrm{A}$ to $400\,\mathrm{A}$ and the DC-link voltage V_dc from

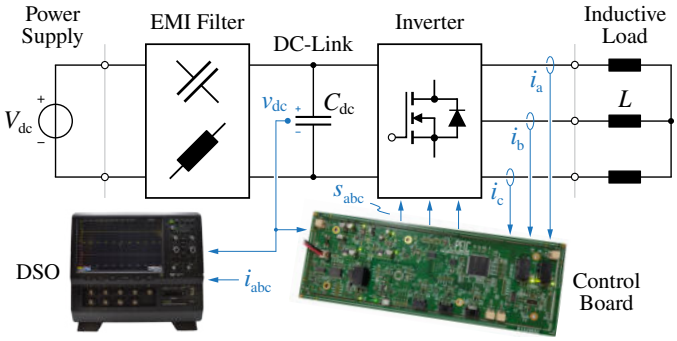


Fig. 18. Equivalent circuit schematic of the adopted experimental setup for the assessment of the DC-link peak-to-peak voltage ripple $\Delta V_\mathrm{dc,pp}$ in the realized $800\,\mathrm{V}$ $550\,\mathrm{kVA}$ inverter prototype. The three-phase output currents i_abc are closed-loop controlled to the desired reference value. The load inductors feature $L = 105\,\mu\mathrm{H}$ up to their saturation current value $I_\mathrm{sat} = 400\,\mathrm{A}$.

$200\,\mathrm{V}$ to $800\,\mathrm{V}$. Fig. 19 shows the experimental phase current waveforms i_abc and DC-link voltage ripple waveform v_dc (i.e., obtained with an AC-coupled voltage probe) for different test conditions, namely fixed output peak phase current $I = 400\,\mathrm{A}$ and variable DC-link voltage V_dc equal to $200\,\mathrm{V}$, $400\,\mathrm{V}$, $600\,\mathrm{V}$ and $800\,\mathrm{V}$. The waveforms show the significant impact of the DC-link voltage bias on the amplitude of the voltage ripple, to be attributed to two independent factors. Firstly, due to the passive (i.e., inductive) nature of the load and being the AC phase current peak I and fundamental frequency f fixed independently of the DC-link voltage value, the modulation index is inversely proportional to V_dc (i.e., $M \approx 4\pi f L I / V_\mathrm{dc} \propto 1/V_\mathrm{dc}$), linearly affecting the peak-to-peak charge ripple for $\varphi \approx \pi/2$ (cf. Fig. 8). Secondly, the variable and non-linear behavior of the PLZT capacitance value increases together with V_dc (cf. Fig 12(b)), leading to even lower peak-to-peak voltage ripple for high V_dc values.

A. DC-Link Voltage Ripple Estimation

To verify the accuracy and applicability of the large-signal capacitance relation $C_\mathrm{eq}(\Delta V_\mathrm{pp})$ derived in Section IV (cf. Fig. 12), the measured peak-to-peak DC-link voltage ripple

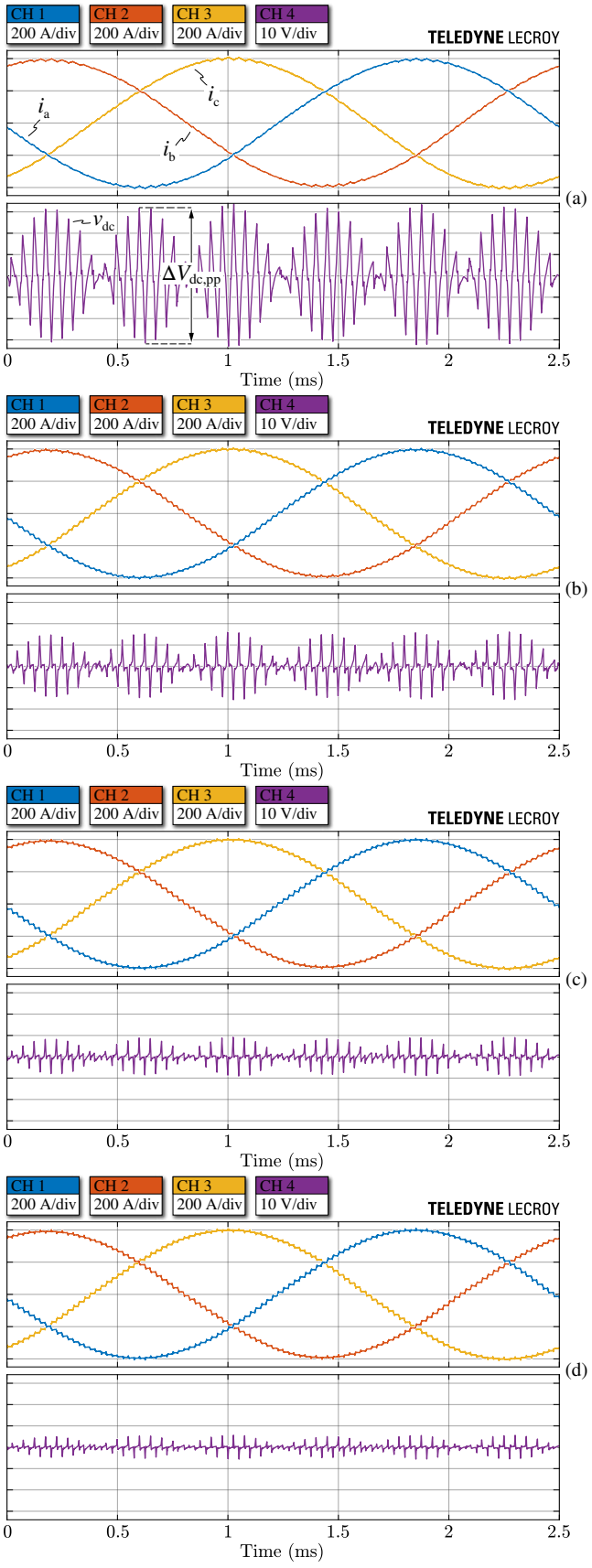


Fig. 19. Experimental phase current waveforms i_{abc} and DC-link voltage ripple waveform v_{dc} with $I = 400$ A and (a) $V_{dc} = 200$ V, (b) $V_{dc} = 400$ V, (c) $V_{dc} = 600$ V, (d) $V_{dc} = 800$ V. A digital low-pass filter with a 1 MHz (i.e., $50 f_{sw}$) cutoff frequency is applied to v_{dc}, to remove the switching noise.

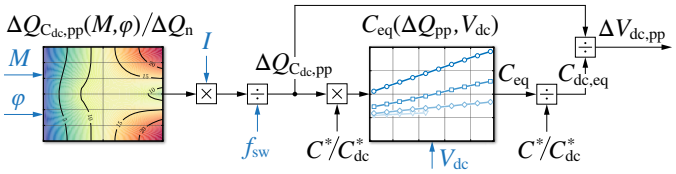


Fig. 20. Flowchart of the adopted procedure to estimate the peak-to-peak DC-link voltage ripple $\Delta V_{dc,pp}$ for given modulation index M, load power factor angle φ, phase current peak I, switching frequency f_{sw} and DC-link voltage bias V_{dc}. Linear interpolation among the experimental characterization results reported in Fig. 12(b) is exploited to obtain C_{eq} and thus $C_{dc,eq}$.

$\Delta V_{dc,pp}$ is compared with a model-based estimation. The flowchart of the adopted voltage ripple estimation procedure for a given operating condition (i.e., determined by V_{dc}, I, M, φ, f_{sw}) is illustrated in Fig. 20 and consists of the following steps:

- the normalized DC-link peak-to-peak charge ripple $\Delta Q_{C_{dc},pp}/\Delta Q_n$ is determined by M and φ according to the numerical relation illustrated in Fig. 8;
- $\Delta Q_{C_{dc},pp}/\Delta Q_n$ is denormalized according to the actual values of I and f_{sw}, obtaining $\Delta Q_{C_{dc},pp}$;
- $\Delta Q_{C_{dc},pp}$ is rescaled to the equivalent charge ripple ΔQ_{pp} of a single capacitor unit (i.e., multiplied by C^*/C^*_{dc});
- the experimental characterization of a single PLZT capacitor unit reported in Section IV is exploited to derive the equivalent large-signal capacitance value C_{eq} as function of ΔQ_{pp} and V_{dc} (cf. Fig. 12(b));
- the large-signal equivalent capacitance C_{eq} is rescaled to the total DC-link capacitor assembly (i.e., divided by C^*/C^*_{dc}), obtaining $C_{dc,eq}$;
- the estimated DC-link peak-to-peak voltage ripple $\Delta V_{dc,pp}$ is calculated as $\Delta Q_{C_{dc},pp}/C_{dc,eq}$.

B. Comparative Results

The peak-to-peak DC-link voltage ripple values obtained experimentally are compared to the model-based estimations and are reported in Table III. The same results are graphically illustrated in Fig. 21, where they are reported as functions of the peak phase current I and the DC-link voltage V_{dc} in (a), and as functions of the modulation index M and the peak phase current I in (b). As previously mentioned, it is worth remarking that the modulation index M is tightly related to the DC-link voltage V_{dc} and the peak phase current I values, due to the inductive load configuration and the constant fundamental frequency f (i.e., $M \approx 4\pi f L I/V_{dc} \propto I/V_{dc}$).

It is observed that the adoption of the large-signal capacitance relation $C_{eq}(\Delta V_{pp})$ experimentally derived in Section IV, together with the estimation procedure illustrated in Fig. 20, leads to excellent agreement between measured and estimated DC-link peak-to-peak voltage ripple values. In particular, a maximum deviation of $\approx \pm 7\,\%$ (including the measurement accuracy) is obtained across all tested operating conditions, successfully verifying the applicability of the large-signal capacitance measurements of Section IV.

Fig. 21(a) also shows the value of $\Delta V_{dc,pp}$ estimated assuming the small-signal capacitance value C^*_{dc} at $V_{dc} = 800$ V

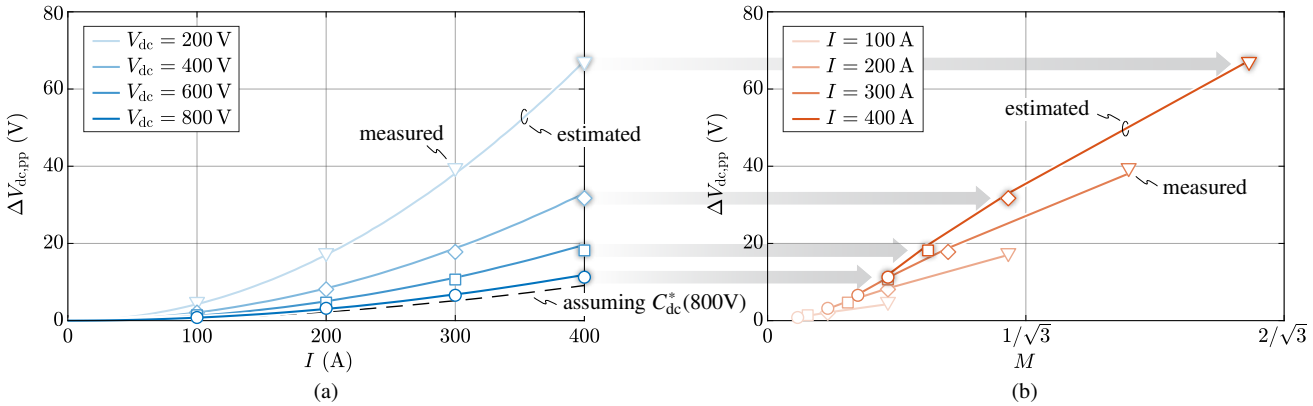


Fig. 21. Measured and estimated (cf. Fig. 20) DC-link peak-to-peak voltage ripple $\Delta V_{dc,pp}$ (a) as function of peak phase current I and DC-link voltage V_{dc}, and (b) as function of modulation index M and peak phase current I with power factor angle $\varphi \approx \pi/2$ and switching frequency $f_{sw} = 20\,\text{kHz}$. The value of M is tightly related to V_{dc} and I, due to the inductive load configuration and the constant fundamental frequency f (i.e., $M \approx 4\pi f L I / V_{dc} \propto I/V_{dc}$). The dashed line in (a) represents the value of $\Delta V_{dc,pp}$ estimated assuming the small-signal capacitance value C^*_{dc} at $V_{dc} = 800\,\text{V}$.

TABLE III
MEASURED AND ESTIMATED DC-LINK VOLTAGE RIPPLE.

V_{dc}	I	M	Measured $\Delta V_{dc,pp}$	Estimated $\Delta V_{dc,pp}$	Relative Error
200 V	100 A	0.269	4.3 V	4.3 V	+0.0 %
200 V	200 A	0.538	17.0 V	17.0 V	+0.0 %
200 V	300 A	0.807	39.0 V	38.1 V	−2.3 %
200 V	400 A	1.076	66.5 V	67.3 V	+1.2 %
400 V	100 A	0.135	2.1 V	2.1 V	+0.0 %
400 V	200 A	0.269	8.1 V	8.4 V	+3.7 %
400 V	300 A	0.404	17.8 V	18.8 V	+5.6 %
400 V	400 A	0.538	31.7 V	33.0 V	+4.1 %
600 V	100 A	0.090	1.4 V	1.3 V	−7.1 %
600 V	200 A	0.179	4.7 V	5.0 V	+6.4 %
600 V	300 A	0.269	10.6 V	11.2 V	+5.7 %
600 V	400 A	0.359	18.2 V	19.6 V	+7.7 %
800 V	100 A	0.067	0.8 V	0.8 V	+0.0 %
800 V	200 A	0.135	3.2 V	3.0 V	−6.3 %
800 V	300 A	0.202	6.6 V	6.8 V	+3.0 %
800 V	400 A	0.269	11.3 V	11.9 V	+5.3 %

provided by the PLZT capacitor manufacturer (dashed line). This approach leads to a significant underestimation of the voltage ripple (i.e., $\approx 20\,\% - 30\,\%$) in the considered operating conditions, further emphasizing the benefits of the adopted large-signal capacitance model.

As a final remark, it is worth highlighting that the validity of the large-signal $C_{eq}(\Delta V_{pp})$ relation derived in Section IV (cf. Fig. 12(c)) suggests that the realized full-ceramic DC-link capacitor assembly (i.e., sized according to the small-signal capacitance value) results in a $\approx 11\,\%$ higher worst-case DC-link voltage ripple with respect to the design target of $\Delta V_{dc,pp,max} = 10\,\% \cdot V_{dc} = 80\,\text{V}$. This further speaks to the importance of exploiting the large-signal $C_{eq}(\Delta V_{pp})$ relation during the DC-link design phase, since the small-signal capacitance value provided by the manufacturer may translate is significant undersizing of the DC-link capacitor, particularly for low $\Delta V_{dc,pp,max}$ targets.

VII. CONCLUSION

This paper has presented the comprehensive analysis, design and experimental assessment of a high power density full-ceramic DC-link capacitor for a 800 V 550 kVA 20 kHz electric vehicle (EV) drive inverter.

First, an overview of the most relevant capacitor technologies for inverter DC-link applications in automotive has been presented, including and comparing both film and ceramic technologies. In particular, the superior theoretical performance of PLZT ceramic capacitors in terms of volumetric/gravimetric capacitance and current densities have been highlighted in a preliminary performance comparison.

With the goal of providing a straightforward and generalized DC-link capacitor sizing procedure for three-phase inverters (and applicable to all kinds of voltage-source converters), analytical expressions of the DC-link RMS current and charge ripple stresses have been recalled and approximate capacitance sizing relations accounting for technology-specific frequency and temperature dependencies have been derived. Remarkably, the already prospected performance advantage offered by PLZT ceramic capacitors has been shown to rapidly and progressively widen for increasing values of switching frequency up to hundreds of kHz, suitable for future drive inverters with fast-switching semiconductor devices. Moreover, being the capacitance and current density ratios between film and PLZT ceramic technologies mostly independent of the selected voltage class, the identified performance benefits are applicable to all EV powertrain voltage levels (i.e., 200–1000 V).

To validate the underlying assumptions of the proposed sizing procedure and to gather additional information on the considered PLZT ceramic capacitor technology, a large-signal experimental characterization has been performed on a single capacitor sample. Other than validating the frequency dependence of the capacitor RMS current capability, this experimental characterization has allowed to obtain for the first

time the equivalent large-signal capacitance value as function of the amplitude of the excitation (i.e., the voltage ripple) and DC-bias voltage level, a crucial information that is not provided by the manufacturer.

The proposed DC-link sizing procedure has then been applied to the considered 550 kVA EV drive inverter and a prototype of a full-ceramic DC-link capacitor assembly has been realized, demonstrating 69 % (i.e., ≈ two thirds) lower volume and 29 % (i.e., ≈ one third) lower weight than an equivalent film-based solution.

Finally, the peak-to-peak voltage ripple performance of the designed DC-link capacitor has been experimentally assessed exploiting a 800 V 550 kVA EV drive inverter prototype operating at 20 kHz. The results have demonstrated excellent agreement between measured and predicted ripple values, successfully validating the non-linear relation between equivalent large-signal capacitance and amplitude of the excitation (i.e., charge/voltage ripple).

Overall, this work has practically demonstrated the well anticipated disruptive performance of PLZT ceramic capacitor technology in high-voltage high-power three-phase EV drive inverters. Remarkably, the authors believe that the increased switching frequency operation unlocked by modern wide bandgap semiconductor devices (i.e., SiC, GaN) and the integration of the capacitor assembly through state-of-the-art manufacturing and dielectric molding techniques may potentially lead to a further performance leap in DC-link (and drive inverter system) power density.

APPENDIX A
CAPACITOR RMS CURRENT SCALING

The RMS current capability of a capacitor is defined by different factors (e.g., physical size, ESR, number of paralleled units, operating frequency, temperature), which can affect the capacitor thermal dissipation capability, the generated losses, or both.

A simplified electrical equivalent circuit of a generic capacitor is illustrated in Fig. 22(a), which indicates that the capacitor power losses can be expressed as

$$P = R_{\mathrm{ESR}}(f,T)\, I_{\mathrm{RMS}}^2, \tag{10}$$

where $R_{\mathrm{ESR}}(f,T)$ is the frequency/temperature-dependent ESR and I_{RMS} is the RMS current flowing through the capacitor itself. For simplicity of the analysis, a sinusoidal current with frequency f is assumed.

The capacitor losses must be dissipated towards the ambient, according to the simplified steady-state thermal equivalent circuit in Fig. 22(b). The heat flow leads to a rise of the capacitor temperature T with respect to the ambient temperature T_{a}, expressed as

$$T - T_{\mathrm{a}} = P\, R_{\mathrm{th}}, \tag{11}$$

where R_{th} is the thermal resistance of the capacitor towards the ambient. Therefore, the RMS current capability of the capacitor is obtained from (10) and (11) as:

$$I_{\mathrm{RMS}} = \sqrt{\frac{T - T_{\mathrm{a}}}{R_{\mathrm{th}}\, R_{\mathrm{ESR}}(f,T)}}. \tag{12}$$

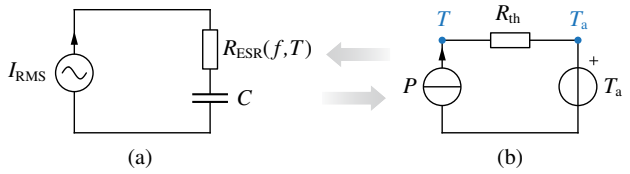


Fig. 22. Simplified (a) electrical equivalent circuit and (b) thermal equivalent circuit of a generic capacitor.

Assuming to parallel N capacitor units (i.e., $N = C/C^*$) and considering general frequency and temperature dependencies of the capacitor ESR (i.e., $R_{\mathrm{ESR}} \propto 1/f^{\alpha}$, $R_{\mathrm{ESR}} \propto 1/[1 + k(T - T_0)]^{\beta}$, cf. Section II), the following scaling laws are obtained:

$$\begin{cases} R_{\mathrm{ESR}}(f,T) = R^*_{\mathrm{ESR}}(f^*,T^*)\dfrac{C^*}{C}\left(\dfrac{f^*}{f}\right)^{\alpha}\left(\dfrac{1+k(T^*-T_0)}{1+k(T-T_0)}\right)^{\beta} \\ R_{\mathrm{th}} = R^*_{\mathrm{th}}\dfrac{C^*}{C} \end{cases} \tag{13}$$

where * indicates the values related to a single capacitor unit operating in the conditions specified in the manufacturer's datasheet, $\alpha \approx \beta \approx 0$ for film capacitors and $\alpha \approx \beta \approx 1$ for PLZT ceramic capacitors.

Therefore, a comprehensive scaling law for the capacitor RMS current capability is obtained from (12) and (13), as

$$I_{\mathrm{RMS}} = I^*_{\mathrm{RMS}}\frac{C}{C^*}\left(\frac{f}{f^*}\right)^{\alpha/2}\left(\frac{1+k(T-T_0)}{1+k(T^*-T_0)}\right)^{\beta/2}\sqrt{\frac{T-T_{\mathrm{a}}}{T^*-T^*_{\mathrm{a}}}}\,. \tag{14}$$

It is worth noting that in inverter DC-link applications the capacitor RMS current includes several frequency components located around integer multiples of the switching frequency f_{sw}. Nevertheless, a worst-case condition can be assumed by considering the complete RMS current stress applied at f_{sw} (i.e., the lowest frequency component).

REFERENCES

[1] I. Husain, B. Ozpineci, M. S. Islam, E. Gurpinar, G.-J. Su, W. Yu, S. Chowdhury, L. Xue, D. Rahman, and R. Sahu, "Electric Drive Technology Trends, Challenges, and Opportunities for Future Electric Vehicles," *Proceedings of the IEEE*, vol. 109, no. 6, pp. 1039–1059, Jun. 2021.

[2] T. M. Jahns and H. Dai, "The Past, Present, and Future of Power Electronics Integration Technology in Motor Drives," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 3, pp. 197–216, Sep. 2017.

[3] J. Reimers, L. Dorn-Gomba, C. Mak, and A. Emadi, "Automotive Traction Inverters: Current Status and Future Trends," *IEEE Transactions on Vehicular Technology*, vol. 68, no. 4, pp. 3337–3350, Apr. 2019.

[4] A. K. Morya, M. C. Gardner, B. Anvari, L. Liu, A. G. Yepes, J. Doval-Gandoy, and H. A. Toliyat, "Wide Bandgap Devices in AC Electric Drives: Opportunities and Challenges," *IEEE Transactions on Transportation Electrification*, vol. 5, no. 1, pp. 3–20, Mar. 2019.

[5] A. Poorfakhraei, M. Narimani, and A. Emadi, "A Review of Multilevel Inverter Topologies in Electric Vehicles: Current Status and Future Trends," *IEEE Open Journal of Power Electronics*, pp. 155–170, 2021.

[6] I. Aghabali, J. Bauman, P. J. Kollmeyer, Y. Wang, B. Bilgin, and A. Emadi, "800-V Electric Vehicle Powertrains: Review and Analysis of Benefits, Challenges, and Future Trends," *IEEE Transactions on Transportation Electrification*, vol. 7, no. 3, pp. 927–948, Sep. 2021.

[7] D. Gerada, A. Mebarki, N. L. Brown, C. Gerada, A. Cavagnino, and A. Boglietti, "High-Speed Electrical Machines: Technologies, Trends, and Developments," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 6, pp. 2946–2959, Jun. 2014.

[8] F. Savi, D. Barater, M. D. Nardo, M. Degano, C. Gerada, P. Wheeler, and G. Buticchi, "High-Speed Electric Drives: A Step Towards System Design," *IEEE Open Journal of the Industrial Electronics Society*, vol. 1, pp. 10–21, 2020.

[9] D. Cittanti, V. Mallemaci, F. Mandrile, S. Rubino, R. Bojoi, and A. Boglietti, "PWM-Induced Losses in Electrical Machines: An Impedance-Based Estimation Method," in *International Conference on Electrical Machines and Systems (ICEMS)*, Gyeongju, Korea, Oct. 2021, pp. 548–553.

[10] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[11] A. Bindra, "Wide-Bandgap-Based Power Devices: Reshaping the Power Electronics Landscape," *IEEE Power Electronics Magazine*, vol. 2, no. 1, pp. 42–47, Mar. 2015.

[12] J. W. Kolar *et al.*, "Application of WBG Power Devices in Future 3-Φ Variable Speed Drive Inverter Systems "How to Handle a Double-Edged Sword"," in *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2020, pp. 27.7.1–27.7.4.

[13] D. Cittanti, M. Guacci, S. Mirić, R. Bojoi, and J. W. Kolar, "Comparative Evaluation of 800V DC-Link Three-Phase Two/Three-Level SiC Inverter Concepts for Next-Generation Variable Speed Drives," in *International Conference on Electrical Machines and Systems (ICEMS)*, Hamamatsu, Japan, Nov. 2020, pp. 1699–1704.

[14] TDK, "CeraLink® Capacitors: Technical Guide," 2021.

[15] S. Chowdhury, E. Gurpinar, and B. Ozpineci, "High-Energy Density Capacitors for Electric Vehicle Traction Inverters," in *IEEE Transportation Electrification Conference Expo (ITEC)*, Jun. 2020, pp. 644–650.

[16] S. Chowdhury, E. Gurpinar, and B. Ozpineci, "Capacitor Technologies: Characterization, Selection, and Packaging for Next-Generation Power Electronics Applications," *IEEE Transactions on Transportation Electrification*, vol. 8, no. 2, pp. 2710–2720, Jun. 2022.

[17] D. Menzi, D. Bortis, G. Zulauf, M. Heller, and J. W. Kolar, "Novel iGSE-C Loss Modeling of X7R Ceramic Capacitors," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13 367–13 383, Dec. 2020.

[18] D. Menzi, M. Heller, and J. W. Kolar, "iGSE-Cx – a New Normalized Steinmetz Model for Class II Multilayer Ceramic Capacitors," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 138–144, 2021.

[19] S. Coday and R. C. N. Pilawa-Podgurski, "Characterization and Modeling of Ceramic Capacitor Losses Under Large Signal Operating Conditions," *IEEE Open Journal of Power Electronics*, vol. 4, pp. 24–33, 2023.

[20] D. Menzi, M. Heller, G. Kerridge, P. Marley, A. Ellmore, S. Ben-Yaakov, and J. W. Kolar, "iGSE-CD—An Electric-/Displacement-Field Related Steinmetz Model for Class II Multilayer Ceramic Capacitors Under Low-Frequency Large-Signal Excitation," *IEEE Open Journal of Power Electronics*, vol. 4, pp. 107–116, 2023.

[21] D. Menzi, S. Ben-Yaakov, G. Zulauf, and J. W. Kolar, "ESR Modelling of Class II MLCC Large-Signal-Excitation Losses," *IEEE Transactions on Power Electronics (Early Access)*, 2023.

[22] Y. Jiang, B. Hu, Y. Shen, X. Ren, S. Sandler, S. Hofmann, and T. Long, "Loss Characterization and Modeling of Class II Multilayer Ceramic Capacitors: A Synergic Material-Microstructure-Device Approach," *IEEE Transactions on Power Electronics (Early Access)*, 2023.

[23] M. Salcone and J. Bond, "Selecting Film Bus Link Capacitors for High Performance Inverter Applications," in *IEEE International Electric Machines and Drives Conference (IEMDC)*, May 2009, pp. 1692–1699.

[24] H. Wen, W. Xiao, X. Wen, and P. Armstrong, "Analysis and Evaluation of DC-Link Capacitors for High-Power-Density Electric Vehicle Drive Systems," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 7, pp. 2950–2964, Sep. 2012.

[25] M. Uğur and O. Keysan, "DC Link Capacitor Optimization for Integrated Modular Motor Drives," in *IEEE International Symposium on Industrial Electronics (ISIE)*, Jun. 2017, pp. 263–270.

[26] R. Alizadeh, M. Schupbach, T. Adamson, J. C. Balda, Y. Zhao, S. Long, K. Jung, C. R. Kharangate, M. Asheghi, and K. E. Goodson, "Busbar Design for Distributed DC-Link Capacitor Banks for Traction Applications," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 4810–4815.

[27] D. Cittanti, F. Stella, E. Vico, C. Liu, J. Shen, G. Xiu, and R. Bojoi, "Analysis and Design of a High Power Density Full-Ceramic 900 V DC-Link Capacitor for a 550 kVA Electric Vehicle Drive Inverter," in *International Power Electronics Conference (IPEC-ECCE Asia)*, May 2022, pp. 1144–1151.

[28] J. Schnack, S. Brückner, H. Süncksen, U. Schümann, and R. Mallwitz, "Analysis and Optimization of Electrolytic Capacitor Technology for High-Frequency Integrated Inverter," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 11, no. 6, pp. 999–1011, Jun. 2021.

[29] TDK, "Film Capacitors: General Technical Information," 2018.

[30] G. F. Engel, "Design and Materials of Antiferroelectric Capacitors for High Density Power Electronic Applications," in *International Conference on Integrated Power Electronics Systems (CIPS)*, Mar. 2016.

[31] S. Schefler, M. Puff, M. Koini, and S. Weber, "Modelling an Anti-Ferroelectric Ceramic Capacitor for Time- and Frequency-Domain Simulations of Power Systems," in *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM)*, May 2016.

[32] D. Neumayr, D. Bortis, J. W. Kolar, M. Koini, and J. Konrad, "Comprehensive Large-Signal Performance Analysis of Ceramic Capacitors for Power Pulsation Buffers," in *IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2016.

[33] EPCOS, "PCC for Infineon HybridPack Drive (HP Drive)," 2016.

[34] TDK, "CeraLink® Flex Assembly (FA) Series," 2019.

[35] J. Kolar, H. Ertl, and F. C. Zach, "Calculation of the Passive and Active Component Stress of Three-Phase PWM Converter Systems with High Pulse Rate," in *European Conference on Power Electronics and Applications (EPE - ECCE Europe)*, vol. 3, Aachen, Germany, Oct. 1989, pp. 1303–1311.

[36] M. Vujacic, M. Hammami, M. Srndovic, and G. Grandi, "Analysis of DC-Link Voltage Switching Ripple in Three-Phase PWM Inverters," *Energies*, vol. 11, no. 2, p. 471, Feb. 2018.

[37] A. Hava, R. Kerkman, and T. Lipo, "Simple Analytical and Graphical Methods for Carrier-Based PWM-VSI Drives," *IEEE Transactions on Power Electronics*, vol. 14, no. 1, pp. 49–61, Jan. 1999.

[38] TDK, "CeraLink® Low Profile (LP) Series," 2019.

[39] F. Stella, E. Vico, D. Cittanti, C. Liu, J. Shen, and R. Bojoi, "Design and Testing of an Automotive Compliant 800V 550 kVA SiC Traction Inverter with Full-Ceramic DC-Link and EMI Filter," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2022.