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***Abstract*—Over the years, several clock and data recovery architectures have been proposed for wireless Amplitude Shift Keying (ASK) transmitted signals. State-of-the-art architectures mainly rely on synchronous phase-locked loop circuits or self-sampling systems, both resulting in large area consumption. This work presents a novel CMOS architecture for Clock and Data Recovery (CDR) in miniaturised and wirelessly powered implants. The proposed CDR architecture works at $433.92\ MHz$ and includes: an ASK-demodulator, an on-chip oscillator, a power-on-reset, a control and a recovering block operating in feedback-loop. The ASK-demodulator works for a data rate as high as $6\ Mbps$ and a modulation index in the range of $9-30\%$. A novel communication protocol is presented for a separated clock and data transmission. The entire CDR architecture occupies $17 \times 89\ \mu m^2$ and consumes $15.01\ \mu W$ while operating with a clock rate of $6\ Mbps$.**

***Index Terms*—ASK-Demodulator, CMOS, Wireless Transmission, Clock Data Recovery, Low-Power, Low-Area, High Data Rate.**

I. Introduction

Simultaneous wireless information and power transfer is a key technology for miniaturised implants. Among the others, inductive coupling is commonly used to transmit both power and data to miniaturised implants (i.e. with a volume smaller than $1\ mm^3$) at penetration depths of $10-15\ mm$ [1]. Amplitude Shift Keying (ASK) modulation is usually adopted in miniaturised and inductively powered systems for its circuital simplicity, low area and small power consumption [2]. Miniaturised and low-power Clock and Data Recovery (CDR) systems are therefore needed. The state-of-the-art proposes different ASK-demodulators operating in: voltage mode [3], current mode [4], and mixed mode [5]. The common ASK-demodulator implementation includes a rectifier, an envelope detector and a digital shaper. Clock recovery is usually performed: i) synchronously and in parallel to the demodulation or ii) asynchronously through an on-chip oscillator synchronised with the demodulated data.

Structures using R-C elements have been exploited [6], [3], resulting in large area consumption. ASK-demodulators with embedded clock recovery systems have been proposed exploiting the self-sampling [7] and the event-based related mechanism [8], also resulting in large area consumption. Pulse Position Modulation (PPM) combined with the ASK has been exploited [9], with the drawback of a recovered clock with a duty cycle different from 50%. Alternatively, the clock is recovered using a Phase-Locked Loop (PLL) or Delay-Locked Loop (DLL) [10], resulting in large area and high power consumption. Alternatively, encoding techniques, such as Manchester encoding [11], can be used with the general payload of doubling the required bandwidth, reducing the data rate and increasing the circuit complexity and thus, the area consumption.

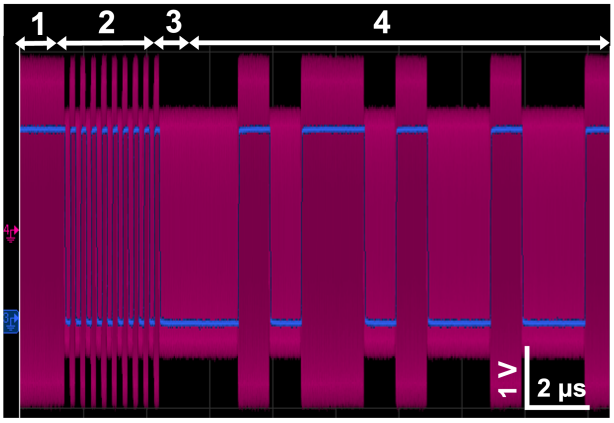

Figure 1: Measurements of the fabricated transmitter showing the digital data (blue) and the ASK-modulated signal (pink). In white the four phases of the communication protocol: phase 1 (power-on preamble), phase 2 (synchronisation preamble), phase 3 (data preamble) and phase 4 (data transmission).

In this paper we propose a novel CDR system for ASK modulated signal. The system is extremely versatile and suitable for wireless, miniaturised and low-power implants. The architecture is R-C-less and is capable of synchronously recover the clock without the need of complex PLL/DLL circuits nor encoding techniques.

II. Materials and Methods

The external Radio-Frequency (RF) ASK transmitter was designed as in [12] and fabricated in $0.36\ mm$-thick PCB. Measurements of the ASK-modulated transmitted signal (Fig. 1) were conducted using a DC power supply (Keysight E3646A), an arbitrary waveform generator (Keysight 33500B)

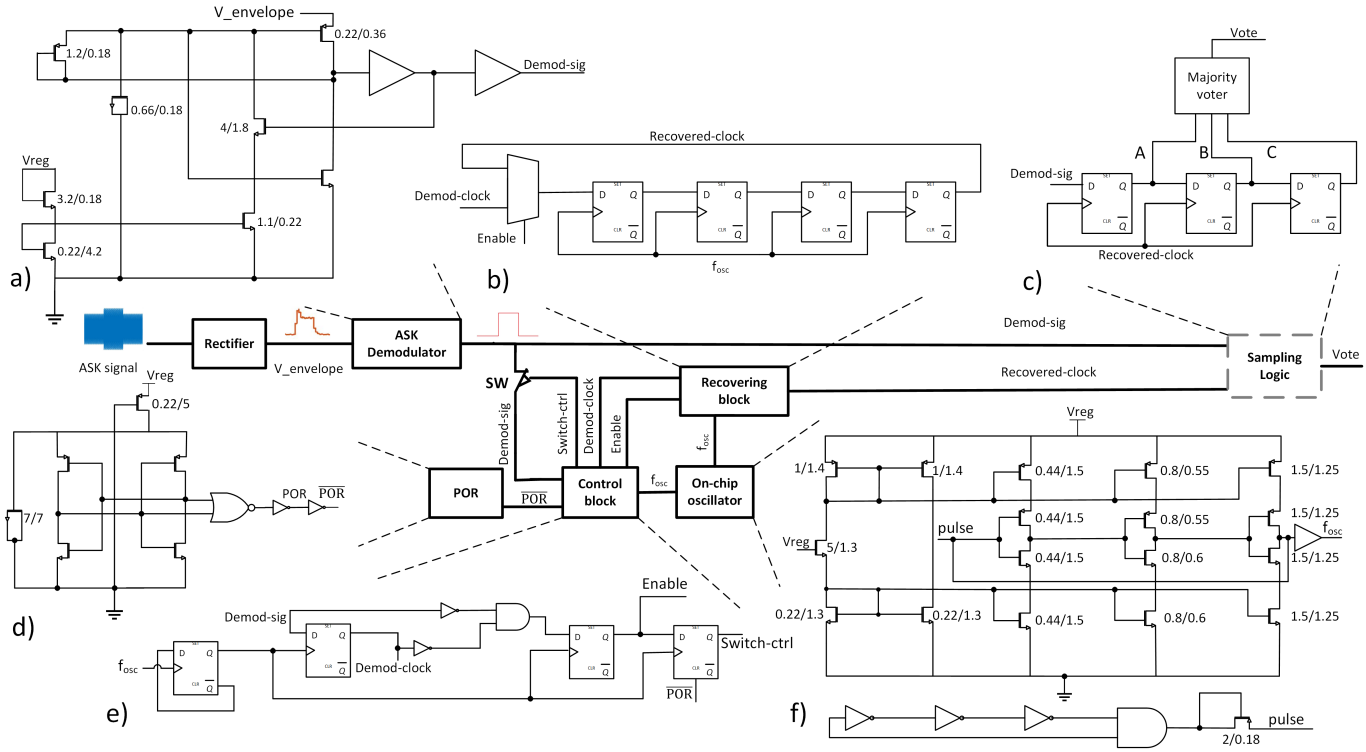

Figure 2: Blocks and CMOS circuitry of the CDR architecture including: (a) the ASK demodulator, (b) the recovering block, (d) the POR, (e) the control block and (f) the on-chip oscillator. (c) The dashed sampling block is used for the BER analysis.

and an oscilloscope (Keysight 4104A). CMOS circuits have been simulated at schematic and post-layout levels using Cadence IC6.1.7 and TSMC 180-nm libraries. DC, transient and noise simulations have been conducted. Post-layout simulations included parasitic resistances, capacitances and coupling-capacitances (R-C-CC) extracted via Calibre. Dedicated Matlab scripts have been used to generate the waveforms to simulate the phase robustness of the recovered clock and the Bit Error Rate (BER). Circuits have been optimised to minimise area consumption. Minimum size transistors have been used if not differently specified.

III. System Design

Fig. 1 shows the typical measurements of the fabricated external base station for wireless power and data transmission [12]. A digital wave (blue) modulates the ASK signal (pink). The latter is generated with a RF of 433.92 MHz, an output power of 30 dBm, and a Modulation Index (MI) of 15%. The ASK signal (attenuated during the transmission to the implant) is the typical input of wirelessly powered CMOS receivers. The novel CMOS CDR system operates with a specific communication protocol, which is highlighted in white in Fig. 1. Phase 1 (power-on preamble) is needed for system power-on (i.e. rectifier stabilisation, which is not the aim of this paper). Phase 2 (synchronisation preamble) is dedicated to the clock recovery: 18 bits are transmitted at the Clock Rate (CR) of 6 $Mbps$. In phase 3 (data preamble) at least two bits at low logical state are transmitted to switch the designed control logic in the off-state. In phase 4 (data transmission) data are transmitted with a Data Rate (DR) of 1 $Mbps$. The CDR architecture is reported in Fig. 2 including: (a) the ASK-demodulator; (f) the on-chip oscillator; (e) the control block; (b) the recovering block and (d) the Power On Reset (POR).

A. ASK Demodulator

After system power-on and signal rectification (phase 1), the same ASK-demodulator operates both for the clock recovery at CR (phase 2) and the data recovery at DR (phase 4). Fig. 2-a shows its structure at transistor level, which is adapted from [13]. It is composed by: i) the envelope detector; ii) the digital shaper and iii) the buffering stage. The designed circuit works with a regulated supply voltage $V_{reg} = 1.1\ V$. It is optimised minimising power and area consumption together with maximising the Demodulator Data Rate (DDR). A maximum DDR of 6 $Mbps$ is obtained, which is used in phase 2 for the clock recovery at CR. The ASK-demodulator works for MI in the range 9-30%. Noise analysis is performed in the range $100 - 1000\ MHz$ with a step of 10 MHz. The simulated Signal-to-Noise Ratio (SNR) is 73.15 dB.

B. On-Chip Oscillator

The on-chip oscillator is the timer used in the control and recovering blocks, for which both the clock at CR and the data at DR are treated as data signals. The minimum frequency f_{osc} of the on-chip oscillator is set accordingly to the Nyquist criterion. In particular, $f_{osc} \geq 2 \cdot CR$. The designed oscillator

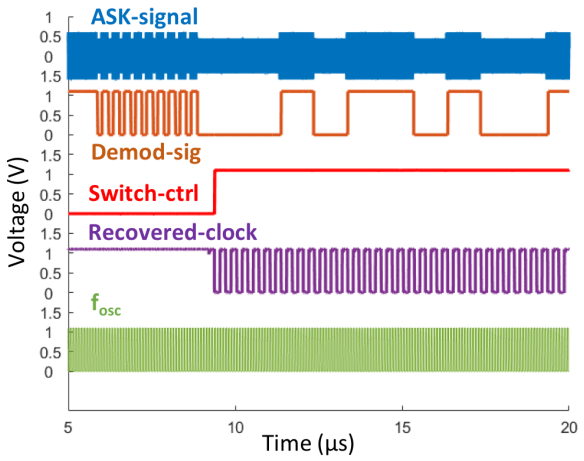

Figure 3: Post-layout simulation of the entire CDR system.

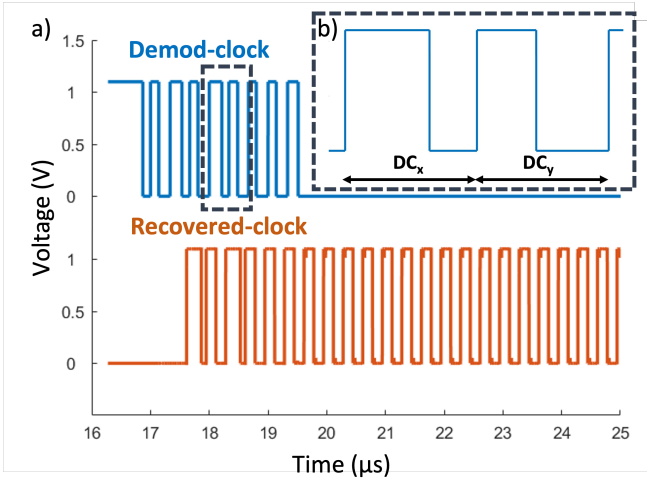

Figure 4: a) Phase robustness analysis of the CDR system and b) $Demod-clock$ detail of two periods with random DC.

is a capacitor-less three stages voltage-controlled current-starved ring oscillator, as in Fig. 2-f. The oscillator wakes up after 142 ns with a self-start logic circuit generating the $pulse$ signal. An $f_{osc} = 16\ MHz$ is obtained at V_{reg} of supply after 1 μs of stabilisation. The oscillator presents good noise performances with a phase noise of $-101.9\ dBc/Hz$. The circuit is extremely miniaturised and low-power, occupying $5.95 \times 37.48\ \mu m^2$ and consuming 2.81 μW.

C. Control Block

When at least two consecutive zeros are detected (phase 3), the control block triggers the $Switch-ctrl$ signal that permanently turnes off the PMOS-switch SW, as in Fig. 2. The control block is made of 3 logic gates and 3 D-Flip Flop (D-FF) triggered at $f_{osc}/2$. The latter is generated by the first D-FF. $Switch-ctrl$ is directly connected to the SW (Fig. 2-e) and it is maintained high thanks to the signal generated by the POR circuit. The latter is a miniaturised version of [14] (Fig. 2-d). In other words, the control block operates on the switch. When the switch is closed the clock is sampled at f_{osc} in a circular shifting register. When the switch is open the system is ready to receive data at DR (phase 4).

D. Recovering Block

The recovering block is used to permanently reconstruct the clock starting from the 9 periods which are wirelessly transmitted in phase 2 at CR. It is composed by a multiplexer and a shifting register made by a chain of 4 D-FF triggered by the on-chip oscillator at f_{osc} (Fig. 2-b). The multiplexer selector $Enable$ is triggered by the control block. When $Enable = 0$ the demodulated clock of phase 2 coming from the control block ($Demod-clock$) is activated by the multiplexer and passes through the shifting register. When $Enable = 1$ (phase 3), the D-FF chain self oscillates obtaining a stable and permanently recovered clock at CR ($Recovered-clock$).

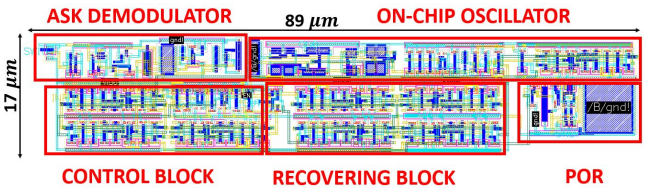

Figure 5: Final layout of the CDR system.

E. Sampling block

The sampling block is used to evaluate the BER of the proposed CDR system. It is composed by a shifting register made by three D-FFs and a three-bits majority voter (Fig. 2-c). The latter generates the $Vote$ signal representing the demodulated transmitted data at DR sampled by the recovered transmitted clock at CR.

IV. Results and Discussion

Fig. 3 shows the post-layout simulation of the proposed CDR system. The designed ASK-demodulator efficiently demodulates the clock at CR and the data at DR ($Demod-sig$ in orange) starting from the $ASK-signal$ (blue). The on-chip oscillator (green) correctly activate the control block which triggers $Switch-ctrl$ (red). The recovering block is capable to permanently recover the clock at CR ($Recovered-clock$ in purple).

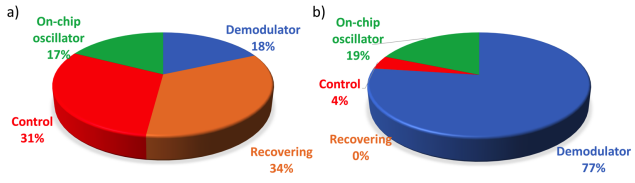

Figure 6: a) Area and b) power contribution of the CDR blocks after layout.

Table I: State-of-the-art comparison.

Parameter	[15]	[16]	[17]	[10]	[18]	[19]	**This work**
Modulation	ASK-PPM	ASK-PWM	ASK-PPM	ASK	FSK	FSK	**ASK**
Method	Charge pump	Monostable circuit	Charge pump	PLL	Digital Logic	Digital logic	**Adaptable transmission**
Technology (μm)	0.25	0.18	0.25	0.18	0.13	0.13	**0.18**
f_c (MHz)	1.5	10	1	13.56	-	10	**433.92**
Data Rate ($Mbps$)	0.0455	0.5	0.01976	0.106	0.1	4	**6**
Area (μm^2)	-	-	3.19 x 10^7	273600	1.7 x 10^7	2.9 x 10^7	**1513**
Power (μW)	31	29.52	100	900	0.05	380	**15.01**
FOM_1 [20][a]	-	-	6.33 x 10^{-6}	4.41 x 10^{-4}	0.118	3.63 x 10^{-4}	**255.75**
FOM_2 [12][b]	0.111	0.292	0.073	0.094	-	1.17	**0.436**

[a] $FOM_1 = \frac{Datarate}{Power \cdot Area}\left(\frac{kbit/s}{mW\mu m^2}\right)$; [b] $FOM_2 = \left(\frac{Datarate^2}{f_c}\right)^{1/3}\left(\frac{Mbps^2}{MHz}\right)^{1/3}$

The phase robustness analysis of the recovered clock is performed and the results are shown in Fig. 4-a. A clock with a random Duty Cycle (DC) is generated at CR and treated by the CDR system ($Demod-clock$ in blue). In particular, the DC is randomly generated for each period i according to (1):

$$DC_i = DC_{nom} \cdot (1 - \beta_i)(\%) \quad (1)$$

where DC_{nom} = 50% and $\beta \in$ [-1,1]. Fig. 4-b highlights two periods of $Demod-clock$ in which $\beta_x = -0.32$ ($DC_x = 66\%$) and $\beta_y = 0.32$ ($DC_y = 34\%$). When $Switch-ctrl = 1$ (phase 3) the CDR structure perfectly reconstructs the clock signal at CR with a DC of 50% ($Recovered-clock$ in orange of Fig. 4-a). The CDR system is robust in recovering clock with random DC ranging from 34% to 66%.

Moreover, BER analysis is performed. The latter is the ratio between the number of incorrect bits with respect to the total bits transmitted. For the analysis, 1000 random bit are transmitted in phase 4. The sampling block output ($Vote$ of Fig. 2-c) is compared bit-by-bit with the transmitted ASK signal ($ASK-signal$) obtaining a BER $= 3 \cdot 10^{-3}$.

Fig. 5 shows the final layout of the entire CDR structure, which occupies a total area of 17×89 μm^2 and consumes 15.01 μW.

Fig. 6-a,b show respectively the area and power contribution of each block of the proposed CDR system. As expected, the digital circuits of the control (red) and recovering blocks (orange), consume a negligible power. On the other hand, they occupy the majority of the silicon area (i.e., 65% of the total area). On the contrary, the ASK-demodulator occupies the 18% of the total area and consumes the 77% of the total power, since high power is needed to transform an analogue signal to a digital one.

Table I compares the novel proposed CDR system with the state-of-the-art. FOM_1 [20] takes into account power consumption, area, and data rate. The proposed CDR system outperforms the state-of-the-art according to FOM_1. Since the maximum data rate is usually higher for higher carrier frequencies f_c (thus, favouring our work), a second figure of merit is considered. FOM_2 [12] considers the maximum data rate and f_c. In general, the proposed solution outperforms the others in terms of area consumption, which is the major goal of this work. Moreover, our CDR system is much more performing considering both FOM_1 and FOM_2. Improvements in terms of power consumption can be made by designing a new demodulator. Moreover, the proposed solution is extremely versatile, regardless the demodulator performances. The same architecture can be used at higher CR and DR (respecting $DR = CR/6$) by increasing the maximum DDR. On the other side, due to the digital nature of the proposed solution, area can be easily minimised by reducing the technology node [21], [22].

V. Conclusions

This paper proposes a novel clock and data recovery architecture for ASK-demodulators in wireless RF applications. The entire system has been designed, simulated and optimised with the gaze turned toward minimising area consumption. A novel communication protocol is presented in which the clock is completely recovered during the first phase of the communication. The external transmitter is fabricated to meet the requirements of the novel CMOS architecture.

The system is extremely powerful and versatile, taking advantage of an adaptable approach based on a separated clock and data transmission. The architecture is stable with respect to phase variation of the clock and bit error rate. The entire circuit operates with a maximum demodulator data rate of 6 $Mbps$ and a variable modulation index in the range $9-30$ %. It consumes 15.01 μW and it occupies 17×89 μm^2. A detailed comparison is performed with different figure-of-merits showing better performances among the current state-of-the-art.

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