A 880 nW, 100 kS/s, 13 bit Differential Relaxation-DAC in 180 nm

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Roberto Rubino[1], Francesco Musolino[1], Pedro Toledo[1], Yong Chen[2], Anna Richelli[3], Paolo Crovetti[1]
[1]*Dept. Electronics and Telecommunication (DET), Politecnico di Torino*, Torino, Italy
[2]*State-Key Laboratory of Analog and Mixed-Signal VLSI and IME/ECE-FST, University of Macau*, Macao, China
[3]*Dept. of Information Engineering, University of Brescia*, Brescia, Italy
email: roberto_rubino@polito.it

***Abstract*—This paper presents a digital intensive, compact and energy efficient 13-bit, 100-kS/s Differential Relaxation Digital to Analog converter (Diff-ReDAC) in 180 nm CMOS. The Diff-ReDAC is able to operate in a supply voltage range from 0.45 V to 1 V having power consumption ranging from 420 nW to 2,650 nW. It has an area footprint of only 7,800 µm^2 while achieving, at 0.6 V a maximum INL (DNL) of 1.07 LSB (0.96 LSB) , 77.81 dB (77.52 dB) of SFDR (THD) and 65.82 dB SINAD, resulting in 10.64 ENOB. Its low power dissipation of 880 nW results in extremely competitive energy efficiency (area-normalzed energy efficiency) figures of merits FOM (FOM$_A$) of 172 dB (178 dB).**

***Index Terms*—D/A converter (DAC), Relaxation D/A Converter (ReDAC), Ultra-low Power, Ultra-low Area, digital intensive, consumer data converter.**

I. Introduction

Analog and mixed-signal (AMS) integrated circuit (IC) design has become increasingly challenging in relation to CMOS technology scaling, reduction of supply voltages and dynamic ranges, along with increasingly stringent power and area constraints of novel Internet of Things (IoT) applications [1]. In this context, digital-based AMS IC design techniques have become more and more popular [3] to overcome the limitation of traditional analog design in advanced technology nodes and to meet the power, supply voltage and area requirements of IoT applications, and also to reduce design time taking advantage of the digital automated flow.

Digital-to-Analog Converters (DACs) play a fundamental role in different applications, including sensor readout, calibration, audio processing [2] and reference generation in analog interfaces for the IoT [1], which require compact, low-power integrated DACs operating at supply voltages below 1 V, low distortion, low power consumption and bandwidth in the sub-MHz range. Aiming to Relaxation Digital-to-Analog converter (ReDAC) exploits the digital-based design approach has been presented in its FPGA implementation [6] and here presented for the first time in its differential-output silicon prototype in 180nm CMOS.

The paper is structured as follows: the ReDAC operation is reviewed in Section II, while the new Differential ReDAC (Diff-ReDAC) and its 180 nm implementation are introduced in Section III. Section IV describes the test chip architecture and the Diff-ReDAC self-calibration. The experimental test results are presented in Section V, followed by a comparison with the state of the art and conclusions in Section VI.

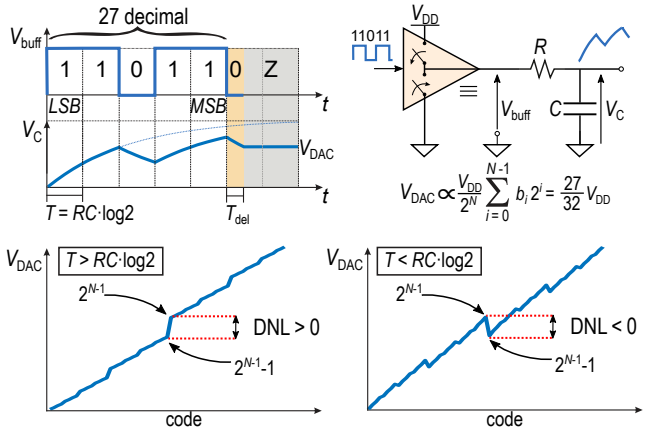

Fig. 1. ReDAC operating principle and clock period (T) related nonlinearity.

II. Relaxation DAC

A ReDAC [5]–[8] converts a N-bit digital input code $(b_{N-1}...b_0)$ into a voltage proportional to its binary value

$$n = \sum_{i=0}^{N-1} b_i 2^i, \tag{1}$$

exploiting the step response of a first-order RC network.

Fig.1 illustrates the basic principle of a ReDAC: a three-state buffer drives the RC network for a period $t \in [0, NT]$ with a stream of rectangular voltage pulses having constant width T and amplitude $V_{\rm DD} b_i$, starting from the LSB. After the last bit (i.e., the MSB) has been processed, the three state buffer is operated in the high impedance state to hold the capacitor voltage, which represents the result of the conversion (hold phase).

If a zero initial capacitor voltage is assumed, indeed, the voltage $v_{\rm C}(NT)$ at the end of the conversion is [5]:

$$v_{\rm C}(NT) = V_{\rm DD}\left(1 - e^{-\frac{T}{\tau}}\right) \sum_{i=0}^{N-1} b_i e^{-\frac{(N-1-i)T}{\tau}}. \tag{2}$$

where $\tau = RC$ is the time constant and if

$$e^{-\frac{T}{\tau}} = \frac{1}{2} \quad \Longrightarrow \quad T = \tau \log 2 = T^* \tag{3}$$

the capacitor voltage at $t = NT^*$ is

$$v_{\rm C}(NT^*) = \frac{V_{\rm DD}}{2^N} \sum_{i=0}^{N-1} b_i 2^i = \frac{n}{2^N} V_{\rm DD} = V_{\rm DAC}(n) \tag{4}$$

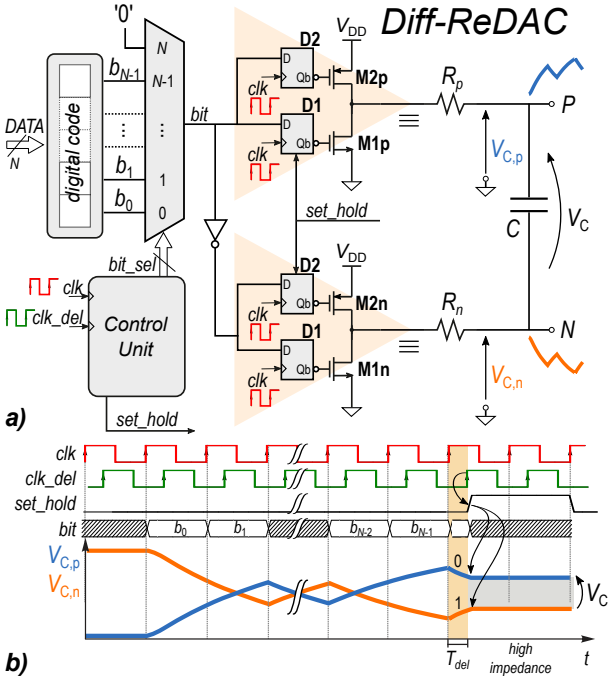

Fig. 2. Integrated Diff-ReDAC architecture and its timing diagram.

and it is proportional to the digital code in (1).

A deviation $\Delta T = T - T^*$ of the ReDAC clock T from its nominal value T^* in (3) results in a maximum differential nonlinearity (DNL) error between codes 2^{N-1} and $2^{N-1}-1$ (see Fig.1), which is monotonically increasing with ΔT [6]. As a consequence, if T is tuned so that to enforce

$$\Delta V_{\mathrm{DAC}} = V_{\mathrm{DAC}}(2^{N-1}) - V_{\mathrm{DAC}}(2^{N-1}-1) = 0 \qquad (5)$$

a 1 LSB maximum DNL across the whole swing can be guaranteed. This feature has been exploited in [6]–[8] for digital self-calibration. Any deviations from the ideal first-order behavior of the RC network due to parasitics also result in ReDAC nonlinearity, which can easily be suppressed by driving the three-state buffer low for a small period $T_{\mathrm{del}} \ll \tau$ before the hold phase, as detailed in [6].

Since the ReDAC does not rely on matched components, both area and power can be minimized by reducing the RC capacitance close to the thermal noise limit [5], provided that the clock period is properly calibrated to meet (3). Moreover, thanks to its simple and robust operating principle, a ReDAC can easily be designed in a standard-cell digital flow at very low effort [6].

III. Differential Integrated ReDAC

In this paper, the first silicon demonstration of a 13-bit 100 kS/s Differential ReDAC (Diff-ReDAC) in 180 nm is presented. The Diff-ReDAC is based on the architecture in Fig. 2a, which entails an output stage made up of two three-state buffers ($\mathrm{Buff_p}$ and $\mathrm{Buff_n}$) that drive a floating RC network ($R_{\mathrm{p}} = R_{\mathrm{n}} = R/2$ and C).

The buffers $\mathrm{Buff_p}$ ($\mathrm{Buff_n}$) are driven with the input code bitstream $(b_{N-1}...b_0)$ (the complemented bitstream $(\bar{b}_{N-1}...\bar{b}_0)$) by the flip flops $\mathrm{D1_p}$, $\mathrm{D2_p}$ ($\mathrm{D1_n}$, $\mathrm{D2_n}$) fed by

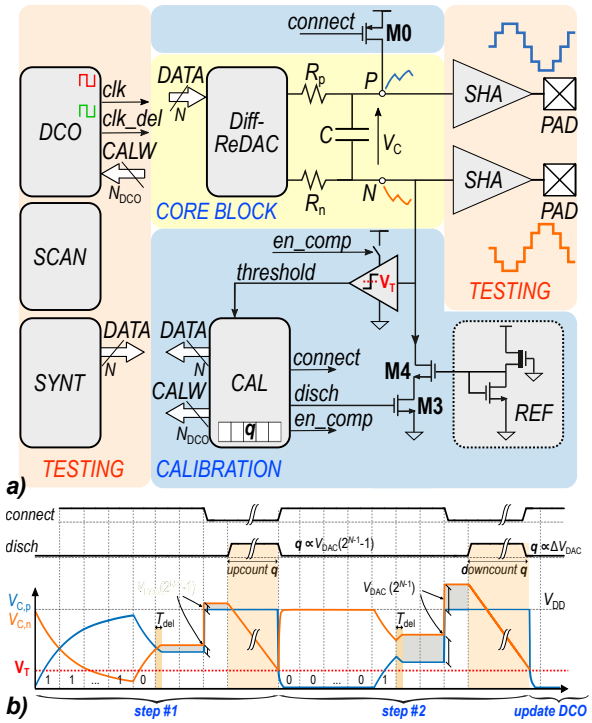

Fig. 3. Chip-level architecture (a), CAL timing diagram (b).

a digital multiplexer (MUX) to serialize the input code. After the MSB is processed, the DAC output $V_{\mathrm{DAC}} = v_{C,\mathrm{p}}(NT^*) - v_{C,\mathrm{n}}(NT^*) = v_C(NT^*)$ is

$$V_{\mathrm{DAC}} = 2\frac{n}{2^N}V_{\mathrm{DD}} - V_{\mathrm{DD}}. \qquad (6)$$

and is hold in the capacitor operating $\mathrm{Buff_p}$ ($\mathrm{Buff_n}$) in high impedance.

The parasitic-induced error suppression proposed in [6] is extended here from the single ended architecture to the Diff-ReDAC. For this purpose, the buffers $\mathrm{Buff_p}$ ($\mathrm{Buff_n}$) are driven to logic 0 (logic 1) at the end of conversion for a sub-clock-cycle time interval T_{del} before being put in high impedance. In practice, this is achieved by asynchronously resetting (setting) $\mathrm{D1_p}$ ($\mathrm{D2_n}$) at the end of T_{del} by a delayed clock signal clk_del.

The converter is designed according to the procedure in [9] choosing a Metal-insulator-Metal (MiM) capacitor $C = 2.6\,\mathrm{pF}$ close to the limit imposed by the $(\kappa T/C)$ noise for 13 bit resolution, while the two high-resistivity poly resistors $R_{\mathrm{p}} = R_{\mathrm{n}} = R/2 = 180\,k\Omega$ are designed to meet (3) at the target sample rate $T_{\mathrm{conv}}^{-1} = 100\,\mathrm{kS/s}$ considering that

$$T_{\mathrm{conv}} = (N+2)T^* = (N+2)\tau \log 2, \qquad (7)$$

in which $N = 13\,\mathrm{bit}$ clock periods are needed for conversion and two more cycles for the parasitics-induced error suppression and for the hold phase [6]. The transistors $\mathrm{M1_p}$ $\mathrm{M2_p}$, $\mathrm{M1_n}$ $\mathrm{M2_n}$ are sized to keep the buffer loading effect on DNL below 1 LSB, and have equal aspect ratios of $5\,\mu\mathrm{m}/0.18\,\mu\mathrm{m}$.

IV. Chip-level Architecture

The Diff-ReDAC test chip architecture is shown in Fig.3. It includes the ReDAC core, a Sample-and-Hold Amplifier

(SHA), the digital Calibration (CAL) unit, a Digitally Controlled Oscillator (DCO), a Direct Digital Synthesizer (SYNT) and a Scanchain (SCAN) to configure the digital blocks.

The DCO is based on a tunable relaxation oscillator with binary weighted tuning capacitors and it provides the clock clk for all the integrated blocks. Its frequency is tuned by the CAL unit during calibration to enforce (3); the DCO also provides the delayed clock clk_del, needed to implement the parasitics error suppression as in [6], by means of a digital delay line.

A. Calibration

The CAL block is designed to enforce (3) as needed to achieve linear operation, tuning the clock period of the DCO depending on the sign of $\Delta V_{\mathrm{DAC}} = V_{\mathrm{DAC}}(2^{N-1}) - V_{\mathrm{DAC}}(2^{N-1}-1)$ stored in the register q.

The aforementioned sign is determined by comparing the constant-current discharge times of the ReDAC capacitor after the conversion of $V_{\mathrm{DAC}}(2^{N-1}-1)$ and $V_{\mathrm{DAC}}(2^{N-1})$. To measure the discharge times, the node P is connected to V_{DD} at the end of each CAL conversions by the switch M0, while the terminal N is left in high impedance. Next, the discharge network consisting of a current sink M4 is enabled by the switch M3, discharging the node N. The capacitor discharge time from $V_{\mathrm{DD}} - V_{\mathrm{DAC}}(2^{N-1}-1)$ ($V_{\mathrm{DD}} - V_{\mathrm{DAC}}(2^{N-1})$) down to the comparator threshold $\mathrm{V_T}$ are digitized by means of the binary UP/DOWN counter q operated in UP (DOWN) mode during the discharge times.

The CAL procedure, illustrated in Fig.3b, operates as follows: at reset, the $N_{\mathrm{DCO}} = 12\,\mathrm{bit}$ calibration word $CALW$ is set to $2^{N_{\mathrm{DCO}}-1}$ to make the DCO oscillate at its center frequency. In the first calibration step $V_{\mathrm{DAC}}(2^{N-1}-1)$ is converted, M0 activated and the capacitor is discharged trough M4, while the counter q is incremented until the capacitor voltage $v_{C,\mathrm{n}}$ crosses $\mathrm{V_T}$. In the second calibration step $V_{\mathrm{DAC}}(2^{N-1})$ is converted, M0 activated and the capacitor is discharged trough M4, while the counter q is decremented until the capacitor voltage $v_{C,\mathrm{n}}$ crosses $\mathrm{V_T}$. The sign of the counter word q at the end of one calibration cycle is equal to the sign of ΔV_{DAC} and ΔT, neglecting the counter quantization error and the comparator noise. If $q = 0$, (3) is met within 1LSB and the calibration is terminated. On the other hand, if $q \neq 0$ the calibration word $CALW \propto T$ is dichotomously decreased (increased) as by a successive-approximation-register (SAR) logic if $q > 0$ ($q < 0$), and a new calibration cycle begins.

V. Experimental Results and Comparison

The ReDAC test setup and the micrograph of the 180 nm ReDAC test-chip are shown in Fig.4(a) and Fig.4(b) respectively. The ReDAC area is only $7,800\,\mu\mathrm{m}^2$. The chip is operated via scanchain trough an FPGA. The output pads of the SHAs are probed and acquired by the two channels of a Picoscope®4262 16bit oscilloscope connectd through a BNC connector to the Diff-ReDAC test PCB.

A. Experimental Results

Static characterization in Fig. 5a under 0.6 V ReDAC supply reveals a maximum (rms) INL of 1.07 LSB (0.28 LSB) and

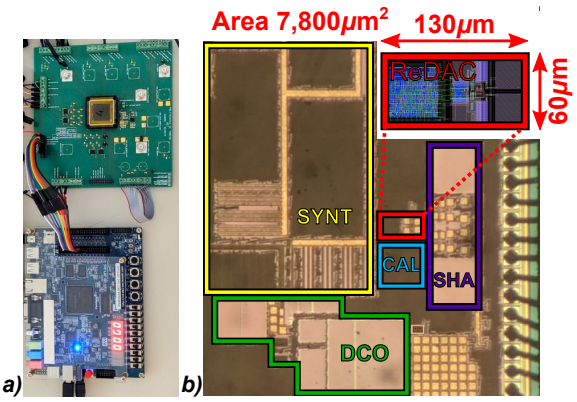

Fig. 4. Measurement setup (a) and chip micrograph (b).

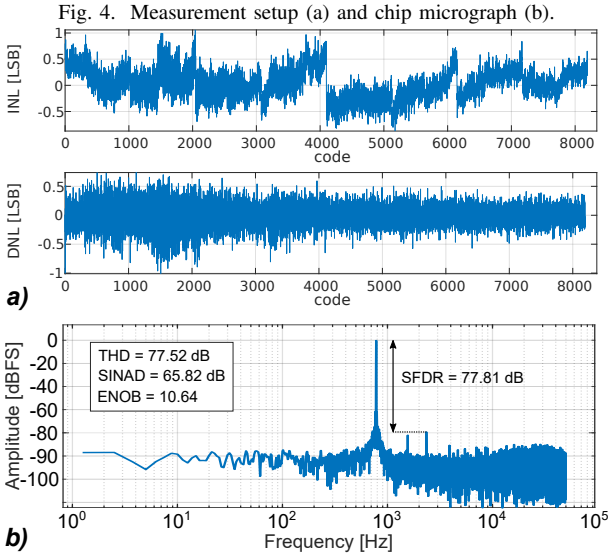

Fig. 5. Diff-ReDAC static linearity (a) and 0.8 kHz, 90% swing spectrum (b).

a maximum (rms) DNL of 0.96 LSB (0.20 LSB). Single-frequency dynamic characterization under 0.8 kHz, 90% swing sine reveal a SFDR (THD) of 77.81 dB (77.52 dB) and a 65.82 dB SINAD, resulting in an effective resolution of 10.64 ENOB. Based on Fig. 6a and Fig. 6b, the Diff-ReDAC shows consistent performance up to the Nyquist rate and over the whole input swing.

Dynamic performance/power evaluation at 1 kHz, 90 % swing sine under different supply voltages (from 0.45 V to 1 V) reveal an ENOB larger than 10 bits on most of the supply range with a power dissipation ranging from 420 nW to 2,650 nW (880 nW under 0.6 V nominal supply).

B. Performance Comparison

Compared to silicon-proven DACs reported in Tab. I, the Diff-ReDAC achieves the second smallest absolute area (6.1× more than [4], fabricated in a finer node) and the second smallest normalised area (2.2× the area of [12], which has comparable sample rate and 2.6 less ENOB) and is 19× smaller than [11]. Moreover, our Diff-ReDAC can operate down to the lowest supply voltage (0.45 V) featuring energy-quality scaling.

TABLE I
DAC PERFORMANCE COMPARISON

	This Work	[4]	[9]	[8]	[10]	[11]	[12]	[13]
CMOS Tech. F (nm)	180	40	40	180	180	180	350	180
Type	ReDAC	DDPM	ReDAC	ReDAC	cap+mos-string	R-string	curr. steer.	$\Sigma\Delta$
validation	meas.	meas.	sim.	sim.	meas.	meas.	meas.	meas.
Digital Area (10^6F^2)	0.075	0.17	0.30	0.39[a]	N/A	1	N/A	0.62
Area ($10^6\mu$m^2) / (10^6F^2)	0.00780 / 0.24	0.00127 / 0.79	0.00091 / 0.57	0.01359[a] / 0.42	0.045[d] / 1.39	0.15 / 4.6	0.014 / 0.11	0.10[‡] / 3.08
Resolution (bit)	13	12	10	10	10	12	9	N/A
Sample rate (kS/s)	100	110	400	1,450	200	72[b]	111	40[e]
Supply / min.supply (V)	0.6 / 0.45	1 / 0.7	0.6 / N/A	0.7 / N/A	0.6 / N/A	18 / 1.8	3.3 / N/A	1.8 / N/A
INL / DNL (LSB)	1.07 / 0.96	3 / 1	0.33 / 0.2	1.01 / 0.45	0.56 / 0.32	0.54 / 0.26	1.6 / 0.8	N/A
SFDR / THD (dB)	77.81 / 77.52	85 / 85	76.8 / 66.7	59.3 / 59.2	71 / N/A	N/A	N/A	N/A
SINAD (dB)	65.82	72	61.0	58.5	56.43	N/A	48[d]	103[f]
ENOB	10.64	11.6	9.9	9.4	9.08	N/A	8[d]	16.8
Power (μW)	0.88	50.8	0.44	9.15	0.85[d]	875[c]	33	700[g]
FOM / FOM$_A$ (dB)	172 / 178	160 / 161	176 / 178	166 / 170	165 / 164	N/A	140 / 149	174 / 169

† $\mathrm{FOM} = 10\log_{10}\left(\frac{2^{2\cdot\mathrm{ENOB}}BW}{P}\right)$ ⋆ $\mathrm{FOM_A} = \mathrm{FOM} + 10\log_{10}(1/A_\mathrm{F})$ being A_F the F-normalised area ‡ not including reconstruction filter [a]includes part of the calibration [b]from row-line time [d]based on text and figures [e]twice the signal bandwidth [f]A-weighted [g]analog power only.

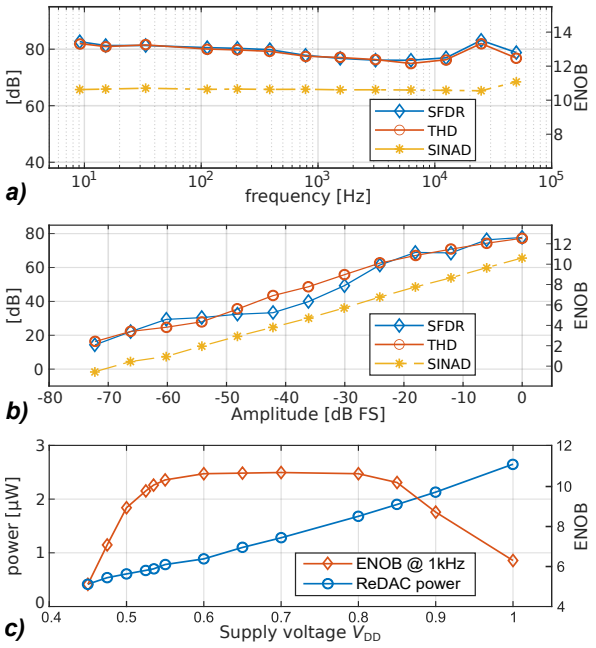

Fig. 6. Dynamic ReDAC characterization in frequency, 90% swing (a), and amplitude, 0.8 kHz (b).

Moreover, the Diff-ReDAC achieves the second best energy-efficiency figure of merit FOM of 172 dB (2 dB less than the FOM of the oversampled converter [13], which is based on A-weighted ENOB and has a 795× larger power consumption) and the best area-normalised FOM$_A$ of 178 dB (9 dB more than [13] and 29 dB more than the current-steering DAC [12]).

VI. CONCLUSION

A 100 kS/s 13 bit Differential ReDAC in 180 CMOS has been presented and validated on silicon for the first time. With its operation down to 0.45 V at 880 nW power consumption and 7,800 μm^2 area, the proposed Diff-ReDAC achieves the best-reported area normalized energy efficiency FOM$_A$ of 178 dB, thus revealing its potential as a power and area efficient general purpose DAC for ubiquitous consumer and IoT applications.

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