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Analysis of the impact of prototyping-related parasitic effects in a hybrid GaN power amplifier for 5G FR1 applications

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Abstract

This article analyses the impact of parasitic effects encountered in the manufacturing of a Gallium Nitride power amplifier optimized for a specific trade-off of efficiency and linearity at 5G FR1 frequencies. The analysis focuses on an example based on a packaged transistor and implemented in hybrid technology, adopting a two-layer printed circuit board for passive distributed elements and surface-mount lumped components. The design is summarized, and the focus is then posed on the comparison of simulated and measured results, the main causes of inaccuracy in their agreement, and a simple way of reproducing these in simulation. The mechanical stability of the assembly and the sensitivity of the second harmonic control are identified as the main sources of performance degradation. These effects are correctly modeled at the simulation level thanks to the insertion of specific parasitic lumped elements but could not be fully eliminated at the experimental level in this specific prototype. However, post-tuning performed on the prototype, guided by the proposed analysis, still allows to reach satisfactory performance although somewhat sub-optimal compared to the one expected from simulations. At 3.5 GHz, the re-tuned PA demonstrates a measured output power in excess of 37.5 dBm at saturation, with associated gain higher than 14 dB and PAE of 60%. In a 2-tone test with 20 MHz spacing, the IMD3 remains lower than −30 dBc up to 29 dBm of output power with a corresponding PAE of the order of 32%.

KEYWORDS

5G, efficiency, gallium nitride, intermodulation distortion, linearity, power amplifier

1 | INTRODUCTION

The performance of transmitters in wireless communication systems is significantly influenced by that of the power amplifier (PA), and designers in this field face the constant challenge of balancing efficiency and linearity. This challenge has become increasingly crucial in recent years due to the frequency spectrum becoming more crowded, which

has resulted in the adoption of very complex modulation signals to optimize the amount of information that can be carried out in a limited frequency band.

Recent modulations used in wireless communications are characterized by a high peak-to-average power ratio (PAPR), which causes the PAs to operate at an average power much lower than their maximum output power. Consequently, average efficiency is adversely affected, especially in standard amplifier architectures such as single-device amplifiers,[1–4] as well as balanced,[5] distributed,[6,7] and other similar PA architectures that typically attain maximum efficiency at saturation and drop rapidly away from it in output power back-off (OBO).

To address this issue, specific back-off efficiency enhancement techniques have been proposed and developed over the years. These techniques, such as load modulation[8–12] and supply modulation,[13–16] have shown great potential for improving efficiency in OBO. It is sometimes the case that these techniques are both applied to the same PA, such as in.[17–19] However, their implementation poses several challenges and may also complicate the inherent linearity of the PA and its ability to be linearized.

The linearity of the PA may be a more or less stringent requirement compared to other performance indicators such as output power, operating bandwidth, gain, and efficiency, depending on the targeted application.[20] While linearization solutions such as predistortion[21–24] or dual-input architectures[12,25,26] can enhance linearity and make it compatible with standards, they can also make PA circuit design more challenging. However, in some cases, it is essential to design a PA that is intrinsically compliant with stringent linearity requirements.

Another critical aspect is the sensitivity of the designed PA to several parameters, such as the bias voltage variations, the operating temperature,[27] the tolerance on the components' values, including the accuracy of the nonlinear model of the active devices,[28–31] and the variability that affects the manufacturing process. In general, hybrid implementations are affected by a stronger variability, related to manual manufacturing and assembly and to the adoption of off-the-shelf components, but allow for a re-tuning of the circuit after the manufacturing to correct possible shifts. Also, the spacing of the transistors and the overall larger circuit size often allow for better heat dissipation thus limiting the temperature sensitivity of the amplifier. On the contrary, the production process of monolithic integrated circuits is more repeatable, although affected by a certain amount of variability, but it allows little or no tuning after manufacturing[32,33] and is typically more sensitive to temperature variations due to the high power density per chip area and the more challenging heat dissipation. The complexity of the architecture, that is, the number of active devices, the presence of integrated driver stages, the spatial proximity of the active devices[34,35] and the presence or absence of isolating elements among them, has also an impact on its sensitivity. For instance, the single-device wideband PA of[36] presents a very good agreement between the target and the obtained frequency band, whereas the two-stage Doherty PA with embedded drivers presented in[37] is affected by a 2-GHz frequency shift. It allows however to fully cover the targeted band thanks to a specific wideband design approach.

The object of this paper is to analyze the parasitic effects related to the prototyping of a single-device class-AB PA and, once identified, to find a simple way of reproducing these effects at the circuit simulation level. The PA has been designed to maximize efficiency while satisfying stringent output power and linearity constraints around 3.5 GHz, targeting 5G applications in the FR1 frequency bands. The design targets are based on the rules imposed by the 2022 student design competition on high efficiency PAs held at the International Microwave Symposium. The PA should satisfy two main requirements, namely achieving an output power in the range 4–40 W in a single-tone test with input power lower than 24 dBm, and maximizing the PAE while maintaining all inter-modulation products below −30 dBc in a two-tone test with 20 MHz tone spacing.[38] The adopted design methodology is based on source and load pull simulations, at fundamental and second harmonic frequencies, aided by the identification of the parameters to which each of the targeted performance is more sensitive.

The PA has been initially fabricated with nominal component values and the experimental characterization in these conditions has evidenced the presence of a frequency shift in the small signal parameters (of about 250 MHz toward lower frequencies) and a slight degradation of the large signal performance at medium-high power. The PA has been shown to achieve, without any post-tuning, a measured output power of about 38 dBm and PAE in excess of 70% in a single-tone test at 3.25 GHz. It also achieves a 33% PAE at the −30 dBc third-order intermodulation distortion (IMD3) point in the 20 MHz two-tone test.[38]

A re-tuning of the parameters was carried out based on the scattering parameters of measurements, resulting in an enhancement of both small and large signal performance. However, despite these improvements, some performance discrepancies, particularly in terms of IMD3 profile at medium-high power, remain. By accurately modeling the deviations from the ideal behavior at the simulation level, we were able to identify the main sources of inaccuracy, namely the mechanical robustness of the assembly and the sub-optimal control of the second harmonic frequency. All in all,

the performed analysis leads to conclude that the design frequency was too high, and the corresponding second harmonic range too close to the reliability limits of the adopted technology and manual assembly, to allow for a fine tuning of the large signal performance that could also be robust and repeatable. These aspects will be analyzed and discussed in detail in the following Sections.

2 | DESIGN AND IMPLEMENTATION

The class-AB PA is designed at $f_0 = 3.5$ GHz, for a hybrid implementation targeting 5G applications, based on the 6 W packaged gallium nitride (GaN) high-electron-mobility transistor (HEMT) (CGH40006P) from Wolfspeed. The design specifications and detailed procedure are described in Reference 38 and briefly recalled here for completeness.

The active device is stabilized in and out of the operating frequency band thanks to a parallel RC ($R_2 \parallel C_4$, 150 Ω ‖ 1.4 pF) network on the gate and a shunt R (R_1, 120 Ω) along the gate bias path. The stability is verified at bias conditions around class-B and deep class-AB (i.e., V_{GS} ranging between −3.2 V and − 2.9 V), since this design strongly relies on the exploitation of the IMD3 sweet spots.

Source and load terminations are optimized at fundamental and second harmonic neglecting higher-order harmonic components marginally affecting the amplifier performance. Baseband impedances are monitored and optimized as well for their impact on IMD3. More in detail, the optimization of the various parameters can be partially decoupled. The selection of the optimum load at the fundamental frequency is a trade-off between IMD3 and PAE requirements. On the other hand, the IMD3 is deeply affected by the baseband termination, which has almost no impact on the output power at the fundamental, gain, and PAE in the 1-tone test. Finally, an additional constraint in the design is represented by the minimum gain (and corresponding minimum P_{out,f_0}) of the stage, mainly impacted by the load at the fundamental and input matching section.

The selected loads assure in simulation an IMD3 below −30 dBc, simultaneously satisfying the constraints of minimum output power with a margin of about 1 dB, to account for the passive networks losses and manufacturing inaccuracies.

Both Output (OMN) and Input (IMN) Matching Networks (MNs) are designed as a cascade of the $2f_0$ harmonic control and of the f_0 matching section. The baseband termination is optimized by tuning the DC decoupling capacitors in the supply lines. The prototype is manufactured on a Rogers 4350b substrate (3.66 relative dielectric constant, 0.762 mm substrate thickness, and 35 μm metal thickness).

The photograph of the realized prototype is shown in Figure 1, where the structure of the MNs is highlighted.

3 | RESULTS

The simulated performance expected from the amplifier is reported in Figure 2, where a sensitivity analysis versus process, voltage and temperature variations is also performed. The performance clouds refer to a Monte Carlo simulation

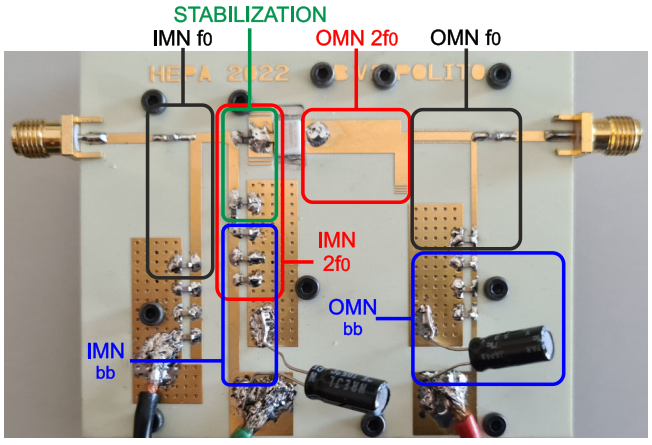

FIGURE 1 Photograph of the manufactured PA, where the stabilization and the IMN and OMN structures are highlighted.

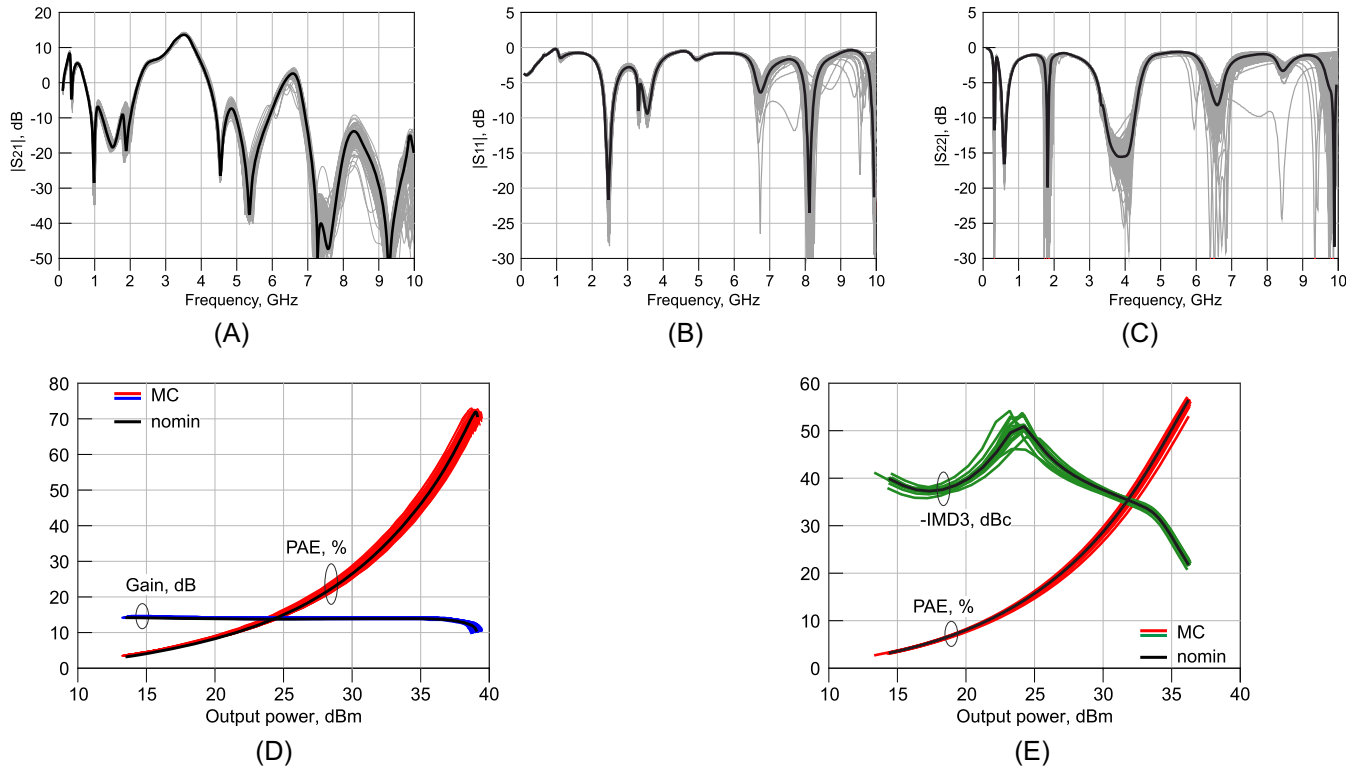

FIGURE 2 Simulated small and large signal performance of the designed amplifier (circuit v0) including process variability: (A) S_{21}, (B) S_{11}, (C) S_{22}, and (D) 1-tone at 3.5 GHz and (E) 2-tone at 3.5 GHz with 20 MHz tone spacing. The solid black curves refer to the nominal performance, that is, without any statistical variability. The curves in other colors in each figure refer to the Monte Carlo simulation, labeled as MC.

with 100 iterations. The transistor and SMDs parameters vary according to the statistics provided by the manufacturer in the model library, and the transmission lines dimensions have a user-defined variation that approximately represents the accuracy of the adopted manufacturing process. The temperature and voltage variations are assumed to be limited within 20% and 5%, respectively, based on the assessment of the adopted setup. The black curves indicate the reference nominal performance when no statistical variability is considered in the simulation.

At 3.5 GHz, the designed PA can provide a saturated output power in excess of 38 dBm with an associated PAE of 70%, while maintaining the required linearity in the 2-tone test up to an output power of 35 dBm and a PAE of 50%. The simulations accounting for the parameters variability evidence that the small signal performance is most sensitive to the variations at high frequency, near the second harmonic range, which translates into a maximum PAE variation of about 8%. The 2-tone test shows a similar variability in terms of PAE and sensitivity of the IMD3 that is more marked in the low-medium power region, where the sweet spot is located. On the contrary, the −30 dBc IMD3 crossing is only slightly affected (around 1 dB variation in the output power point corresponding to the crossing).

The PA has been mounted with the nominal values for transmission lines (TLs), surface-mount devices (SMDs) and edge launchers. The nominal values summarized in Table 1 refer to the equivalent circuit schematic of Figure 3, where TL_i has physical width W_i and length L_i indicated in mm and the values of resistor R_i and capacitor C_i are specified in Ω and pF, respectively. Note that the low-frequency decoupling capacitors and the input and output 50 Ω lines are omitted in the schematic. Additionally, $L_{\mathrm{p,S}}$ and $L_{\mathrm{p,D}}$, specified in nH, represent parasitic inductive effects at the Source and Drain terminals. They are initially assumed to be null, and more details will be provided in the following.

The small signal characterization has been performed in terms of scattering parameters of the amplifier considered as a two-port double bipole, where port 1 is the input (RF IN) and port 2 is the output (RF OUT). The experimental test-bench adopts a 2-port Keysight VNA (E8361A), calibrated at the DUT planes by means of a short-open-load-thru (SOLT) calibration procedure.

The placement of the calibration planes has been considered when comparing measurements and simulations; the presence of the edge launcher amounts to a shift of approximately 20° from the PCB edge. However, this shift has a

TABLE 1 Values of the nominal passive components relative to the schematic of Figure 3.

Network	Parameter	Units	v0
IMN, f_0	W_1, L_1 (TL_1)	mm, mm	0.97, 5.7
IMN, f_0	W_2, L_2 (TL_2)	mm, mm	1.8, 18.6
IMN, f_0	W_3, L_3 (TL_3)	mm, mm	1.48, 3.68
IMN, $2f_0$	W_4, L_4 (TL_4)	mm, mm	1.63, 8.5
IMN, $2f_0$	W_5, L_5 (TL_5)	mm, mm	6.3, 4
OMN, $2f_0$	W_6, L_6 (TL_6)	mm, mm	5.27, 14.17
OMN, $2f_0$	W_7, L_7 (TL_7)	mm, mm	1.63, 4.4
OMN, f_0	W_8, L_8 (TL_8)	mm, mm	1.3, 9.54
OMN, f_0	W_9, L_9 (TL_9)	mm, mm	0.9, 16
OMN, f_0	W_{10}, L_{10} (TL_{10})	mm, mm	1.16, 4.68
IMN, f_0	C_1	pF	47
IMN, f_0	C_2	pF	2.7
Stabilization	C_3	pF	3.3
Stabilization	C_4	pF	1.4
OMN, f_0	C_5	pF	3.3
OMN, f_0	C_6	pF	47
IMN, bb	$C_{DC,i}$	pF	33
OMN, bb	$C_{DC,o}$	pF	100
Stabilization	R_1	Ω	120
Stabilization	R_2	Ω	150
Parasitic effect at Source terminal	$L_{p,S}$	nH	0
Parasitic effect at drain terminal	$L_{p,D}$	nH	0

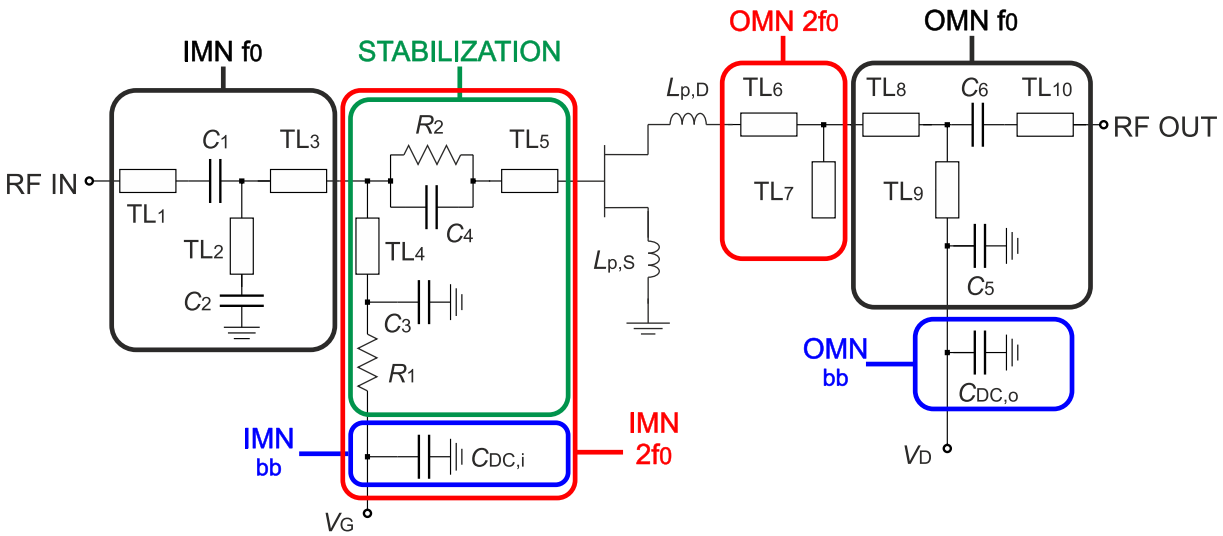

FIGURE 3 Schematic of the designed PA, where the stabilization and the IMN and OMN structures are highlighted.

negligible effect on the simulated large signal performance. Therefore, for the sake of conciseness, only the magnitudes of the scattering parameters will be shown in the following discussion. The resulting measurements (thin lines with symbols) are compared to the simulated ones (thick solid lines) in Figure 4. Such simulation runs on the circuit v0, which illustrates the originally designed behavior. A shift toward lower frequencies in the position of the main peak of

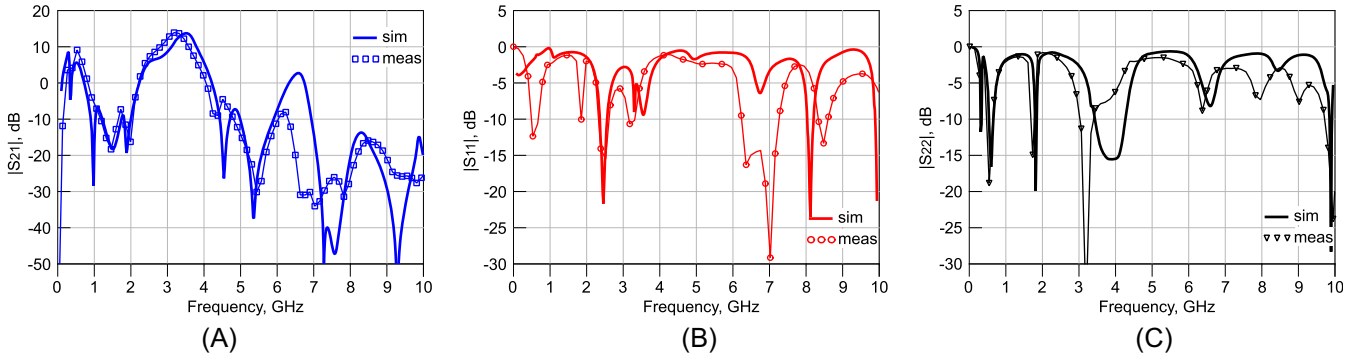

FIGURE 4 Comparison of measured (symbols) scattering parameters and simulations on circuit v0 (solid): (A) S_{21}, (B) S_{11}, and (C) S_{22}.

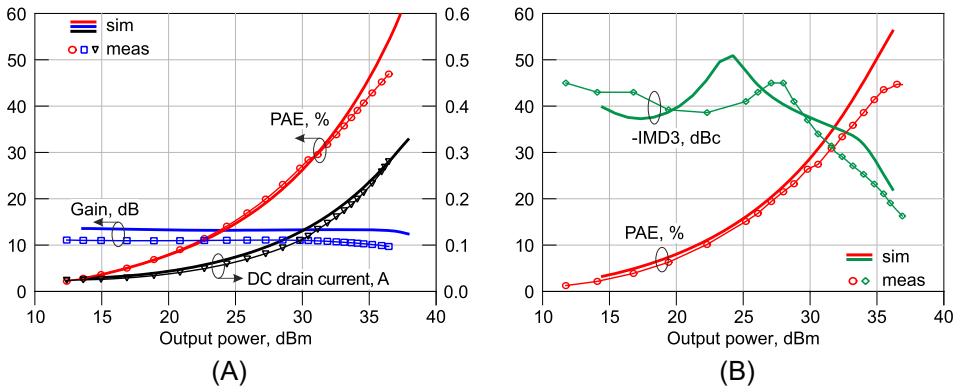

FIGURE 5 Comparison of measured (symbols) large signal performance and simulations on circuit v0 (solid): (A) 1-tone and (B) 2-tone with 20-MHz spacing.

S_{21} can be observed, of about 250 MHz. Additionally, the agreement is deteriorated above 5 and 6 GHz, both in terms of gain and input/output return losses. This is partially expected, since the guaranteed operating range of both substrate and transistor only extends up to 6 GHz.

The 1-tone large signal characterization is performed on a real-time vector bench calibrated through a two-step procedure: a two-port SOLT for the relative calibration compared to a reference, followed by a SOL calibration at an extended output port connected to a power meter for the absolute power calibration. As expected, the comparison between simulations and measurements at the design frequency of 3.5 GHz does not present a very good agreement, due to the shift observed in the scattering parameters both at the input and at the output. In particular, as shown in Figure 5A the power gain is lower, and so are the saturated output power and efficiency at the similar gain compression. Note that the full PA characterization has not been performed in strong compression due to the maximum input power imposed by the design requirements.

The linearity of the stage is evaluated by measuring the IMD3 in a two-tone test with 20 MHz tone spacing.[39] Even if other metrics are available, such as AM-AM and AM-PM distortion[40] or more sophisticated system-level metrics (adjacent channel power ratio, noise-to-power ratio[41]), they are often adopted to benchmark the linearity of the amplifier in real field conditions, while the two-tone test is mainly adopted during the design phase as an initial estimation of the linearity.

The 2-tone large signal characterization adopts a two-locked source 4-port Keysight VNA (N5227A). Figure 5(B) reports the IMD3 (with opposite sign, for convenience) and PAE curves and highlights the similar discrepancy as observed in the 1-tone performance. The measured PAE at medium-high power is lower than predicted by simulations, and the IMD3 has a different trend altogether, across the whole power sweep. All in all, the PAE at −30 dBc IMD3 results of 30% in measurements, compared to the 48% expected from simulations. Since the IMD3 is very sensitive to V_{GS} variations, especially in deep class AB, the measurements have been repeated at several bias conditions. It has been

TABLE 2 Values of the passive components modified in the circuit versions v1 and v2.

Parameter	Units	v0	v1	v2
TL_2 (W_2, L_2)	mm, mm	1.8, 18.6	1.8, 19.6	1.8, 19.60
TL_4 (W_4, L_4)	mm, mm	1.63, 8.5	1.63, 9.5	1.63, 9.5
TL_5 (W_5, L_5)	mm, mm	6.3, 4	6.3, 6	6.3, 6
TL_6 (W_6, L_6)	mm, mm	5.27, 14.17	5.27, 17.17	5.27, 17.17
TL_7 (W_7, L_7)	mm, mm	1.63, 4.4	1.63, 5.4	0.93, 5.4
$L_{p,S}$	nH	0	0	0.1
$L_{p,D}$	nH	0	0	0.5

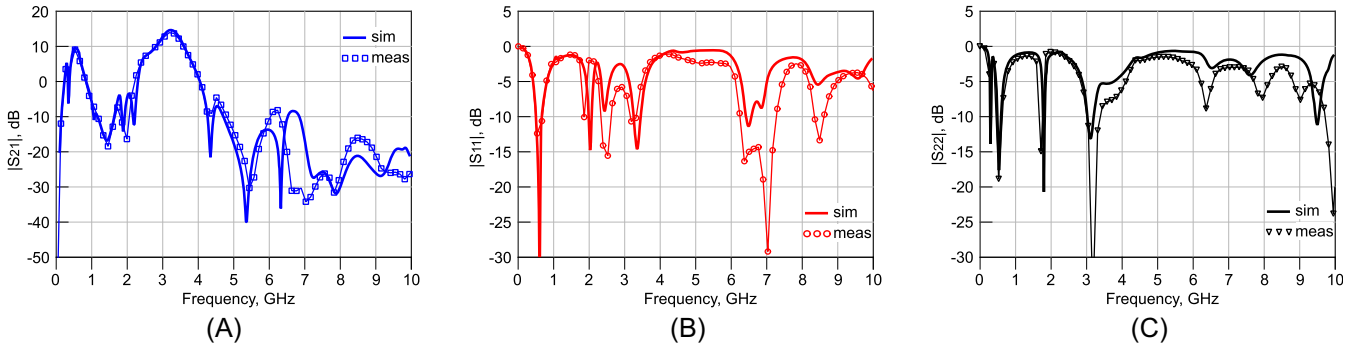

FIGURE 6 Comparison of measured (symbols) scattering parameters and simulations on circuit v1 (solid): (A) S_{21}, (B) S_{11}, and (C) S_{22}.

verified that the position and depth of the sweet spot can be varied, but the performance at medium-high power remains almost unchanged.

Attempts at re-tuning have been done by modifying the size of the transmission lines and stubs, as well as the values of the SMDs of the demonstrator. The main guide adopted to evaluate improvements in the agreement during this procedure has been the scattering parameters. It has been observed that the frequency shift of the S_{21} peak can be recovered, and all the S_{ij} scattering parameters (with $i,j = 1,2$) can be brought to a good agreement with simulations up to 5–6 GHz. The resulting 1-tone performance is also in good agreement, but the 2-tone one is not. However, circuit optimization and re-tuning based on 2-tone measurements are rather unpractical.

Therefore, the goal of the investigation detailed in this article is a reverse procedure, based on the modification of the circuit in simulation to reproduce the performance obtained during the measurement campaign and hence gain some insight into the sources of disagreement.

As the first step, the original circuit (v0) has been modified to get the best agreement in terms of scattering parameters (v1). The modifications to the circuit are those highlighted in Table 2. The most sensitive parts are the lines closest to the active device (TL_5, TL_6) and the stubs (TL_2, TL_4, and TL_7), especially the ones that implement the second harmonic control. The effective length of the lines toward the device may be affected by inaccurate modeling of the position of its reference planes as well as the precision of the PCB cut where the package is inserted. The main source of length shift for the capacitor-terminated stubs, instead, is the position in which the capacitor is soldered, whereas deviations of the actual capacitance away from the nominal value have a lesser impact.

The resulting scattering parameters are reported in Figure 6. It can be noted that the S_{21} behavior in the band can be perfectly captured and that all the positions of the secondary resonances of all parameters can be very well reproduced up to 9 GHz, which fully includes the second harmonic range ($2f_0 = 7$ GHz). The agreement in terms of magnitude above 6 GHz is better for S_{11} and S_{22}, whereas the magnitude of S_{21} is still affected by a partial disagreement, which could not be recovered.

The corresponding large signal performance of circuit version v1 is shown in Figure 7. The 1-tone simulated performance (Figure 7(A)) has become more in line with the measured one in terms of gain, whereas the saturated power is still around 1.5 dB higher, with a consequent difference of 10% points in the maximum PAE. The agreement in the

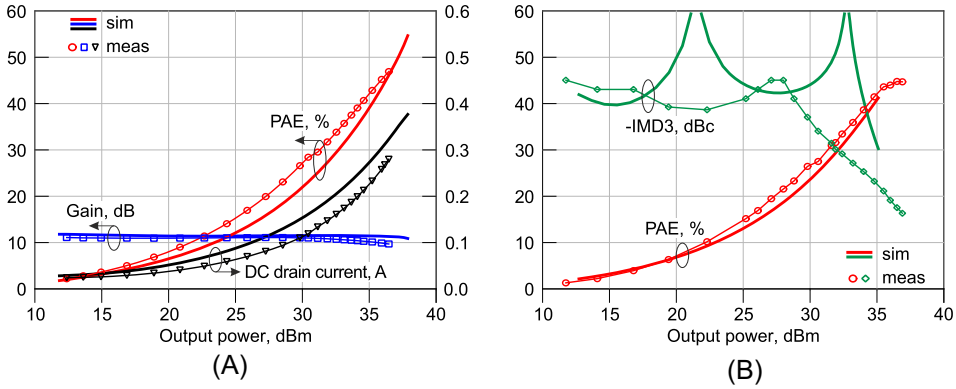

FIGURE 7 Comparison of measured (symbols) large signal performance and simulations on circuit v1 (solid): (A) 1-tone, and (B) 2-tone with 20-MHz spacing.

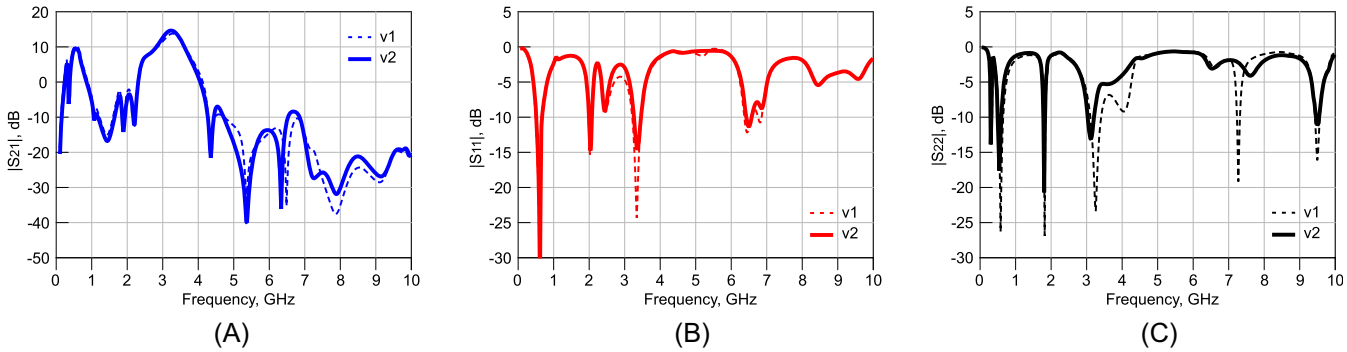

FIGURE 8 Comparison of simulated scattering parameters of circuit v2 (thick solid) and v1 (thin dashed): (A) S_{21}, (B) S_{11}, and (C) S_{22}.

2-tone simulated performance (Figure 7(B)), on the other side, has significantly improved in terms of PAE, but the IMD3 curve has assumed a very different trend. Two sweet spots are now present, and the slope of the curve near saturation has become steeper. The resulting simulated PAE at −30 dBc IMD3 is now 42%.

Then, the circuit has been further modified to get the best agreement in terms of 2-tone performance (v2), while ensuring that the agreement of the scattering parameters is not compromised at least in the working band. The modifications to the circuit are highlighted in Table 2. This only required modifications to the OMN, in particular to the stub that implements the $2f_0$ control, whereas the rest of the MNs is unchanged. The passive circuit is however modified to include parasitic effects at the source and drain of the transistor. The possible cause of these inductive parasitic effects has been identified in a circuit assembly that is not so mechanically stable. For instance, air gaps below the device package (main body and flanges) may have such effect. These inductances have proven to have a strong effect on linearity. Finally, a slight tuning of the gate bias voltage was also required, from −3.08 V to −3.03 V. A similar modification of the bias is most likely unfeasible in a real experimental setup, where the resolution of the power supply unit cannot allow this fine tuning. A possible practical implementation compatible with this range of variation would require the insertion of ad-hoc trimmers on the bias lines.

The resulting scattering parameters are reported in Figure 8, where they are compared to the ones of circuit version v1 (dashed lines). It can be noted that:

1. S_{11} is almost unchanged, compatibly with a modification that only affected the OMN;
2. S_{22} is slightly modified around the operating frequency (3–4 GHz), where the mismatch increases, and most noticeably modified around the $2f_0$ range (6–8 GHz), where a shift in the position of a local minimum is clearly visible; and
3. consequently, S_{21} is mainly unchanged until 6 GHz, apart from a small difference in the gain at f_0, and varies primarily from 6 GHz to 8 GHz.

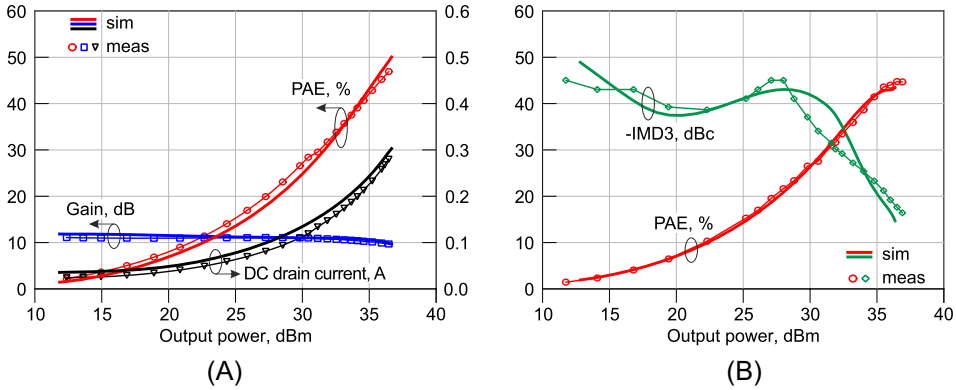

FIGURE 9 Comparison of measured (symbols) large signal performance and simulations on circuit v2 (solid): (A) 1-tone and (B) 2-tone with 20-MHz spacing.

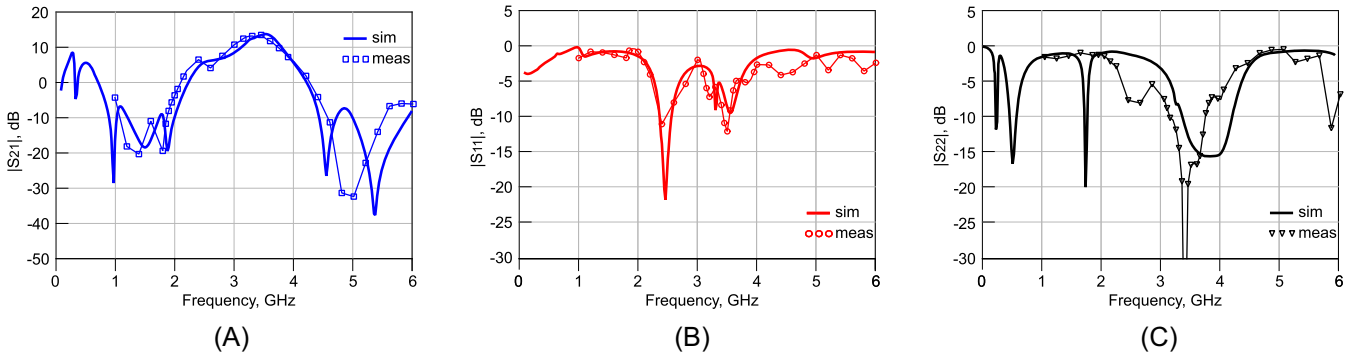

FIGURE 10 Comparison of re-tuned measured (symbols) scattering parameters and simulations on circuit v0 (solid): (A) S_{21}, (B) S_{11}, and (C) S_{22}.

The corresponding large signal performance of circuit v2 is shown in Figure 9. The 1-tone simulations (Figure 9A) now capture very accurately all the performance indicators of interest, namely power gain, PAE, and total DC current consumption. As a consequence, the saturated output power also correctly predicts the measured one.

The agreement in the 2-tone performance (Figure 9B), which is what the circuit modification was based on, is also very good at this stage. The PAE is perfectly captured at all power levels, and the IMD3 curve reproduces with a reasonable degree of accuracy (within 5 dB difference) the measured one, especially in terms of the position of the sweet spot and slope close to saturation. A difference in the PAE at −30 dBc still exists (34% simulated versus the 30% measured one), but this can be considered reasonable since the IMD3 measurement is the one affected by a larger error (approximately 2 dB in the adopted experimental setup) and the model of the transistor may also have some inaccuracy.

Finally, the prototype has been re-tuned based on the outcome of the previous analysis, applying the reverse modifications to the circuit elements highlighted in Table 2. However, no modification was possible to counteract the parasitic elements $L_{p,S}$ and $L_{p,D}$.

The resulting prototype has been experimentally characterized, both in small and large signal conditions. The measured performance is summarized in Figure 10 and Figure 11, where it is compared to the simulations of circuit v0, that is, the expected performance of the originally designed amplifier. The frequency shift of the S_{21} peak present in the initial version of the prototype is almost fully recovered, and a very good agreement is also obtained in terms of input return loss (S_{11}). Some discrepancies are still present in the output return loss (S_{22}), which is somewhat expected from the previous analysis. In fact, the re-tuning allows obtaining a very good agreement in terms of large signal performance, especially under 1-tone excitation, despite some differences in the small signal parameters. Finally, the 2-tone performance has also become more in line with the predicted one, despite a difference in the IMD3 slope toward saturation.

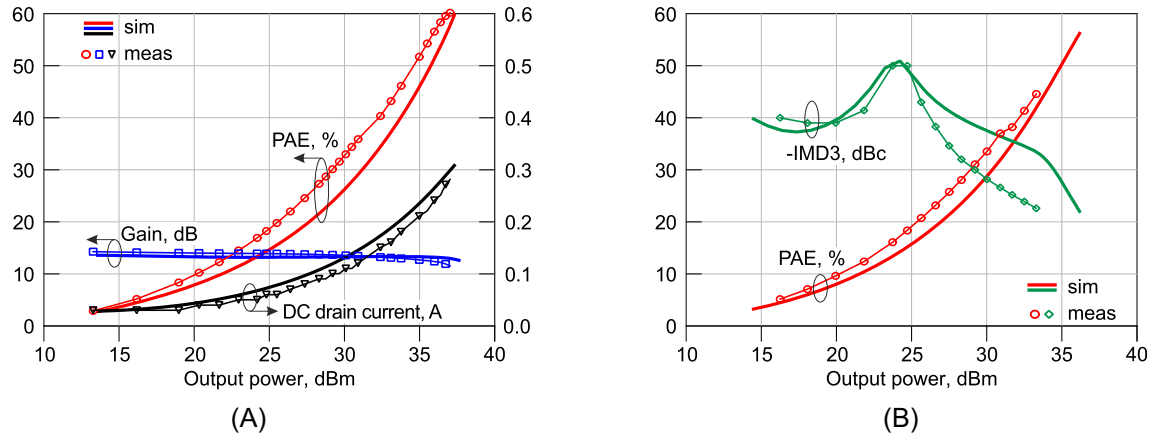

FIGURE 11 Comparison of re-tuned measured (symbols) large signal performance and simulations on circuit v0 (solid): (A) 1-tone and (B) 2-tone with 20-MHz spacing.

TABLE 3 Comparison of the re-tuned class-AB with similar PAs from the scientific literature.

Ref.	Topology	Freq. (GHz)	Output power (dBm)	Efficiency (%)	Gain (dB)	IMD3 (dBc)
42	Doherty	2.9–3.3	43.9	70	11	–
43	Class AB	3	35	60	13.5	−30 (@ 34 dBm)
44	Doherty	3.5	40	72	14	−30 (@ 40 dBm)
45	Doherty	3–3.7	44.2	74	13	–
This Work	Class AB	3.5	37.5	70	14	−30 (@ 30 dBm)

Table 3 summarizes the measured performance of the re-tuned prototype and compares it with similar examples taken from the available scientific literature. Although the re-tuning has not completely restored the expected performance, the PA shows competitive results in line with the state of the art. Note also that the larger signal performance of the re-tuned PA at 3.5 GHz is very similar to the one that it initially showed at 3.25 GHz without any re-tuning, as mentioned in Section 1 and presented in Reference 38.

4 | DISCUSSION

The reverse process described in Section 3 has allowed reproducing in simulation the performance modifications observed during the experimental characterization campaign of the hybrid PA. This has been obtained by acting on three main aspects:

1. the physical dimensions of the distributed elements in the IMN and OMN;
2. the gate bias voltage; and
3. the parasitic effects related to the prototype assembly.

On the contrary, post-tuning on the realized prototype to recover the frequency shift based on the comparison of scattering parameters has not allowed to fully replicate in measurement of the performance expected from simulations of the original circuit (v0), although a significant improvement of the performance is observed. The remaining discrepancy can be ascribed mainly to the parasitic effects relative to the prototyping, which could be properly modeled in simulation but could not be removed in the realized hardware. Some further improvement could possibly be obtained by improving the source contact (e.g., with better mechanical control of the carrier roughness, or a more robust mounting), which was not possible to apply to the hardware presented in this work. Note also that these effects could not be taken into account by the sensitivity analysis initially performed (see Figure 2).

The process described in this work suggests that, in a case such as this, the scattering parameters are not a sufficiently good indicator of the conformity of the implemented prototype to the corresponding simulated design. The main reason, in the authors' opinion, resides in the strong effect of the second harmonic control in the specific linearity-efficiency trade-off sought here, together with the fact that the second harmonic falls outside of the frequency range where the performance of the adopted transistor and substrate are guaranteed.

In fact, it has been shown that a set of circuit parameters able to perfectly match the small and large signal measurements simultaneously could not be found and that a satisfactory match of the 2-tone large signal performance can be achieved with a set of parameters that do not capture the scattering parameters at $2f_0$. Consequently, a post-tuning of the prototype to recover the desired performance would have been possible, if the 2-tone performance were used as a guide instead of the scattering parameters. This, however, is strongly impractical and leads to the conclusion that the proposed class-AB PA has the potential to fulfill the requirements but has a strong sensitivity to many aspects of the prototyping.

Finally, this work has provided experimental evidence that a technology pushed to its frequency limits, such as in this case, is not very robust for designs that aim at maximizing the device performance in a relatively narrow frequency range. The design would result more robust if it aimed to maintain slightly suboptimal performance on a wider frequency band, which however is not in line with the framework for the presented design. On the contrary, if a fine tuning of the termination impedances from the baseband to the second harmonic is targeted, the design frequency should be kept low enough for the whole relevant frequency range to fall well within the range where all the adopted components and their electrical models are reliable.

5 | CONCLUSION

The paper has presented a study of the prototyping-related parasitic effects in a single-stage class-AB GaN power amplifier designed to trade off efficiency and linearity and operate in the 5G FR1 frequency range. The analysis is based on the comparison of an initial set of measurements with different sets of simulated results, which model different sources of discrepancy between the expected results and the obtained ones. The most common one, related to the components tolerances and pcb manufacturing inaccuracies, can be successfully recovered thanks to post-tuning. However, this case study also evidences the impact of different aspects related to manufacturing, which cannot be solved a posteriori and would require a full re-design and possibly a different technological implementation. The most critical aspects are identified in the mechanical stability of the assembly and the accuracy of the second harmonic control. As a practical guideline to mitigate the effects of these inaccuracies, it appears very important to ensure good mechanical robustness of the assembly (launchers, device mounting) due to their strong impact on the performance. On the other hand, the operating frequency must be kept far enough from the maximum ratings for the transistor and substrate adopted in the selected implementation, especially if waveform engineering is adopted in the design.

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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