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# Maximum Peak Current and Junction-to-ambient Delta-temperature Investigation in GaN FETs Parallel Connectionct 2

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ABSTRACT PEAK CURRENT AND JUNCTION-TO-AMBIENT DELTA-TEMPERATURE INVESTIGATION IN GAN FETS PARALLEL

In power inverter applications, Gallium Nitride (GaN) technology demonstrates advantages of energy conversion quality, power density, and efficiency, such as in medium to high switching frequency motor drive. The parallel connection of GaN FETs increases the current capability of power switches. In the parallel connection, wide threshold voltage $V_{GSth}$ spread of GaN FETs is the main parameter to consider. This paper investigates peak current and thermal response depending on the number $N$ of GaN FETs connected in parallel and the operating conditions. This study provides new insights for the design of a board with a large number of paralleled GaN FETs. The target is to show how the peak current and the maximum junction-to-ambient delta-temperature are related to the $V_{GSth}$ spread. In order to separate the PCB or parasitic impedance effects from the device parameter spread one into the analysis, it was agreed to proceed by running simulations with a validated GaN FET model. A comparison between the maximum spread declared in the datasheet, to the typical one that can be found on the same production lot is carried out. Furthermore, switching operation and temperature evaluations are analyzed.

## Introduction

Gallium nitride FET is increasingly being used in many high switching frequency converter applications due to its advantages such as minor power loss and size reduction characteristics. It has a great potential for application in the field of motion control, and it significantly features the increasing of the performance of the motor-drive system in terms of (Palma, Musumeci, Mandrile & Barba, 2021; Wang, Li & Han, 2015)

- lower total harmonic distortion (THD) of the current output waveforms
- higher torque obtained by reducing harmonics and related oscillations (Brosch, Rauhaus, Wallscheid, Boecker & Zimmer )
- higher total system efficiency (Musumeci, Mandrile, Barba & Palma, 2021).

In GaN FET a two-dimensional electron gas (2DEG) is created at the interface of AlGaN on top of GaN crystal. The threshold voltage ($V_{GSth}$) is when the 2DEG underneath the gate is fully depleted by the voltage generated by the gate electrode. This occurs when the voltage of the gate balances the voltage generated by the piezoelectric strain in the AlGaN/GaN barrier. Enhancement-mode or cascode device has a positive threshold voltage and do not have a p-n diode, but they do conduct in a way similar to a diode in the reverse direction (Lidow, Strydom, de Rooij & Reusch, 2020). The absence of body diode typical of MOSFETs and the possibility of current flowing from the drain to the source and vice versa allows using the GaN FET as bidirectional switch (Musumeci, Panizza, Stella & Perraud, 2020).

To extend their use to high-power applications several devices need to be connected in parallel. The current sharing of paralleled GaN FETs is still considered a challenge because of the various parameters spread of the power device and parasitic components in layout management (Zhang & Zhang, 2018). Paralleling design considerations and the switching loss distribution evaluation among paralleled GaN FETs are presented in Ruoyu& Lu, Hou and Chen (2018).

A challenge for parallel operation of several power devices is attributable to the that the various parasitic parameters of the power device, power stage, and its gate driver circuits are very sensitive. To reduce the influences from the parasitic components, different packaging for power devices have been proposed (Luo et al., 2014). The parameters mismatch of the parallel circuit legs will lead to a significant effect on the dynamic characteristics and bring the thermal problem management to the GaN FETs (Zhang et al., 2019). Generally, the current imbalance in parallel connection are caused by the device parameters mismatching, package parasitic inductances and the PCB design

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choices (Musumeci, Scrimizzi, Longo, Mistretta & Cavallaro, 2020). In literature, the main impact of the parameter variation on the parallel connection of super-junction power MOSFET devices has been experimental studied and evaluated in several operative conditions (Chimento, Raciti, Cannone, Musumeci & Gaito, 2009). For the GaN FETs, experiment results verified that the parasitic parameters have also a great influence on switching characteristics (Yajing et al., 2018). In insulated gate devices, the main parameter involved in the current difference during the transient behavior is the threshold voltage $V_{GSth}$ as demonstrated in Musumeci et al. (2019). Safe working operation prevents thermal runaway and hottest cell destruction (Cheng & Chou, 2014).

The analysis of the electrical parameters that critically influence the feasibility of the parallel-connected GaN FETs have been explored in Musumeci et al. (2019); Zhang and Zhang (2018).

This study provides new insights into the choice of the number of GaN FETs to be connected in parallel under specific operating conditions. It is useful for the preliminary design phase of circuit boards with a large number of devices connected in parallel.

This paper aims to exclude effects due to PCB and parasitic impedances introduced by the layout arrangement. If proceeding through the experimental evaluation, the effects due only to the parameter spread would be covered by those introduced by these parasitic impedances. For this reason, it is reasonable to proceed by performing simulations using a validated GaN FET model.

Simulations investigation demonstrated that the main critical parameter to consider is the threshold voltage $V_{GSth}$ spread. It constrains the possibility of connecting many devices in parallel when a high current level is required to operate at a fixed switching frequency. The analysis carried out shows how to estimate the maximum current peak for each paralleled device during commutation. Then, the map of the maximum junction-to-ambient delta-temperature $\Delta\theta_{JA}$ of the most stressed GaN FET as a function of the number of devices $N$ and the switching frequency $f_{sw}$ is given.

In the parallel connection of $N$ GaN FETs, the worst-case condition appears when only one device, named (A), has the minimum $V_{GSth}$ and all the others have the maximum one. The maximum $V_{GSth}$ spread of 1.8 V is declared in the GaN FET datasheet. In GaN FET EPC2065 (from EPC©) $V_{GSth}$ are: typical $V_{GSth\ typ} = 1.2$ V, minimum $V_{GSth\ min} = 0.7$ V, and maximum, $V_{GSth\ max} = 2.5$ V. If all GaN FETs come from the same production lot, it is possible to consider the $V_{GSth}$ spread from $V_{GSth\ typ}$ to be reduced by half (considering a range of 0.7 V between $V_{GSth,\min}$ and $V_{GSth,\max}$). Thus, the case of a typical threshold voltage spread ($V_{GSth\ min} = 0.95$ V and $V_{GSth\ max} = 1.65$ V) can be considered. The chosen values of the circuit parameters and these spreads cause a turn-on time delay between the most stressed device and all other devices. In the paper, an analysis with several simulation runs in LTSpice is performed considering the model of the EPC2065 GaN FET for the parallel connection circuit.

## GaN FET Model Notes

The full electrical scheme of the system used in the simulation runs is shown Fig. 1. In this layout, N GaN FETs are connected in parallel. Each one is driven by its own voltage source. The driving signals are sent synchronously to every device. The driving voltage $V_q$ has been set as a square waveform voltage source with 5 V amplitude, rise time and fall time equal to 0.1 ns and duty cycle 0.5. Unlike MOSFETs, in GaN FETs the $V_q$ amplitude is a design constraint and cannot have wide variations from the designated value. $R_G$ indicates the gate resistance and its value is 10 Ω for every GaN FET. The value of the gate resistance is chosen according to have a slew rate drop (95%−5%) of 5 V/ns that is good for a motor drive application. A parasitic source inductance $L_S$ for each device is introduced. Cases with $L_S$ having a typical value of 200 pH due to a well-executed PCB layout and without $L_S$ will be compared in the following sections. The load is modeled as a current source $I_{load}$. It works with a DC load voltage of $V_{load} = 48$ $V$. A freewheeling diode is connected in parallel with the load current source. The freewheeling diode can be regarded as a GaN FET operating in reverse conduction, and therefore has no reverse recovery during transients.

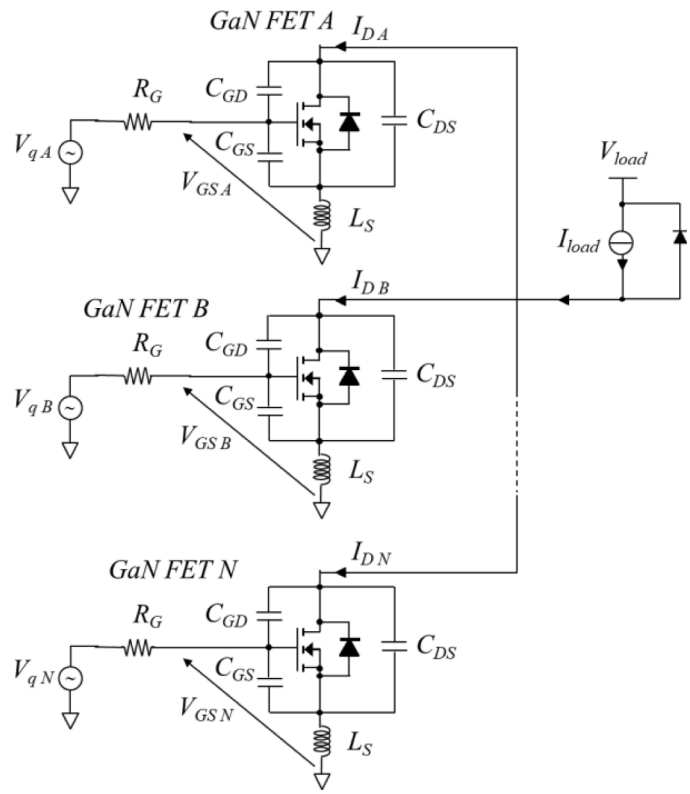


**Fig. 1.** Electrical schematic for N parallel-connected GaN FETs.

The equivalent electrical schematic of the GaN FET model is shown in Fig. 2.

The model of the GaN FET comes from the base model of a typical MOSFET and it is a modified property (Lidow et al., 2020). The three resistors called $R_G$, $R_D$ and $R_S$ are the gate, drain and source electrical inner resistors. The drain current value is modelled by a controlled current generator as function of the gate voltage ($V_{GS}$), the output drain-source voltage ($V_{DS}$) and the temperature (θ) (Cheng & Chou, 2014). The parasitic capacitors are needed to model the dynamic behavior of the GaN FET. Each one connects two of the three poles of the device and is composed of two different capacitance terms. One term is constant and represents the typical behavior of a capacitor ($C_{GD0}$, $C_{GS0}$, $C_{SD0}$), the other capacitances are a voltage-dependent functions in parallel to model the depletion characteristics ($C_{GD1}$, $C_{GS1}$, $C_{SD1}$).

In this work, a GaN FET from EPC (EPC2065) with conduction

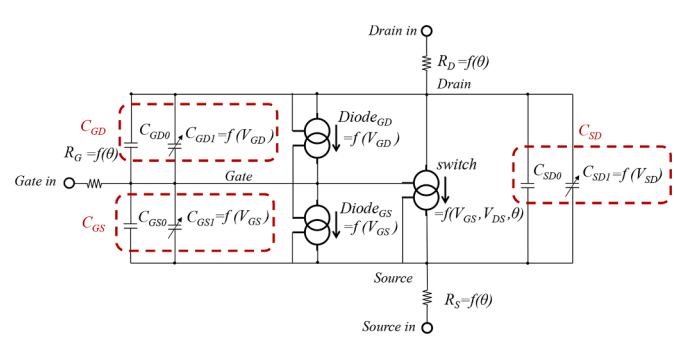


**Fig. 2.** Equivalent electrical schematic of the GaN FET model.

resistance $R_{on} = 3.6\ m\Omega$, and a maximum drain-source voltage of 80 V are used for the modeling features. In the modeling approach, the non-linear behaviours of the parasitic capacitances and all the temperature dependencies are considered.

This model has proved to be a good representation of the device's operation, including those caused by its internal parasitism. It has been validated by comparing the waveforms resulting from simulation with those experimentally measured. In the experimental tests the GaN FET operation condition is in a Synchronous Buck Converter configuration supplying an inductive load with 48 V bus voltage and 10 A load current. More test details are in Barba et al. (2022). Fig. 3 shows the comparisons of the GaN FET $V_{GS}$ and $V_{DS}$ waveforms coming from simulation (solid lines) and those experimentally measured (dashed lines) on the lower device of a Synchronous Buck Converter used as workbench. Waveforms referring to the turn-off transient are depicted on the left, while those referring to the turn-on transient are depicted on the right.

$V_{GS}$ waveform (see upper plots of Fig. 3) show a flat interval due to the variation of the input capacitance value $C_{ISS}$=$C_{GD}$+$C_{GS}$, which is non-linear with the gate current $I_G$. The $V_{GS}$ value for which this plateau occurs is called the Miller voltage $V_{Miller}$ and is related to the threshold voltage and the drain current $I_D$ according to the relation

$$V_{Miller} = V_{GSth} + I_D/g_m \tag{1}$$

where $g_m$ indicates the gain of the GaN FET. Furthermore, being $V_{Miller}$ related to $V_{Gsth}$, it determines the variation of the drain current $I_D$ of the device over time according to the formula

$$\frac{dI_D}{dt} \approx \frac{g_m \cdot I_G}{C_{ISS}} \approx \frac{g_m \cdot (V_q - V_{Miller})}{R_G \cdot C_{ISS}} \tag{2}$$

In order to describe the freewheeling diode, the GaN FET transient handling of the turn-on is investigated on the lower device of a Synchronous Buck Converter used as a workbench. A dead time of 100 ns and a load current of 6 A entering into the switching node are set. Fig. 4 shows the comparisons of the lower GaN FET $V_{DS}$ waveform coming from the simulation (yellow lines) and the experimentally measured one (black lines). During the dead time, the equivalent GaN FET body-diode causes a reverse conduction voltage drop $V_{RC}$. Its amplitude is highlighted in Fig. 4. Then, the GaN FET turn-on corresponds with the turn-off of the GaN diode operation.

## Maximum Peak Current

Device (A) (with $V_{GSth\ min}$) turns on earlier and turns off later than other GaN FETs that have the maximum threshold voltage fixed ($V_{GSth\ Max}$). For this reason, the higher current always appears on the (A) GaN FET. Turn-on and turn-off time gaps, caused by the $V_{GSth}$ spread, determine the current peak duration.

The peak drain current value is the sum of the effects of the parasitic

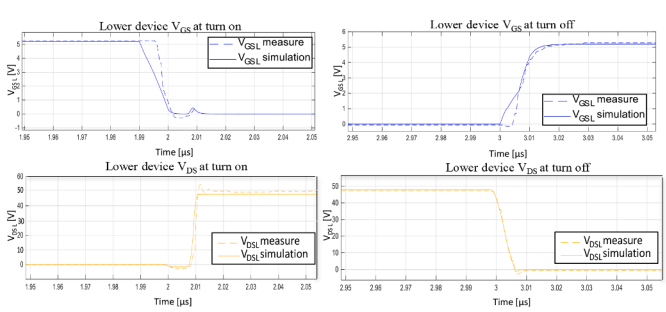


**Fig. 3.** GaN FET based Synchronous Buck converter switching cycle at 48 V bus voltage, 10 A load current. Simulation results are solid lines. Experimental results are dashed lines. (left) turn-off; (right) turn-on. (up) gate-source voltages of the low GaN FET $V_{GS\ L}$, $V = 1$ V/div; (down) drain-source voltage of the low GaN FET $V_{DS\ L}$, $V = 10$ V/div. Timestep 10 ns/div.

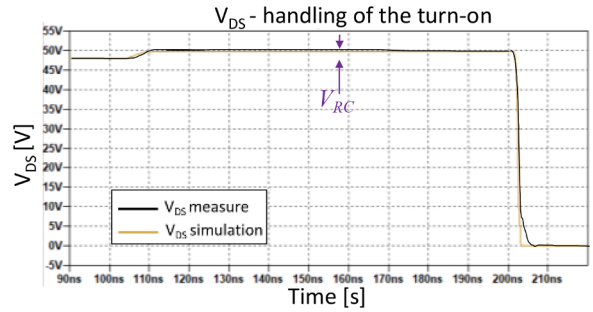


**Fig. 4.** GaN FET based Synchronous Buck converter switching cycle at 48 V bus voltage, 6 A load current, 100 ns dead time. GaN FET drain-source voltage during the handling of the turn-on. Simulation results is in yellow. Experimental result is in black. Equivalent GaN FET body-diode causes a reverse conduction voltage drop $V_{RC}$. $V = 1$ V/div; (down) drain-source voltage of the low GaN FET $V_{DS\ L}$, $V = 5$ V/div. Timestep 10 ns/div.

output capacitances $C_{OSS\ n}$ and the rising current during GaN FETs switching delay. It is expressed in (3) for the turn-on and the turn-off commutations.

$$\begin{cases} I_{D\ A\ pk\ (turn-on)} = \dfrac{di_{D\ A}}{dt} \cdot t_{cr} + (N-1) \cdot I_{C_{OSS\ n\ pk}} \\ I_{D\ A\ pk\ (turn-off)} = I_{load} - (N-1) \cdot I_{D\ n\ min}(v_{GS\ n}) \end{cases} \tag{3}$$

The first GaN FET (A) that changes its conduction state causes the drain voltage variation. $V_{GSth\ min}$ determines the current rise slope $\frac{di_{D\ A}}{dt}$. In the cases of wide $V_{GSth}$ spread, the current rise time $t_{cr}$ persists until the drain current of the device has reached the load current value. In the cases of narrow $V_{GSth}$ spread, $t_{cr}$ lasts earlier because the devices having $V_{GSth\ max}$ start conducting part of the load current. At turn-off, the GaN FETs with $V_{GSth\ max}$ start to carry less current earlier than GaN FET (A). The current that these devices do not carry anymore is diverted to GaN FET (A) causing a drain current peak. The parasitic output capacitances contribute to increasing the current peak in the most stressed GaN FET. In a parallel connection, the parasitic output capacitances ($C_{oss}$=$C_{GD}$+$C_{SD}$) of all the devices with $V_{GSth\ max}$ provide a current for the time duration of the drain voltage transition (Burkard & Biela, 2019). At turn-off, the current still carried by GaN FETs with $V_{GSth\ max}$ sets the current peak on the GaN FET that turns off later. The presence of the source inductance $L_S$ lowers the current peak but extends the commutation time, increasing switching losses. These conclusions are obtained by performing simulations varying some parameters and maintaining others constant (cases of studies A, B and C). In the case of studies A and B, the attention points to the influence of the number of devices N when a specific load current demand $I_{load}$ is given. Case B shows how the common source inductance $L_S$ acts during the switching transient of GaN FETs as a comparison with the case A, where $L_S$ is null. The focus of the C case is on the impact of the amount of drain current required from each individual device on the GaN FET with the lowest threshold voltage. In this latter case, the number of devices N remains constant, while the load current $I_{load}$ demand is varied.

The comparison between the maximum and reduced threshold voltage spread conditions is investigated in all cases.

### *Constant Load Current and Different Number of Parallel-connected GaN FETs – Without Source Inductances*

In this section, the analysis with N devices in the number range 2–8 is considered. In this case the common source inductances are neglected. Fig. 5 shows the drain currents of the most stressed device current peak of the different numbers of the paralleled GaN FETs. The waveform is obtained considering a total load current equal to $I_{load} = 50\ A$ with N GaN FETs in parallel connection. As the number of devices grows, the load current is shared between more devices. In this way, less current is

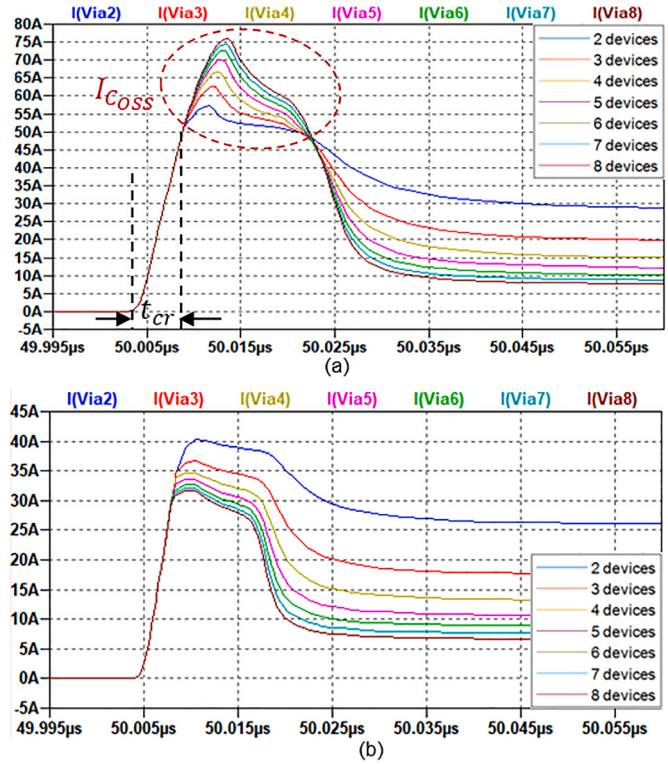


**Fig. 5.** Drain current of GaN FET with $V_{GSth\ min}$. $I_{load} = 50\ A$ supplied by N from 2 to 8 GaN FETs in parallel connection. Neglected $L_S$. Turn-on. Maximum (a) and reduced (b) $V_{GSth}$ spread. 5 A/div. Reduced $V_{GSth}$ spread allows $\frac{dI_{D\ A}}{dt} \cdot t_{cr} < I_{load}$ and lower $I_{D\ A\ pk\ (turn-off)}$.

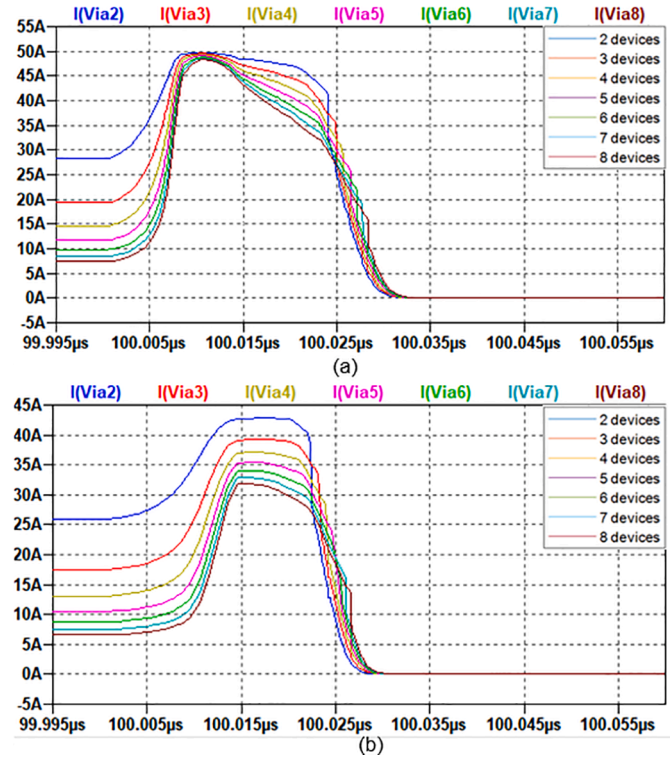


**Fig. 6.** Drain current of GaN FET with $V_{GSth\ min}$. $I_{load} = 50\ A$ supplied by N from 2 to 8 GaN FETs in parallel connection. Neglected $L_S$. Turn-off. Maximum (a) and reduced (b) $V_{GSth}$ spread. 5 A/div. Reduced $V_{GSth}$ spread allows $\frac{dI_{D\ A}}{dt} \cdot t_{cr} < I_{load}$ and lower $I_{D\ A\ pk\ (turn-off)}$.

carried out by devices during the conduction phase. The peak current of the most stressed device (A) $i_{D\ A}$ is shown at turn-on (Fig. 5a and b) and turn-off (Fig. 6a, and b). In Figs. 5a and 6a the maximum $V_{GSth}$ spread is considered. While in Figs. 5b and Fig. 6b the reduced $V_{GSth}$ spread is investigated. In Figs. 5 and 6 the increase of N is responsible for the increase of the sum of $C_{OSS}$ ($N$-1 parasitic capacitors) currents as described in (3),( $I_{Coss}$ in Fig. 5a). During turn-on, GaN FET A $i_{D\ A}$ reaches the total load current value after $t_{cr}$ and then it became higher as a consequence of the $C_{OSS}$ currents. At turn-on this current reaches the load current value. With reduced $V_{GSth}$ spread, $t_{cr}$ is shorter and the peak current decreases under $I_{load}$ when N increases, as highlighted in Fig. 5b compared with Fig. 5a. During the turn-off, GaN FETs with $V_{GSth\ max}$ still carry more current if the $V_{GSth}$ spread is lower and then the device with $V_{GSth\ min}$ carries a minor current peak (see Fig. 6a and b).

### *Constant Load Current and Different Number of Parallel-connected GaN FETs – With Source Inductances*

The comparison between the operating conditions of N parallel-connected GaN FETs varying in the range 2–8 when an $L_S$=200 nH is connected to the source of each device is analysed in this section. The drain current of the device having $V_{GSth\ min}$ when all devices supply $I_{load}$=50 A is reported in Figs. 7a and 8a for the maximum $V_{GSth}$ spread case and Figs. 7b and 8b for the reduced one. Fig. 7 refers to the turn-on transient while Fig. 8 refers to the turn-off.

Similarly to case A discussed above, the reduction of the $V_{GSth}$ spread causes the GaN FET with $V_{GSth\ min}$ to have peak currents below the $I_{load}$ value in both transient commutations. A comparison between the waveforms in case A and case B shows that the presence of $L_S$ slows down both current switching dynamics. At turn-on, comparing Figs. 7 and 5, this slowing down can be observed by a lower rising slope of the drain current waveforms and the wider $t_{cr}$ current rising range. In

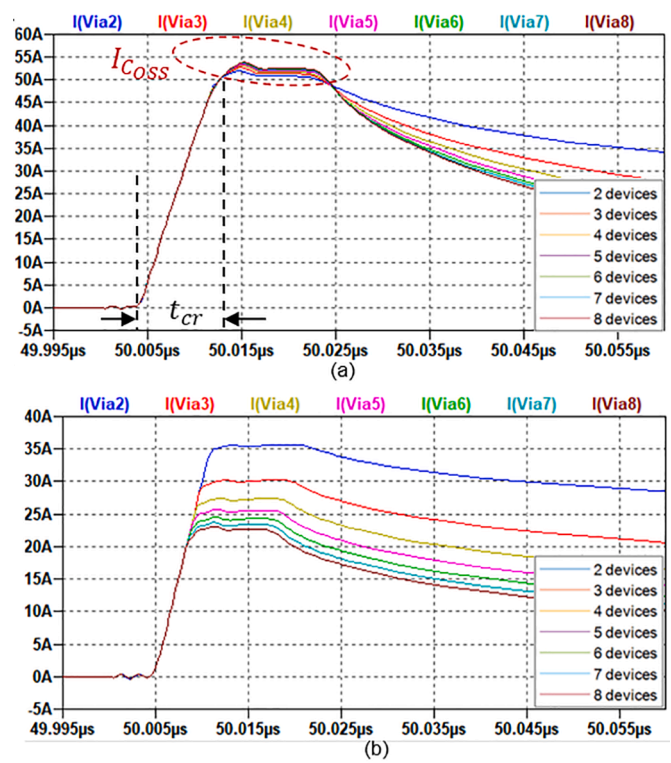


**Fig. 7.** Drain current of GaN FET with $V_{GSth\ min}$. $I_{load} = 50\ A$ supplied by N from 2 to 8 GaN FETs in parallel connection. $L_S$=200 pH. Turn-on. Maximum (a) and reduced (b) $V_{GSth}$ spread. 5 A/div.

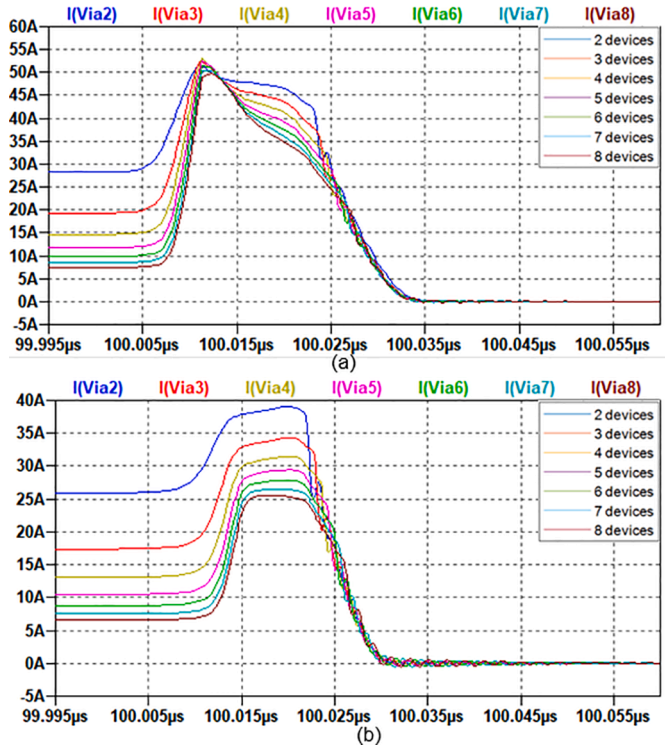


**Fig. 8.** Drain current of GaN FET with $V_{GSth\ min}$. $I_{load} = 50\ A$ supplied by N from 2 to 8 GaN FETs in parallel connection. $L_S$=200 pH. Turn-off. Maximum (a) and reduced (b) $V_{GSth}$ spread. 5 A/div.

addition, capacitive current contributes less to the GaN FET A current peak if Ls is present. Comparing the turn-off transients in Figs. 8 and 6, focusing on the interval before the peak, the current value is lower in the case with $L_S$. In addition, ringing in the current tail are present due to the presence of $L_S$ and the parasitic capacitances of the GaN FET.

*Eight Parallel-connected GaN FETs Working for Several Values of Drain Current*

In this case, simulations with 8 GaN FETs in parallel connection are carried out. They differ for the value of the load current. It is calculated as

$$I_{load} = N \cdot I_D \tag{4}$$

with $I_D$ varying at values 8 A, 15 A, 20 A, and 25 A.

The Figs. 9 and 10 show the drain current $I_D$ waveform of the GaN FET with the lowest threshold voltage and the drain voltage $V_{DS}$ (in green and Bordeaux respectability). The turn-on commutation is depicted in Fig. 9a and b. The turn-off commutation is reported in Fig. 10a and b. In Figs. 9a and 10a the maximum $V_{GSth}$ spread is considered. While In Figs. 9b and 10b the reduced $V_{GSth}$ spread is investigated.

Looking at the current waveforms in Figs. 9 and 10, the current reaches the expected value when the device is on the on-state. A non-equal current sharing happens during commutations because of the threshold voltage spread. It causes a current peak on the (A) device with a lower threshold voltage.

The rising current slope is different according to the minimum threshold voltage value. In the case of $V_{GSth\ min} = 0.95\ V$, it is lower than the case with $V_{GSth\ min} = 0.7\ V$.

The transconductance of the GaN FET is described as (Burkard & Biela, 2019)

$$I_{D\ n} = g_m \cdot (V_{GS} - V_{GSth}) \tag{5}$$

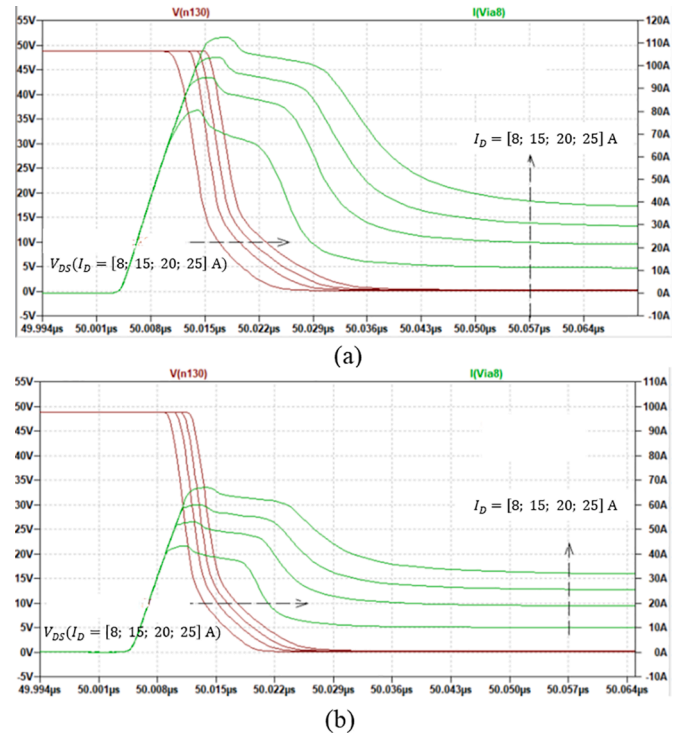


**Fig. 9.** Eight GaN FETs in parallel connection. Waveforms of the GaN FET with $V_{GSth\ min}$. Drain current in green and drain voltage in Bordeaux; Drain current $I_D$ at values 8 A, 15 $A$, 20$A$, 25 $A$. Turn-on. Maximum (a) and reduced (b) $V_{GSth}$ spread.

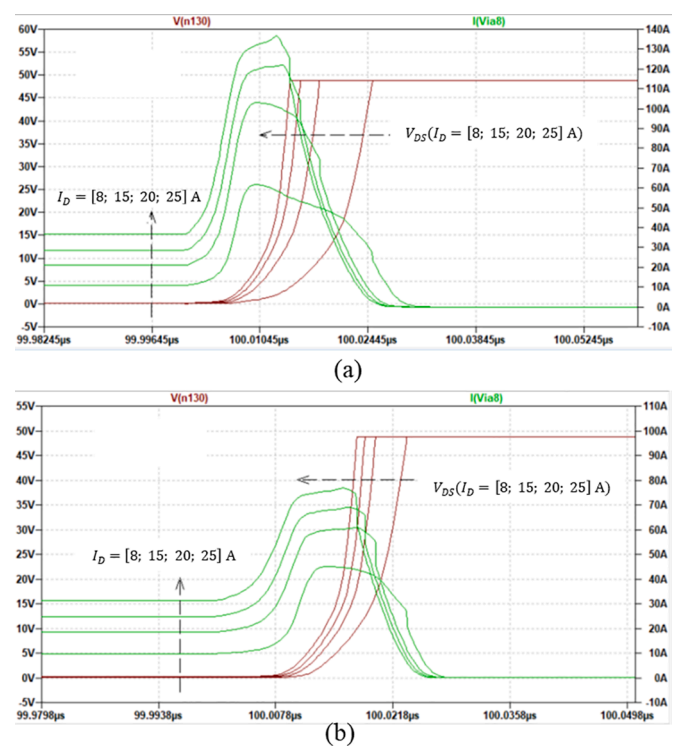


**Fig. 10.** Eight GaN FETs in parallel connection. Waveforms of the GaN FET with $V_{GSth\ min}$. Drain current in green and drain voltage in Bordeaux; Drain current $I_D$ at values 8 A,15 $A$, 20$A$, 25 $A$. Turn-off. Maximum (a) and reduced (b) $V_{GSth}$ spread.

where $g_m$ is the transconductance gain. At the same $V_{GS}$, the quantity $(V_{GS} - V_{GSth})$ is smaller when the $V_{GS\ th}$ is the biggest. In this way, the current derivate is higher as $V_{GS\ th}$ is smaller. In the examples considered, it is $\frac{di_{D\ A}}{dt} = 11.6$ A/ns for the $V_{GSth\ min} = 0.7\ V$ case (Fig. 9a) and $\frac{di_{D\ A}}{dt} = 10$ A/ns for the $V_{GSth\ min} = 0.95\ V$ one (Fig. 9b). These values don't change between the simulations at 8 A, 15 A, 20 A or 25 A drain current.

The value of the current request acts on the duration of the rising current. This time is longer if the current demand is high. The current rise time $t_{cr}$ ends in correspondence with the start to change (fall-time) in drain-source voltage $V_{DS}$.

This voltage variation on the parasitic output capacitors creates an additional current $I_{C_{OSS}}$ in the circuit, involving the GaN FET with $V_{GSth\ min}$.

The combination of these two effects determines the drain current peaks. The turn-off peak is more dangerous than the turn-on one when the current request is high. Moreover, the restriction of the $V_{GSth}$ spread reduces the current peaks and their duration.

### Maximum Junction-to-ambient Delta-temperature

The GaN FET used in this paper has an absolute maximum rating of the junction temperature of 150 °C. The switching energy losses $E_{sw}$ of the GaN FET with $V_{GSth\ min}$ increases with the $V_{GSth}$ spread (J. Lu, Hou & Chen, 2018). In some inverter applications that require a high power level and high switching frequency, the thermal limit may be reached. Simulations demonstrated that the presence of parasitic source inductances $L_s$ causes a lower current peak at the cost of a higher energy $E_{sw}$ due to a longer commutation time. As examples, the cases without $L_s$ and with $L_s = 200\ pH$ are compared. A thermal junction-to-ambient resistance $R_{\theta JA} = 10\ \frac{°C}{W}$ is considered. The $R_{\theta JA}$ is obtained using a passive air heatsink. Starting from the voltage and current waveforms, the trend of losses over time is achieved. Since the losses and $R_{\theta JA}$ of the GaN are known, the lost energies and the junction-to-ambient temperature variation are obtainable. The focus is on the GaN FET with $V_{GSth\ min}$, named (A), because it is the most stressed and it has the highest losses.

The maps that represent the maximum junction-to-board delta-temperature as a function of the number $N$ of parallel-connected GaN FETs and the switching frequency $f_{sw}$ are obtained in the case of a constant load current $I_{load}$ supplied by all the GaN FETs. Several simulations have been carried out for N from 2 to 8 parallel-connected devices and at various switching frequencies (from $f_{sw} = 10\ kHz$ to $f_{sw} = 200\ kHz$). The worst-case in which only the (A) GaN FET has threshold voltage $V_{GSth\ min}$ while all the other devices have the maximum one $V_{GSth\ max}$is considered in two cases of maximum $V_{GSth}$ spread ($V_{GSth\ min} = 0.7\ V$; $V_{GSth\ max} = 2.5\ V$) and reduced ($V_{GSth\ min} = 0.95\ V$; $V_{GSth\ max} = 1.8\ V$).

In this section, the delta-temperature maps of the (A) GaN FET $\Delta\theta_{JA}$ obtained with drain current $I_{load} = 90\ A$ are depicted in Fig. 11 for the case without $L_s$ and in Fig. 12 for the case with $L_s = 200\ pH$. The cases of maximum $V_{GSth}$ spread are shown in Figs. 11a and 12a. The cases of reduced $V_{GSth}$ spread are shown in Figs. 11b and 12b.

The cause of the increase in temperature is due to two types of losses: conduction losses $E_{cond}$ and switching losses $E_{sw}$. The first type depends on the drain current conducted $I_D$, (on-state), while the commutation ones depend on all the switching current. Hence a higher $V_{GSth}$ spread results in higher $E_{sw}$.

An increase in switching frequency causes commutations to be repeated several times over time and reduces the duration of a single conduction period. It means that the losses due to the $V_{GSth}$ spread and the resulting increase in temperature are predominant at high switching frequencies.

At constant $I_{load}$, growing the number of parallel connected GaN FETs results in a lower conduction current level requested to each device during the on-state. However, during commutations the GaN FET (A) current feature a higher current peak as the $V_{GSth}$ spread is wide.

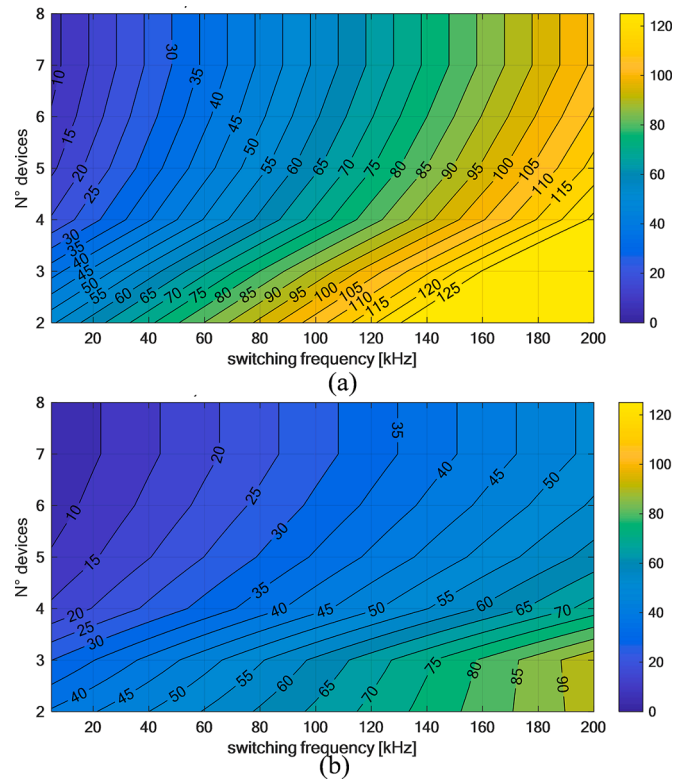


**Fig. 11.** junction-to-ambient delta-temperature [ °C] of the most stressed GaN FET. Map in function of the switching frequency and number of parallel-connected devices. $I_{\text{load}}$=90 $A$. Without $L_s$. $R_{\theta JA} = 10\ \frac{°C}{W}$. $f_{sw} = 20\ kHz/div$. Maximum (a) and reduced (b) $V_{GSth}$ spread.

The comparison of the maps in Figs. 11 and 12 shows that the delta-temperature differences between the maximum (Figs. 11a and 12a) and reduced (Figs. 11b and 12b) $V_{GSth}$ spread cases are most evident at high $f_{sw}$, where $E_{sw}$ predominate over conduction losses $E_{cond}$.

The comparison of the maps without source inductance $L_s$ in Fig. 11 and with $L_s = 200\ pH$ in Fig. 12 shows that in the case with source inductances temperatures are higher, especially at high frequency and at a low number of devices. With $L_s$ the switching transient lasts longer and switching losses are higher than in the case without source inductances. For this reason, the transition from low to high switching frequencies results in a higher increase in temperature as $L_s$ is significant. As the number of devices increases the current from $C_{oss}$ at turn-on increases, but occurs during the switching period. So, even when Ls is zero, the effect on switching losses is small.

In Fig. 13 the isothermal curves at $\Delta\theta_{JA} = 50°C$ for load current $I_{load}$ values (blue) 65 A; (red) 90 A; (magenta) 120 A; (green) 140 A are shown. Continuous curves refer to the maximum $V_{GSth}$ spread case and dashed curves refer to the reduced $V_{GSth}$ spread case.

Energy $E_{sw}$ increases with both the $V_{GSth}$ spread and the source inductance $L_s$ value.

Iso-temperature curves referring to higher load current are placed at lower switching frequencies. This is due to the higher conduction losses that are the cause of a higher delta-temperature. Iso-temperature curves are limited to lower $f_{sw}$ as the $N$ (parallel devices) increases, whatever is the considered $V_{GSth}$ spread.

When comparing the two analyzed spread cases (typical and maximum), at low $f_{sw}$, the value of the delta-temperature is almost the same for both cases. At high $f_{sw}$ the higher delta-temperature is reached if the $V_{GSth}$ spread is maximum or $L_s$ is high. The system is less thermally stressful if the current that the device has to conduct is smaller.

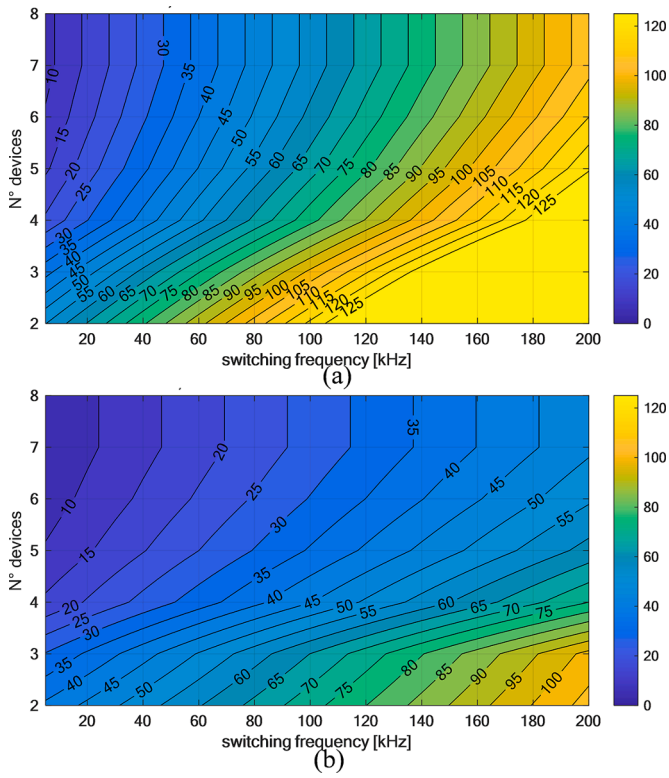


**Fig. 12.** junction-to-ambient delta-temperature [ °C] of the most stressed GaN FET. Map in function of the switching frequency and number of parallel-connected devices. $I_{\text{load}}$=90 $A$. With $L_s = 200\ pH$. $R_{\theta JA} = 10\ \frac{^\circ C}{W}$. $f_{sw} = 20\ kHz/div$. Maximum (a) and reduced (b) $V_{GSth}$ spread.

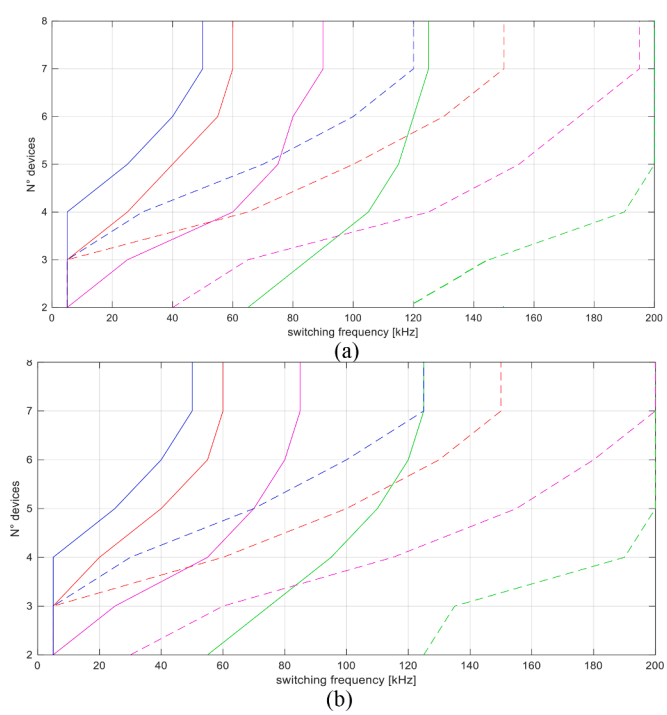


**Fig. 13.** 50 °C isotemperature curves in the switching frequency versus the number of devices N. (a) without $L_s$; (b) with $L_s = 200\ pH$. $R_{\theta JA} = 10\ \frac{^\circ C}{W}$. $f_{sw} = 20\ kHz/div$. Constant $I_{\text{load}}$: (blue) 65 A; (red) 90 A; (magenta) 120 A; (green) 140 A. Continuous lines for the maximum $V_{GSth}$ spread condition and dashed lines for the reduced $V_{GSth}$ spread condition.

## Conclusions

The performed analysis gives the theoretical guidelines for a correct choice of the number of GaN FETs to connect in parallel. The main parameter investigated is the $V_{GSth}$ spread. Based on the simulation results, the parallel connection is optimized considering the reduced spread $V_{GSth}$.

The current peak at turn-on and turn-off is evaluated at a different number of paralleled devices. The peak current is reduced by the source inductance Ls. On the other hand, the effect of $L_s$ on the junction temperature $\Delta\theta_{JA}$ of the device is smaller than the spread of $V_{GSth}$ due to the longer switching time (see Figs. 4, 6, and 12). A better current share and thermal management may be achieved by selecting devices from the same production lot. When working at high $f_{sw}$ it is best to keep conduction losses very low to compensate for the switching losses. It is achievable to use more parallel-connected devices that supply the load current requesting to conduct fewer drain currents for each one. Also reducing the $V_{GSth}$ spread of devices in advance allows to an increase in switching frequency

Given the operative conditions of switching frequency, load current, and acceptable delta temperature of devices, an appropriate number of GaN FETs to be connected in parallel can be selected by choosing a value between the maximum and reduced $V_{GSth}$ spread curves of the thermal map achieved. For example, four devices connected in parallel may be sufficient to supply a 90 A load current at $f_{sw} = 100\ kHz$ without that devices exceed 50 °C delta temperature (see Fig. 13).

In future work, a board with a very large number of paralleled GaN FET will be tested to demonstrate experimentally the capability and limitations of the parallel connection.

## Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Data availability

Data will be made available on request.

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