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***Abstract*— This paper present a two-stage Doherty power amplifier designed to maximize the efficiency at 6 dB back-off while minimizing the complexity in terms of bias voltages. The amplifier has been manufactured on a GaN-SiC 150 nm monolithic microwave integrated circuit technology. The fabricated chip, measured in continuous wave conditions, maintains a linear gain higher than 13 dB, a saturated output power in excess of 34 dBm, with a power-added efficiency higher than 20 % both at saturation and at 6 dB output back-off, over the 14.5 GHz–17.25 GHz band, favorably comparing with the present state of the art for similar applications.**

***Keywords*— Gallium Nitride, Doherty power amplifier, MMIC, high efficiency.**

I. Introduction

The exploitation of microwave and millimeter-wave bands for mass communications, initially foreseen for 5G and currently in expansion for the future 6G applications, is pushing the development of high efficiency power amplifiers with multi-gigahertz bandwidths [1].

The Doherty Power Amplifier (DPA) [2], successfully adopted in the sub-6 GHz frequency range, is very promising also in this new scenario, if supported by technology. Under this aspect, Gallium Nitride (GaN) is an ideal candidate, thanks to the large power density allowing to reach on-chip several watts of power. From a design standpoint, the low capacity per millimeter of GaN (similar to Gallium Arsenide (GaAs)) results favorable especially because it allows to realize simple and wideband matching networks [3]. On the other hand, only recently Monolithic Microwave Integrated Circuits (MMIC) processes with gate lengths of the order of 150 nm or less, sufficient to assure reasonable gain of the active devices in K-bands, are appearing [1].

Demonstrators of Ku- to Ka-band DPAs are available in the literature, both in Silicon-On-Insulator Complementary Metal Oxide Semiconductor (SOI-CMOS) [4] and in compound semiconductors [5], [6], [7], [8], with different power levels and architecture complexity. Focusing on the compound scenario, the first examples at these frequencies were developed as single stages and covering narrow bands, whereas the present trend is toward the challenge of realizing sufficient gain (asking for multi-stage architectures) and to cover multi-gigahertz bands.

This paper presents a two-stage MMIC DPA manufactured adopting the 150 nm gate length GaN-SiC High Electron Mobility Transistor (HEMT) process of WIN semiconductors. The DPA is designed minimizing the number of distinct bias voltages, and making it suitable to different applications thanks to the adoption of different bias conditions with analogous complexity. The MMIC delivers more than 34 dBm of saturated output power in the 14.5–17.25 GHz band, with a linear gain in excess of 13 dB and a Power-Added Efficiency (PAE) higher than 20 % both at saturation and at 6 dB of Output Back-Off (OBO), over the whole band. The presented DPA favorably places itself among the present state of the art for similar frequency range and power, showing the highest relative bandwidth and competitive efficiency performance.

II. Design

The DPA is a symmetrical two-stage architecture embedding drivers in each branch of the Doherty configuration. Both drivers and power devices of the main and auxiliary branches have the same size, namely $4\times75\,\mu$m for the drivers and $6\times100\,\mu$m for the power devices, to enhance symmetry thus easing wideband operation and to maximize the power utilization of the auxiliary power device.

The output combiner includes a $\lambda/4$ impedance inverter on the main and two $\lambda/4$ sections with different characteristic impedances on the auxiliary. The output parasitic effects of the $6\times100\,\mu$m devices are resonated out at the drain plane by means of RF-short-circuited stubs, which are also used as drain supply lines. This combiner topology allows to set the common node impedance to $50\,\Omega$, thus avoiding additional post-matching and minimizing size and losses.

The inter-stage matching networks are high order filters and adopt the same topology on the two branches. They are designed to transform the input impedance of the power devices, including their stabilization RC network, to the drivers' optimum load.

The input matching networks are designed to minimize reflections at the input, assuming a $50\,\Omega$ input impedance, and the power splitter, based on a Lange hybrid coupler designed on $50\,\Omega$, divides the power evenly between the two branches.

The microscope photograph of the manufactured chip, brazed on a brass carrier and DC- and RF-probed for successive characterization, is shown in Fig. 1.

The input and inter-stage matching networks are optimized considering the impedance levels in saturation condition, i.e., when the devices biased in class C are already on, in order to maximize the performance in the Doherty region, and to make the architecture reconfigurable in terms of gate bias voltage levels. In particular, aiming at minimizing the number

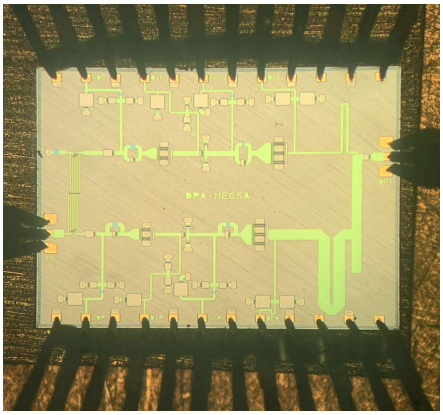


Fig. 1. Microscope photograph of the fabricated Doherty MMIC; the area is 3.6x2.9 mm^2.

of different voltages required for the chip to operate, two alternative bias conditions have been considered, both adopting only two distinct gate voltages.

The first assumes that both drivers and the main power device are biased in the same class-AB condition, which is selected for the desired trade-off between gain, efficiency, and phase distortion, and the auxiliary power device is biased in class C, in such a way to ensure the proper turn-on. This condition is referred to as ABAB-ABC. This bias condition maximizes the input matching, since biasing the auxiliary driver in class AB minimizes the unbalance between the Lange output ports, and the gain flatness, but it may be sub-optimal in terms of efficiency and saturated output power. In fact, since the auxiliary power device has to be biased in a relatively deep class C, it is difficult to maximize the back-off efficiency peak while ensuring that the full current is provided at saturation, i.e., the full output power is provided. A trade-off of these two requirements typically implies a lower back-off efficiency to maintain the optimum saturated performance.

The second considered condition, named ABAB-CC, assumes the main devices in the same class-AB condition, selected as above, and the two auxiliary devices in the same class-C condition, optimized to ensure the best trade-off between the proper turn-on point and the required full current swing at saturation. Conversely, this condition is slightly sub-optimal in terms of input matching, since the output ports of the Lange coupler are terminated on quite different impedances, and gain flatness, since the auxiliary turn-on is usually slower. On the other side, this allows to maximize the first efficiency peak, despite renouncing to the additional degree of freedom of adopting different class-C bias voltages, without compromising the performance at saturation. In fact, the auxiliary power device is biased at a shallower class C, thus easing the reach of the full current swing at saturation.

III. Experimental Characterization

The manufactured DPA has been characterized on-wafer, in small and large signal. The characterization has been performed under the two operating conditions introduced in

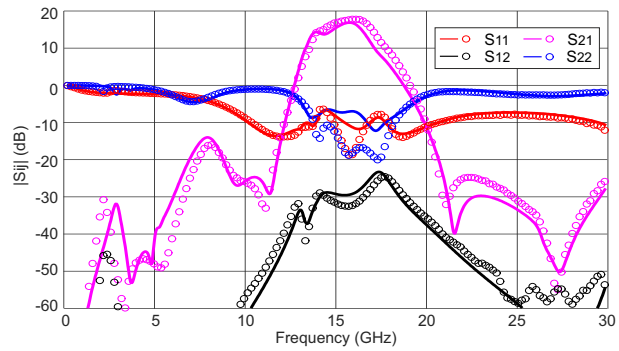


Fig. 2. Comparison of simulated (solid) and measured (symbols) scattering parameters in the frequency range 0.1–30 GHz for the nominal ABAB-CC bias conditions.

Sec. II, adopting the minimum number of different bias voltages for the selected architecture.

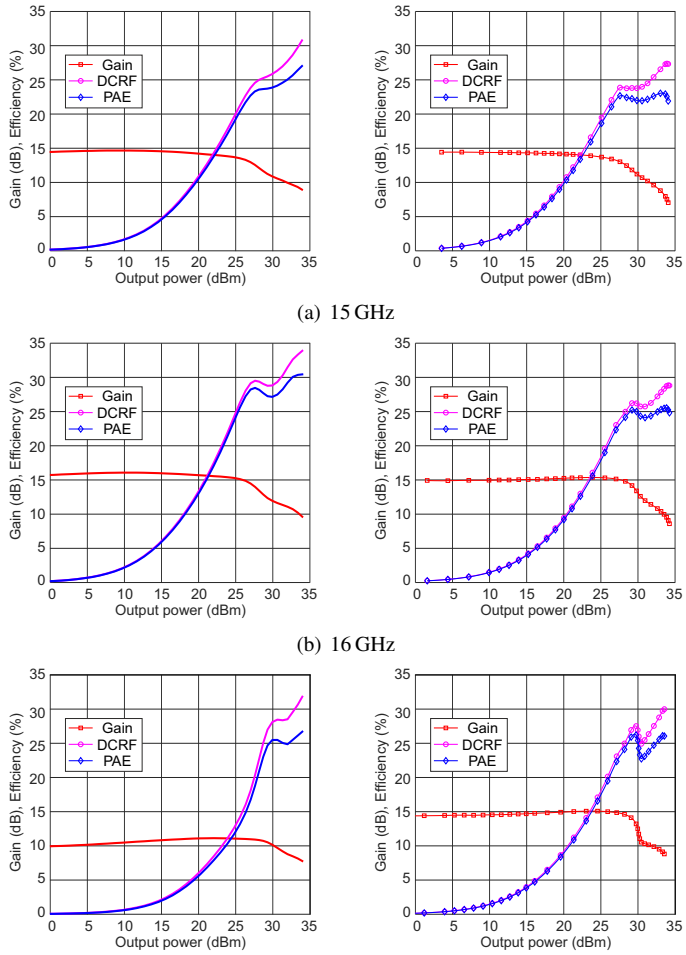
The results reported below all refer to the following ABAB-CC operating condition: V_{GMd}=V_{GM}=-2 V, V_{GAd}=V_{GA}=-2.6 V, V_{DD}=20 V, I_{D}=30 mA, i.e., corresponding to a 25 mA/mm class AB for the main branch and the same class C condition for the two devices in the auxiliary branch.

The simulated and measured scattering parameters performed in analogous operating conditions (i.e., applying a -0.2 V shift to all gate voltages from simulation to measurement, to equalize the class AB drain current accounting for the difference in the threshold voltage of the transistors) are reported in Fig. 2. They are quite in good agreement, except for a slight shift of the measured S_{21} to higher frequencies compared to the simulated one, and a difference in the output reflection coefficient (S_{22}) level in the operating frequency range, possibly due to an inaccurate modeling of the microstrip-coplanar waveguide transition. The measured scattering parameters show input and output matching better than 7 dB and gain higher than 14 dB from 14 dB to 17 GHz.

The simulated and measured continuous wave (CW) power sweeps are shown in Fig. 3 at 15 GHz, 16 GHz, and 17 GHz, for the same operating conditions already described. A good agreement is maintained also in large signal, apart from a slight shift of the gain cutoff towards higher frequencies experienced in the measurements, already observed in the small signal characterization. The proper Doherty load modulation is confirmed by the shape of the efficiency curve across the whole frequency range.

The measured large signal performance is summarized in Fig. 4 and compared to other MMIC PAs working at similar frequencies in Table 1. This DPA maintains small signal gain and saturated output power in excess of 13 dB and 34 dBm from 14.5 GHz to 17.25 GHz, with a power-added efficiency (PAE) higher than 20 % both at saturation and at 6 dB OBO. This performance compares well with the state of the art (SOA), featuring the widest relative bandwidth and competitive efficiency levels, especially when compared to narrowband designs.

The characterization performed with the alternative bias



(a) 15 GHz

(b) 16 GHz

(c) 17 GHz

Fig. 3. Simulated (left, solid) and measured (right, symbols) CW power sweeps at three selected frequencies.

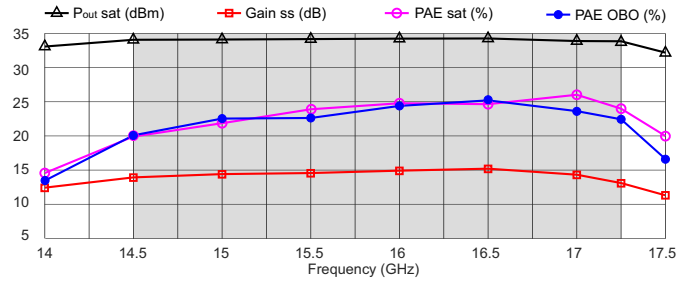


Fig. 4. Measured CW large signal performance versus frequency, from 14 GHz to 17.5 GHz in 0.5 GHz steps.

configuration (ABAB-ABC, with V_{GMd}=V_{GM}=V_{GAd}=-2 V, V_{GA}=-3.3 V), not reported here for brevity, has returned comparable saturated output power and linear gain, with a small unbalance between the two efficiency peaks, the PAE resulting a few percentage points higher and lower at saturation and OBO, respectively, than in the ABAB-CC condition. This proves that the proposed DPA can be suitably employed adopting either of the two bias conditions, depending on the convenience for the specific application, without added complexity for the system in terms of number of bias paths.

Table 1. Comparison with SOA K-band DPAs.

Tech.	Freq (GHz)	BW %	P_{out} (dBm)	PAE (%)	PAE 6 dB (%)	Gain (dB)	Ref.
CMOS	14–16	13.3	25	25	21	25	[4]
GaAs	15	-	27	41	34	17	[5]
GaN	13.7–15.3	11	35	29	16	8	[6]
GaN	20	-	35	37	18	25	[7]
GaN	26-30	14.2	36	26	25	11	[8]
GaN	**14.5–17.25**	**17**	**34**	**20**	**20**	**13**	**T.W.**

IV. Conclusion

This paper has presented the design and characterization of a GaN MMIC DPA with minimized bias voltage complexity, for applications around 15 GHz. The manufactured DPA has a 17 % relative bandwidth, maintaining saturated output power higher than 34 dBm and PAE higher than 20% both at saturation and at 6 dB OBO from 14.5 GHz to 17.25 GHz. This performance compares well with the state of the art at similar frequencies.

Acknowledgments

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References

[1] V. Camarchia, R. Quaglia, A. Piacibello, D. P. Nguyen, H. Wang, and A.-V. Pham, "A Review of Technologies and Design Techniques of Millimeter-Wave Power Amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2957–2983, 2020.

[2] A. Grebennikov and S. Bulja, "High-efficiency Doherty power amplifiers: Historical aspect and modern trends," *Proc. IEEE*, vol. 100, no. 12, pp. 3190–3219, Dec. 2012.

[3] A. Piacibello and V. Camarchia, "Ka-band MMIC GaN Doherty Power Amplifiers: Considerations on Technologies and Architectures," in *2021 IEEE MTT-S International Wireless Symposium (IWS)*, 2021, pp. 1–3.

[4] N. Rostomyan, J. A. Jayamon, and P. M. Asbeck, "15 GHz Doherty Power Amplifier With RF Predistortion Linearizer in CMOS SOI," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 3, pp. 1339–1348, 2018.

[5] M. Darwish and A.-V. Pham, "Compact and high efficiency Doherty power amplifier using a new modulation load range," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, 2017, pp. 782–784.

[6] R. Quaglia, V. Camarchia, J. J. Moreno Rubio, M. Pirola, and G. Ghione, "A 4-W Doherty Power Amplifier in GaN MMIC Technology for 15-GHz Applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 4, pp. 365–367, 2017.

[7] V. Valenta, I. Davies, N. Ayllon, S. Seyfarth, and P. Angeletti, "High-gain GaN Doherty power amplifier for Ka-band satellite communications," in *2018 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, 2018, pp. 29–31.

[8] Y. Yamaguchi, K. Nakatani, and S. Shinjo, "A Wideband and High Efficiency Ka-band GaN Doherty Power Amplifier for 5G Communications," in *2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2020, pp. 1–4.