# Efficiency versus linearity trade-off in an S-band class-AB power amplifier

# Efficiency versus linearity trade-off in an S-band class-AB power amplifier

Zhifan Zhang[1], Anna Piacibello[2], Vittorio Camarchia[3]
Department of Electronics and Telecommunications, Politecnico di Torino, Torino, Italy
[1]zhifan.zhang@studenti.polito.it, {[2]anna.piacibello, [3]vittorio.camarchia}@polito.it

***Abstract*—This paper presents a design strategy to simultaneously optimize the efficiency and linearity of a single-device class-AB power amplifier, given minimum output power and gain requirements. The adopted linearity metric is the highest inter-modulation distortion in a two-tone test with 20 MHz spacing. The simultaneous selection of optimum source and load terminations that provide the best trade-off among all of the requirements is described in detail, and the synthesis of the matching networks is then presented. A prototype is developed based on a 6 W packaged GaN device around 3.5 GHz, manufactured and measured. According to the measured results, the amplifier achieves output power higher than 38 dBm with associated gain higher than 12 dB and saturated power-added efficiency in excess of 73% in a single-tone test at 3.25 GHz, while providing a 33% power-added efficiency and -30 dBc inter-modulation distortion in the 20 MHz two-tone test.**

***Index Terms*—GaN, high efficiency, intermodulation, linearity, power amplifiers.**

## I. Introduction

The Power Amplifier (PA) is one of the bottlenecks in determining the performance of wireless transmitters, both for space and ground applications, in terms of energy efficiency and linearity. During the design phase, the intrinsic linearity of the PA is often considered a less stringent requirement compared to output power, operating bandwidth, gain, etc. This is especially true when the targeted application allows for the adoption of linearization solutions, such as predistortion [1] or dual-input architectures, that allow to enhance linearity and make it compatible with the standards. However, there are cases where it is essential to design a PA intrinsically compliant to quite stringent linearity requirements.

This paper presents a design strategy to maximize efficiency while simultaneously maintaining stringent output power and linearity constraints in a single-device class-AB power amplifier. The adopted linearity metric is the power of the highest inter-modulation distortion (IMD) product in a two-tone test with 20 MHz tone spacing [2]. Although the recent trend is towards the adoption of system level metrics, such as adjacent channel power ratio or noise-to-power ratio [3], the two-tone metrics are more easily estimated during the design and thus still provide a useful initial estimation of the PA linearity. The adopted design methodology is based on source and load pull simulations, at fundamental and second harmonic frequencies, aided by the identification of the parameters to which each of the targeted performance is more sensitive. The measurements on the realized prototype amplifier show performance in line with the targeted one, despite the presence of a frequency shift. It achieves output power higher than 38 dBm and saturated efficiency in excess of 80% in a single-tone test at 3.25 GHz, with a 40% power-added efficiency (PAE) at the -30 dBc third-order (IMD3) point in the corresponding 20 MHz two-tone test.

## II. Project aims and requirements

The specifications adopted for this design are inspired to those of the IMS 2022 Student Design Competition on High Efficiency PAs. The PA should satisfy two main requirements:

1) achieve an output power ($P_{\mathrm{out},f_0}$) in the range 4–40 W for a single-carrier drive at frequency $f_0$ with input power ($P_{\mathrm{in},f_0}$) not higher than 24 dBm.
2) maintain the highest inter-modulation product below -30 dBc in a two-tone measurement with 20 MHz tone spacing and maximum input power ($P_{\mathrm{in,2t}}$) of 21 dBm per tone, while achieving a PAE as high as possible.

Therefore, the strategy to trade off linearity and efficiency while maintaining sufficient output power is crucial. Lately, a promising architecture to satisfy these contrasting requirements has proven to be the Doherty PA [4], thanks to the beneficial effect of the Auxiliary amplifier in compensating the amplitude-to-phase distortion (AM/PM) of the Main, if a specific design strategy is adopted. However, class-AB PAs have proven to be competitive [5].

This work aims at assessing the highest performance achievable by a single-stage class-AB PA in this framework, especially as the modulation bandwidth increases as the recent trend has evidenced.

## III. Design

The class-AB PA is designed at $f_0$=3.5 GHz, compatibly with a hybrid implementation targeting 5G applications, optimizing the matching networks over a 500 MHz bandwidth.

The 6 W packaged Wolfspeed GaN HEMT (CGH40006P) is selected for a hybrid implementation, as it provides sufficient output power to reach the target 36 dBm while featuring high efficiency and good linearity. An input stabilization circuit ensuring unconditional stability in and out of the band is designed. It includes a parallel RC (150 Ω ∥ 1.2 pF) block connected to the gate of the transistor and a shunt R (120 Ω) along the gate bias path. The stability is verified at several bias conditions, foreseeing a gate bias voltage around class-B and deep class-AB (i.e., ranging between -3.2 V and -2.9 V)

to exploit the IMD3 sweet spots [6] thus trading off between gain, efficiency, and linearity.

After stabilizing the active device, simultaneous optimization of the source and load terminations is needed to satisfy all requirements. Given the choice of the operating frequency and the maximum frequency of operation of the packaged transistor, the terminations are optimized only up to the second harmonic. Higher harmonics have been verified to have a negligible effect on the performance in the targeting frequency. The termination will be referred to in the following as source ($\Gamma_{\mathrm{S}}$) and load ($\Gamma_{\mathrm{L}}$) reflection coefficients, relative to a 50 $\Omega$ normalization impedance, at either baseband (bb), fundamental ($f_0$), or second harmonic ($2f_0$).

A first down-selection of the $\Gamma_{\mathrm{L},f_0}$ region of interest is based on the $P_{\mathrm{out},f_0}$ requirement. The selection of the optimum load will be based on a trade-off with the IMD3 and PAE requirements. Achieving the desired performance within the allowed input power range poses a constraint on gain, which is then mainly determined by the input matching section. The IMD3 is only slightly affected by the choice of $\Gamma_{\mathrm{S},f_0}$, instead strongly influenced by $\Gamma_{\mathrm{L,bb}}$, which in turn has a negligible effect on $P_{\mathrm{out},f_0}$, gain, and PAE. Finally, the second harmonic terminations $\Gamma_{\mathrm{L},2f_0}$, $\Gamma_{\mathrm{S},2f_0}$ affect the efficiency performance, while having a limited effect on IMD3. Therefore, the optimization of the various parameters can be partially decoupled.

Fig. 1 shows the single-tone and two-tone simulated fundamental load pull contours at 24 dBm input power, with the following terminations: $\Gamma_{\mathrm{S},f_0} = 0.62e^{-j0.92\pi}$, $\Gamma_{\mathrm{S},2f_0} = e^{-j0.94\pi}$, $\Gamma_{\mathrm{L,bb}} = e^{j\pi}$, $\Gamma_{\mathrm{L},2f_0} = e^{-j0.86\pi}$, selected after successive optimization steps according to the criteria described above. The red curves are the single-tone output power contours, while the blue and green curves are the two-tone PAE and IMD3, respectively.

Despite the selected transistor allows for a limited margin in terms of achievable power, therefore, to be terminated on a load that is quite close to its optimum for power, the selected source and load terminations are such as to allow to achieve the $P_{\mathrm{out},f_0}$ target at $P_{\mathrm{in},f_0}$=24 dBm with a reasonable margin (around 1 dB) over a sufficiently wide set of fundamental loads $\Gamma_{\mathrm{L},f_0}$. Moreover, there is a subset of such loads that allows achieving IMD3 better than -30 dBc at maximum input power ($P_{\mathrm{in,2t}f_0}$=24 dBm) while achieving PAE as high as 55%. It should be noted that the $P_{\mathrm{out},f_0}$ is typically the most stringent requirement, while the required linearity could be recovered with a limited efficiency drop by slightly backing off the input power. Therefore, the selected fundamental load termination ($\Gamma_{\mathrm{L},f_0} = 0.4e^{j0.7\pi}$) is in the region where the IMD3 is exactly below -30 dBc and the output power margin is optimized up to 1dBm, foreseeing the losses in the output passive networks and possible deviations from the desired loading conditions due to manufacturing.

The Output (OMN) and Input (IMN) Matching Networks are both built as a cascade of the $2f_0$ tuning section (close to the device) and of the $f_0$ matching section. In the OMN, the critical control of $\Gamma_{\mathrm{L,bb}}$ is performed by optimizing the

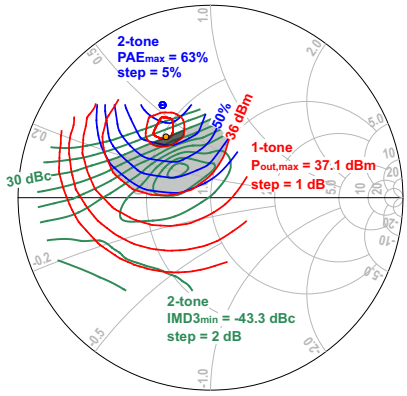


Fig. 1. Simulated fundamental load pull contours at 3.5 GHz for the selected $\Gamma_{\mathrm{S},f_0/2f_0}$ and $\Gamma_{\mathrm{L,bb}/2f_0}$: single-tone output power (red), and two-tone PAE (blue) and IMD3 (green) at 24 dBm input power. The light shaded area corresponds to the design space for $\Gamma_{\mathrm{L},f_0}$ based on the power and linearity constraints. The dark area is the subset of the design space for which the PAE is maximized, the optimum load $\Gamma_{\mathrm{L},f_0} = 0.4e^{j0.7\pi}$ is highlighted by the yellow dot.

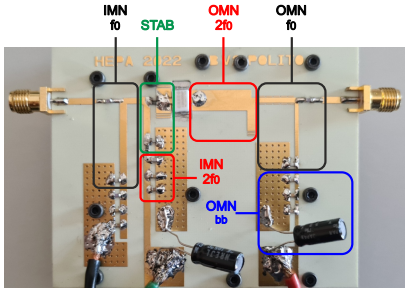


Fig. 2. Photograph of the manufactured PA.

positions and value of the decoupling capacitors on the drain supply line. The substrate selected for the implementation of the passive structures is the Rogers 4350b substrate (3.66 relative dielectric constant, 0.762 mm substrate thickness, and 35 $\mu$m metal thickness). The photograph of the realized prototype is shown in Fig. 2, where the structure of the MNs is highlighted.

## IV. Experimental Characterization

The amplifier has been characterized in small and large signal conditions. The selected bias point is $V_{\mathrm{DS}} = 30$V, $V_{\mathrm{GS}} = -2.84$V corresponding to $I_{\mathrm{DS}} = 35$mA. In simulation, the same drain current is obtained for $V_{\mathrm{GS}} = -3.1$V.

The small signal performance in the range 1 GHz to 6 GHz is illustrated in Fig. 3, where measured results (symbols) are compared to simulated ones (solid). The agreement is good apart from a 200 MHz shift towards lower frequency; $S_{21}$ peaks at 3.3 GHz while input ($S_{11}$) and output $S_{22}$ matching results better than 7 dB and 10 dB in a 500 MHz bandwidth, between 3 GHz and 3.5 GHz respectively.

The large signal measurement are performed by a real-time vector test bench, calibrated using a 2-port Short-Open-Load-Thru (SOLT) routine, plus a SOL additional calibration at an extended output port connected to a power

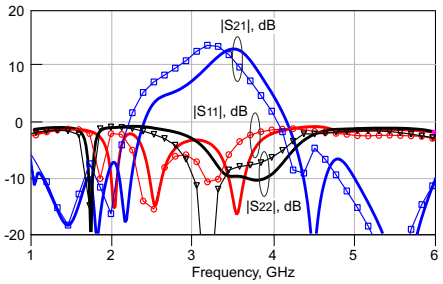


Fig. 3. Simulated (solid) and measured (symbols) scattering parameters.

meter for the absolute power calibration. The simulated and measured continuous wave (CW) performance at the respective center frequencies is reported in Fig 4. The comparison, once accounting for the center frequency shift, highlights a very good agreement in terms of gain and output power, with a small difference only in terms of PAE, slightly higher in measurements (around 3%), due to a lower DC consumption. This may be due to the joint effect of a difference in the $2f_0$ termination and of lower losses in measurements as a result of the lower absolute frequency. At saturation (3 dB compression), the amplifier presents a power gain in excess of 10 dB, an output power in excess of 38 dBm, and a PAE of 73%. At the target 24 dBm input power, the gain, output power, and power-added efficiency are 12 dB, 36 dBm and 60%, respectively.

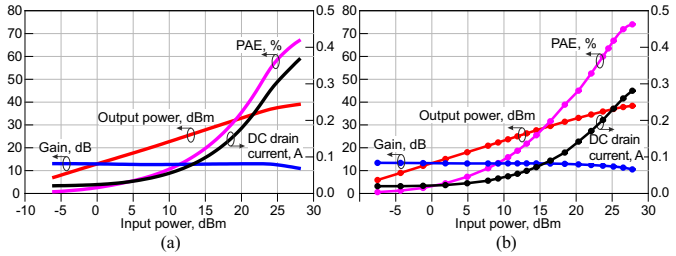


Fig. 4. Comparison of CW single-tone performance at respective center frequencies: (a) simulated (solid) at 3.45 GHz and (b) measured (symbols) at 3.25 GHz.

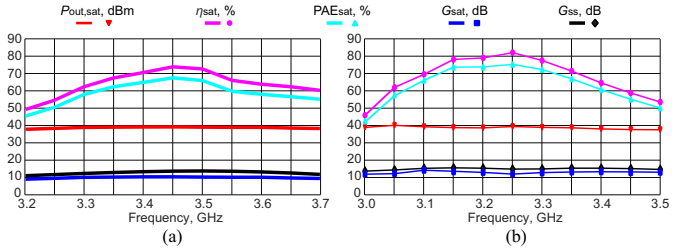


Fig. 5. Comparison of CW single-tone performance versus frequency: (a) simulated from 3.2 GHz to 3.7 GHz and (b) measured from 3 GHz to 3.5 GHz.

The agreement over a 500 MHz band remains very well captured, as evidenced in Fig. 5. From 3 GHz to 3.5 GHz, the measured output power, gain, and PAE at saturation are higher than 36.5 dBm, 10 dB and 40%, respectively.

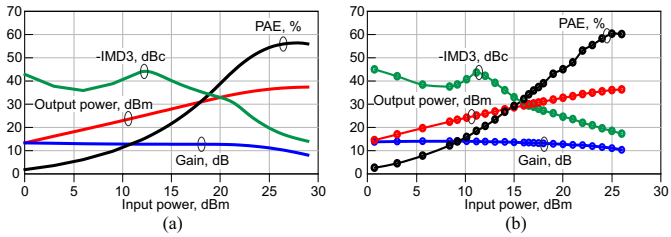


Fig. 6. Comparison of two-tone performance at respective center frequencies: (a) simulated (solid) at 3.45 GHz and (b) measured (symbols) at 3.25 GHz.

Two-tone measurements with 20 MHz spacing have been performed in the range 3–3.5 GHz. The comparison between simulated and measured results at the respective center frequencies is reported in Fig. 6. Also in this case, the agreement is rather good. The output power, gain and PAE are accurately captured, as well as the IMD3 up to the position of the sweet spot (around 12 dBm input power). The main difference is visible in the IMD3 slope in the non-linear region, causing a faster drop in measurement than in simulation, which could not be fully compensated by adopting post tuning of either bias point or matching networks. Around 3.25 GHz, the PA demonstrates a measured PAE of 33% at -30 dBc IMD3, while simulations predict a PAE of 45%. This, in turn, is lower than the one observed in the load pull, due to the losses of the OMN as well as slightly sub-optimal synthesis of the baseband and second harmonic terminations after bias point adjustments.

## V. Conclusion

A design strategy to optimize the efficiency of a class-AB PA, given minimum output power, gain and linearity requirements, has been presented. The selection of optimum source and load terminations and the required trade-offs have been discussed. The validity of the approach is demonstrated by a prototype that achieves a PAE of 73% at maximum power and 33% at the minimum required linearity.

## References

[1] N. Safari, T. Roste, P. Fedorenko, and J. S. Kenney, "An Approximation of Volterra Series Using Delay Envelopes, Applied to Digital Predistortion of RF Power Amplifiers With Memory Effects," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 2, pp. 115–117, 2008.

[2] C. Clark, C. Silva, A. Moulthrop, and M. Muha, "Power-amplifier characterization using a two-tone measurement technique," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 6, pp. 1590 –1602, Jun. 2002.

[3] R. Figueiredo, N. B. Carvalho, A. Piacibello, and V. Camarchia, "Nonlinear Dynamic RF System Characterization: Envelope Intermodulation Distortion Profiles—A Noise Power Ratio-Based Approach," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 9, pp. 4256–4271, 2021.

[4] H. Lyu, Y. Cao, and K. Chen, "Linearity-Enhanced and Highly Efficient Doherty Power Amplifier: 16th High Efficiency Power Amplifier Student Design Competition," *IEEE Microwave Magazine*, vol. 22, no. 10, pp. 62–69, 2021.

[5] P. E. de Falco, J. Birchall, and L. Smith, "Hitting the Sweet Spot," *IEEE microwave magazine*, vol. 18, no. 1, pp. 63–70, 2017.

[6] R. Quaglia, L. Piazzon, V. Camarchia, R. Giofrè, M. Pirola, P. Colantonio, G. Ghione, and F. Giannini, "Experimental investigation of bias current and load modulation effects in phase distortion of GaN HEMTs," *Electronics Letters*, vol. 50, no. 10, pp. 773–775, 2014.