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TCAD assisted design of the Doherty Power Amplifier☆,☆☆

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ABSTRACT

Nonlinear physics-based TCAD simulations based on the Harmonic Balance technique represent an important tool to link the performance of microwave circuits to the active device fabrication technology (Donati Guerrieri et al., 2016 [1,2]). While nonlinear TCAD simulations were previously limited to the analysis of circuits including a single device, starting from Donati Guerrieri et al. (2022) they have been extended to circuits with multiple interacting devices. This work, further extending Donati Guerrieri et al. (2022), shows a complete example of the design of a Doherty Power Amplifier fully assisted by TCAD nonlinear simulations. The analysis allows for a complete inspection of the internal physical variables of the DPA, including carrier concentrations and electrostatic potential, making it possible to verify the correct operation of the main and auxiliary devices. The proposed DPA, exploiting a GaAs MESFET technology, achieves 30 dBm output power at 12 GHz with peak Power Added Efficiency (PAE) of 52% at 6 dB Output Power Back-off (OBO) and 5 dB gain. The reported results show that the power split ratio between the MAIN and AUX amplifier can be used to achieve a good compromise between linearity and efficiency.

1. Introduction

The successful design for 5G/6G front-ends in modern telecommunication systems strongly depends on the design of broadband Power Amplifies (PAs) efficiently handling high Peak-to-Average Power Ratio (PAPR) signals, i.e. featuring high efficiency from back-off to saturation. Microwave PAs typically combine multiple devices in their final stage to reach the required output power level. Hence, high efficiency PA design schemes aim at combining the devices maximizing at the same time the PA efficiency in a prescribed back-off power range [1]. One the most successful high efficiency PA scheme is the Doherty Power Amplifier (DPA) [2,3], where two active devices (FETs) from the same technology are combined so that one (the so-called peaking or auxiliary — AUX) acts like an active load for the other (the main — MAIN). In the symmetric Doherty configuration, two devices of the same periphery contribute with the same amount to the overall PA output power and the DPA should exhibit a constant efficiency in a range of 6 dB output power back-off (OBO) [2]. Although the Doherty scheme has gained great attention even exploiting the most advanced microwave power technologies, including GaAs and GaN, practical realizations often show poorer performance than expected due to the difficult design and optimization of the output coupling and matching network (OCMN) [4,5], which includes quarter-wave transmission lines and matching networks. In fact, the OCMN design requires accurate device models from deep class C (used for the AUX device) to class AB (MAIN device), often not available even in the foundry design kits. In fact, the DPA operation is highly nonlinear, non only at high power, but even in back-off, due to the nonlinearity of the class C stage.

Physics-based analysis through nonlinear Technological CAD (TCAD) simulations represents the ideal way to analyse and optimize the DPA, since both the device currents and the gate charge are seamlessly modelled in all operating conditions from the threshold up to saturation, accurately linking them to the underlying technological and physical device parameters. Contrary to the usual parallel stage PAs, where devices are isolated, the AUX and MAIN devices interact through the OCMN: hence the DPA analysis requires to model the two active devices concurrently. Only recently, the nonlinear TCAD simulations, originally limited to the analysis of circuits including a single active device, have been extended [6] to circuits with multiple interacting devices, making the LS TCAD analysis of the DPA amenable for the first time.

This work, further extending [6], shows a complete example of the analysis and preliminary design of a Doherty amplifier fully assisted by TCAD simulations. In this preliminary design, the active device is entirely modelled by means of physics-based simulations while the passive structures, including transmission lines and matching networks,

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are modelled as ideal components or idlers. This allows to tailor the DPA optimization starting from the constrains coming from the active device itself. The physical design of the passives is considered as a further step which will be the object of future work. The designed DPA, exploiting a GaAs MESFET technology, achieves 30 dBm output power at 12 GHz with peak Power Added Efficiency (PAE) of 52% at 6 dB Output Power Back-off (OBO) and 5 dB gain. The reported results show that the power split ratio between the MAIN and AUX amplifier can be used to achieve a good compromise between linearity and efficiency.

2. DPA TCAD simulation

Nonlinear LS TCAD analysis specifically addresses the physics-based simulation of high frequency semiconductor devices in the typical operating conditions of microwave (MW) stages, namely periodic and highly nonlinear. In [7,8], the Harmonic Balance (HB) algorithm was first introduced as the main tool to solve the physical equations in the frequency domain. With this approach, the harmonics of the device solution, in terms of both terminal variables (e.g. drain and gate currents) and internal physical quantities (e.g. electric field, potential and carrier densities) are made directly accessible for the specific device LS operating condition, driven by the external large-signal stimuli coupled to the external circuit (mixed-mode analysis). Notice that the HB TCAD analysis is similar to the HB techniques used in microwave circuit simulators (e.g. ADS [9]), making it simple to include in a seamless way the device embedding circuit in terms of harmonic loads, transmission lines, dividers/combiners etc.

In this work we exploit our in-house mixed-mode drift-diffusion TCAD simulator [10], implementing the Harmonic Balance technique. Besides the solution of the device LS working point, our simulator implements unique capabilities, like the Small-Signal LS and conversion Green's Function analyses [11] for noise and the sensitivity analysis of MW stages [12,13]. In [6] we have extended our TCAD code to the mixed mode analysis of a complete circuit, including multiple active devices, with the preliminary demonstration of a TCAD DPA analysis.

In this work we address the full TCAD analysis of a Doherty stage at 12 GHz based on a GaAs MESFET technology. The active device is a MESFET GaAs epitaxial device with 170 nm active GaAs channel, 2×10^{17} cm^{-3} channel doping, 0.5 μm gate length and 0.5 μm contact length, 0.5 μm source-gate spacing and 1 μm drain-gate spacing [12]. The device periphery is set to 1 mm. Velocity saturation is included via the Caughey-Thomas model, with low field electron mobility $\mu_0 = 2500$ cm^2/(Vs) and saturation velocity $v_{sat} = 1.4 \times 10^7$ cm/s. The drain and source contact resistance is 3 Ω/mm while the gate contact resistance is 5 Ω/mm. The estimated threshold voltage is −3.75 V. This device was analysed in [14,15] for the design of a class AB amplifier (10% I_{DSS}). The optimum load $Z_{opt} = 47 + j11$ Ω was extracted from accurate TCAD load-pull simulations. The same bias point and optimum load will be used for the MAIN amplifier in this work. The device output characteristics and the MAIN device bias point are shown in Fig. 1.

The basic Doherty topology is shown in Fig. 2: the MAIN amplifier is connected to the common load $R_{opt}/2$ (half of the MAIN optimum load) by the impedance inverter (typically a quarter wavelength line). In back-off the AUX amplifier is OFF, and the MAIN sees an equivalent load $2R_{opt}$; when the AUX device turns on, both devices will see an equivalent load equal to R_{opt}. This ideal scheme is oversimplified in terms of the MAIN optimum load in back-off. Fig. 1 shows the expected load lines of the MAIN amplifier for the fundamental tone. The highest efficiency in back-off is obtained when the voltage swing is maximum (i.e., the dynamic load line touches the knee voltage) while the current swing is half the maximum allowed (I_{DSS}). Notice that, when the MAIN operates with a load $R_{opt,BO} > R_{opt}$, the maximum voltage swing of the drain voltage increases due to the lower knee voltage (see Fig. 1). This effectively corresponds to an even higher load that must be presented to MAIN in back-off condition. In our device, the value of the optimum

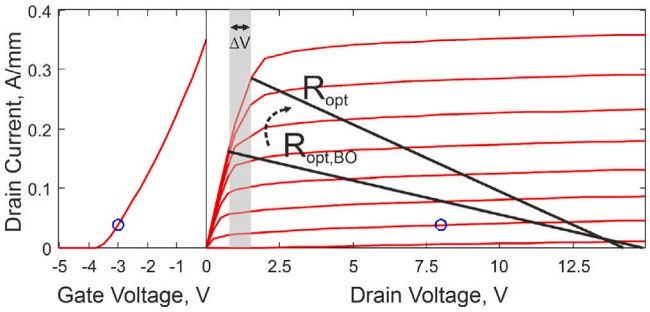

Fig. 1. Transcharacteristic and output characteristic of the MESFET device. The blue circles shows the selected AB bias point (10% IDSS) used for the MAIN amplifier. The load required in back-off $R_{opt,BO}$ is higher than the ideal value $2R_{opt}$ due to the effect of the lower knee voltage.

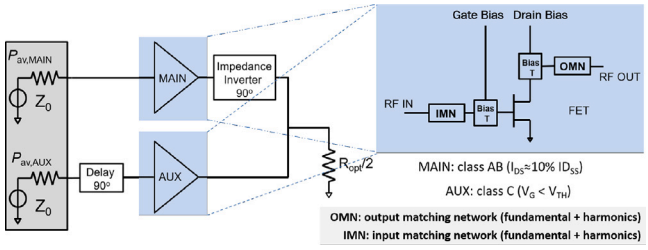

Fig. 2. Circuit setup of the ABC Doherty scheme. The main and auxiliary amplifiers are both implemented as shown in the inset.

load in back-off has been estimated 15% higher than the ideal $2R_{opt}$ value.

The AUX amplifier input is 90° phase shifted with respect to the MAIN input, compensating the delay of the quarter-wave transmission line at the MAIN output, so that the powers combine in phase at the common output node. Instead of an input power splitter, we consider a dual input with a fixed power ratio $\alpha = P_{av,AUX}/P_{av,MAIN}$, where $P_{av,AUX}$ and $P_{av,MAIN}$ are the available input powers of the AUX and MAIN amplifiers, respectively. An even input splitter corresponds to $\alpha = 1$, while uneven splitters can be simulated by simply changing the value of α. As shown in the inset of Fig. 2 each amplifier includes the active device (here the MESFET) along with the input matching network (IMN) and output matching network (OMN). We follow the standard ABC Doherty scheme [16], exploiting a Class AB bias condition for the MAIN amplifier and a Class C one for the AUX amplifier, respectively. While the MAIN device bias point is shown in Fig. 1, the AUX bias will be tuned in the following section, ranging from $V_{GS} = -6$ V to $V_{GS} = -4.5$ V.

The Doherty scheme has been implemented for TCAD simulations as shown in Fig. 3.

The transmission line TL2 with characteristic impedance $Z_{C2} = \sqrt{R_{opt} R_L/2}$ transforms the output load $R_L = 50\ \Omega$ into the common load $R_{opt}/2$. The transmission line TL1 with characteristic impedance $Z_{C1} = \sqrt{k} R_{opt}$ ($R_{opt} = \mathrm{Re}(Z_{opt})$) inverts the impedance (notice the factor $k = 1.15$ to compensate the knee voltage reduction in back-off). The imaginary part of the optimum load stems basically from the combined effect of the C_{DS} and C_{GD} capacitances. Hence the output matching networks have been replaced by a negative shunt capacitance tuning out the device output capacitance (the design of a physical matching network will be addressed in future works). Notice, though, that small-signal simulations of the MESFET device show that the output capacitance does not vary considerably with gate bias: hence

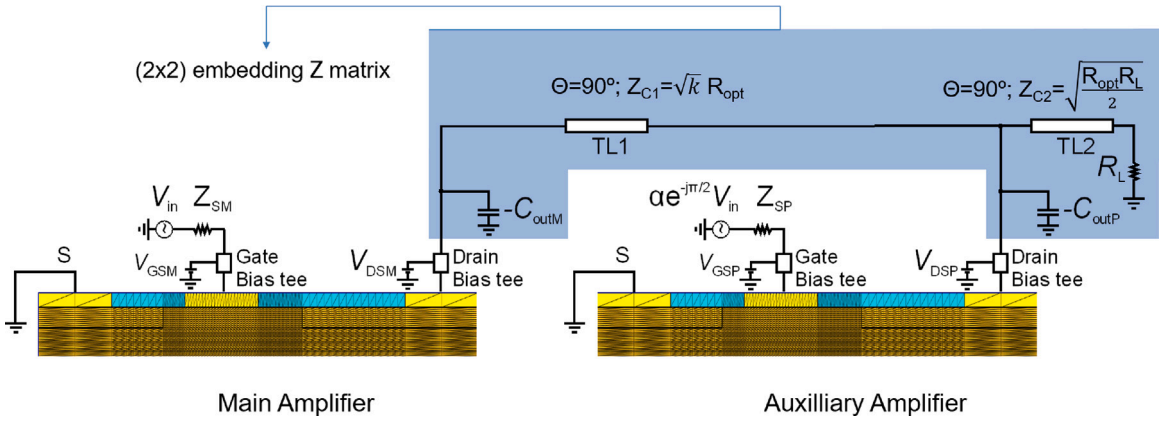

Fig. 3. Circuit setup for the TCAD Doherty simulation. The embedding circuit is represented by an equivalent 2 × 2 impedance matrix coupling the drain ports of the main and auxiliary devices.

$C_{out,M}$ and $C_{out,P}$ have similar values.[1] The source impedances Z_{SM} and Z_{SP} are implemented by ideal tuners. For low frequency analysis they have been set to 50 Ω. For the operating frequency of 12 GHz they have been extracted from LS analysis as will be discussed in Section 5. The external network has been converted into a passive 2 × 2 block described by the equivalent Z matrix, as shown in Fig. 3 for the mixed-mode TCAD analysis.

The two MESFET devices are shown in Fig. 3 with their discretization mesh, including roughly 3200 nodes each. The two independent grids have been merged into a unique mesh equivalent to a 6 terminal device with approximately 6500 grid nodes overall. Devices interact only through the external network, since Neumann boundary conditions ensure isolation at the GaAs level. The Harmonic Balance drift-diffusion system including the Poisson equation, electron continuity equation and circuit external equations was solved including 8 harmonics. The overall number of equations was thus 219,980. The simulation time is approximately 15–30 min for each input power on a Core i9 8 Core PC with 3.6 GHz processor and 64 GB memory, depending on the degree of nonlinearity of the operating condition.

3. Doherty amplifier physical analysis

As a preliminary demonstration of the capability of the TCAD DPA analysis, we have run simulations varying some of the relevant DPA design parameters, e.g. the gate bias and the power split ratio, starting with a low frequency case (f = 1 MHz) where dynamic effects can be neglected. In the low frequency analysis, the combining network at the output of the MAIN and AUX amplifiers only includes the impedance inverter and the common load, while there is no need to tune out the device capacitances, since they can be neglected. In this section we provide the physical insight of the MESFET variables in the particular case of V_{GS} = −5 V and α = 2 (i.e. approximately 1.5 dBm more input power to the AUX stage).

Fig. 4 shows the DC component of the device electron concentration at three increasing powers, from back-off to saturation. In back-off the AUX has a depleted channel, which turns-on at increasing input power due class C self-biasing. At saturation the two devices exhibit nearly the same channel population and the class C device operates similarly to the class B one. This confirms the good operation of the Doherty stage. In fact, at peak power both devices must contribute the same power to the common load. The same is observed for the first harmonic: notice that here we compare the real part of the electron concentration for the MAIN with the imaginary part for the AUX (we plot the opposite for display purpose): in fact due to the 90° phase shift in the input drive, these two quantities turn out to be in phase.

Similarly, Fig. 5 (top) shows the first harmonic of the electrostatic potential in the device cross section. Here again we compare the real part of the MAIN potential with the corresponding imaginary part of the AUX. We notice again that the class C stage the voltage swing becomes similar to the class B one, a condition that has to be met in order for the two devices to contribute evenly to the overall output power. While the external generator provides power at the fundamental frequency only, harmonics are generated in the device due to the nonlinearities of the class AB and C stages. The second harmonic of the electrostatic potential is reported in Fig. 5 (bottom). We notice that it is generated mainly in the saturated portion of the channel and again the MAIN and AUX stages behave similarly once they reach the peak power condition. Interestingly, here we compare the real parts for both devices, since nonlinearities excited by the 90° phase-shifted inputs induce in-phase second harmonics.

Finally, Fig. 6 shows the dynamic load lines (DLL) for the same three bias conditions presented in Figs. 4 and 5. The modulation of the equivalent load seen by the MAIN device is clearly observed, and further demonstrates the proper operation of the Doherty amplifier.

4. Multi-bias analysis

The first issue encountered in the design of the Doherty stage is the correct selection of the bias point for the AUX and MAIN devices. Concerning the MAIN amplifier, the choice is usually driven by a compromise between efficiency and linearity, which is usually found in a deep class AB point. Here we have selected the bias point shown in Fig. 1, as explained in Section 2. In this section we perform simulations in order to define the best bias and power split ratio for the AUX stage. The power split ratio α between the available input powers directly corresponds to an equivalent ratio $\sqrt{\alpha}$ between the values of the open-circuit voltage generators applied to the AUX and MAIN gate terminals. In order to avoid the issues of the dynamic effects, and focusing only on the load modulation capability of the AUX device when correctly turned on, we perform this analysis again in the low frequency case (f = 1 MHz). We investigate 4 cases and compare them to the case of a parallel stage with two 1 mm devices biased at the same bias as the MAIN amplifier, hereafter denoted as the PARALLEL solution. Denoting with $V_{GS,MAIN}$ $V_{GS,AUX}$ the applied gate voltages, we identify the following cases:

A: $V_{GS,MAIN}$ = −3 V, $V_{GS,AUX}$ = −4.5 V, α = 1
B: $V_{GS,MAIN}$ = −3 V, $V_{GS,AUX}$ = −5 V, $\alpha = \sqrt{2}$
C: $V_{GS,MAIN}$ = −3 V, $V_{GS,AUX}$ = −5 V, α = 1
D: $V_{GS,MAIN}$ = −3 V, $V_{GS,AUX}$ = −6 V, $\alpha = \sqrt{2}$

[1] Hereafter we will use subscript "M" to denote MAIN quantities, and subscript "P" for AUX quantities, where "P" stands for Peaking.

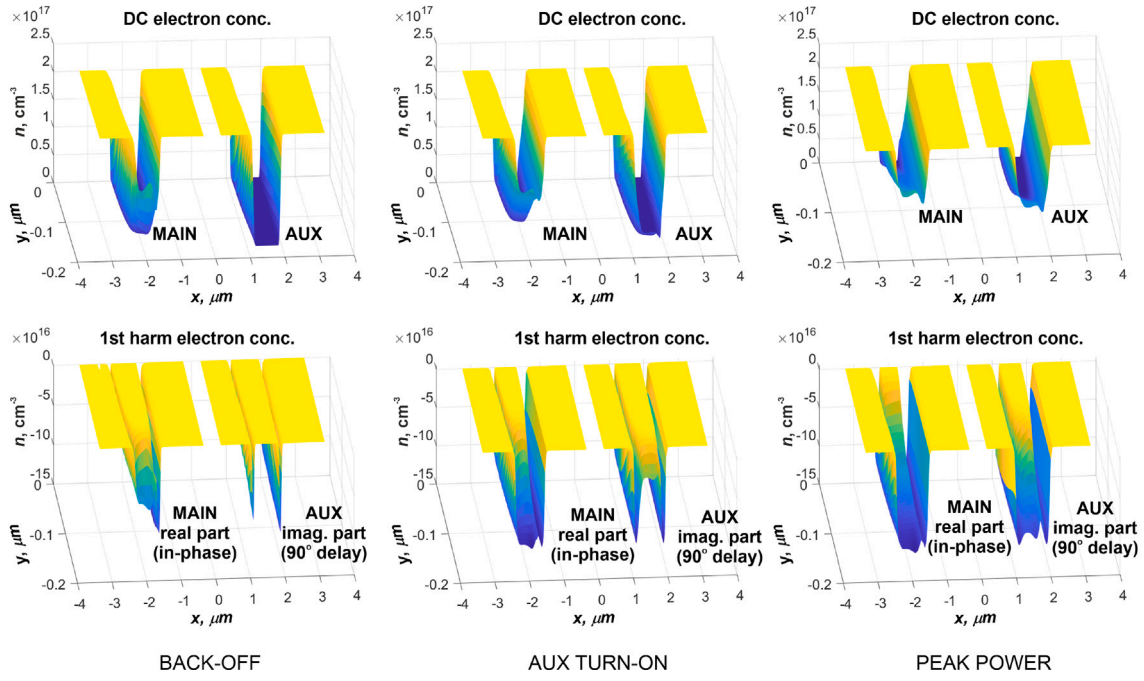

Fig. 4. DC component (top) and 1st harmonic of the electron density (bottom) in the MAIN and AUX devices. Left: back-off. Middle: intermediate power. Right: peak power. The gates are located at the position $y = 0$ (rear of the plots). The MAIN gate extends from $x = -2.25\,\mu m$ and $x = -1.75\,\mu m$ and AUX gate is from $x = 1.25\,\mu m$ and $x = 1.75\,\mu m$. The overall available power is 2.5 dBm (left), 12.5 dBm (middle) and 19.5 dBm (right) divided among the MAIN and AUX devices with a power split ratio of $\alpha = 2$.

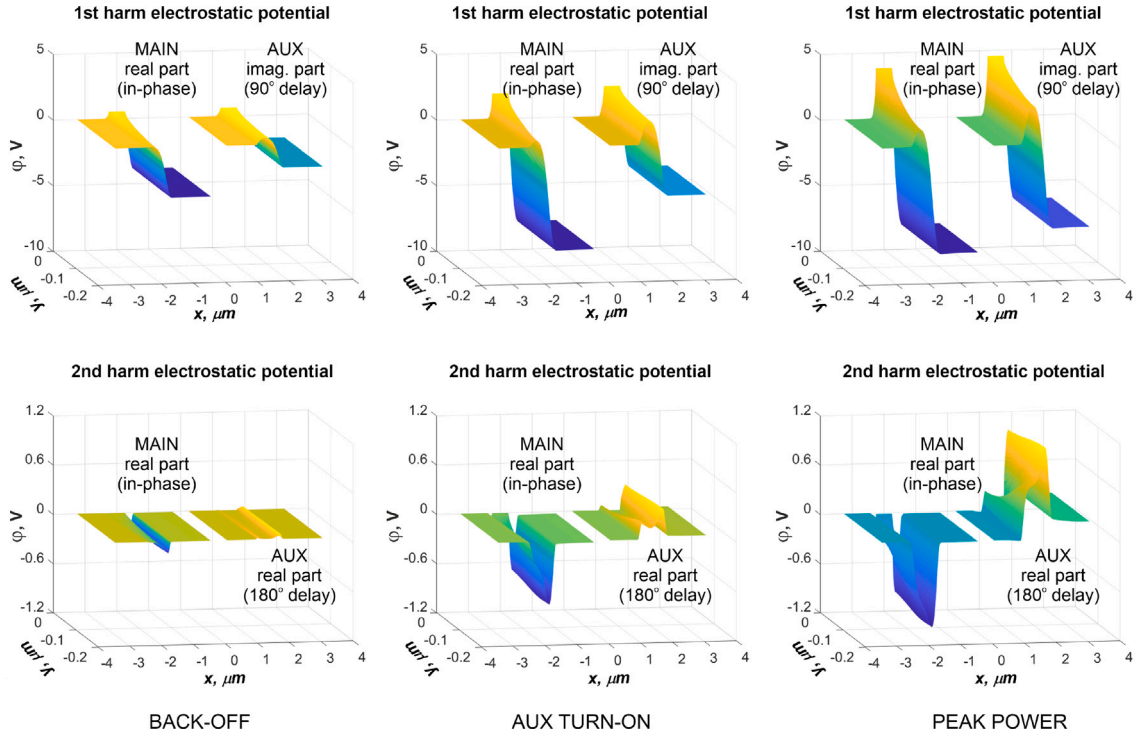

Fig. 5. First (top) and second harmonic (bottom) of the electrostatic potential in the device cross-section. The three operating conditions are the same as Fig. 4.

Fig. 7 monitors the equivalent loads seen at the MAIN and AUX output ports, showing the good load modulation of the MAIN amplifier, starting close to 2 R_{opt} and decreasing to a value close to the optimum load (real part). On the other hand, the AUX impedance is very high in back-off and settles to R_{opt} at peak power. Fig. 7 shows that in case A the AUX stage turns on much earlier than in case D.

Fig. 8 reports the overall DPA efficiency while Figs. 9 and 10 show the individual MAIN and AUX efficiency in the various cases. We clearly see that all the Doherty stages outperform the conventional class B amplifier (dashed lines) in terms of efficiency, showing the characteristic high efficiency region over a 6 dB output power back-off extension. In particular, Fig. 9 shows that the MAIN stage reaches

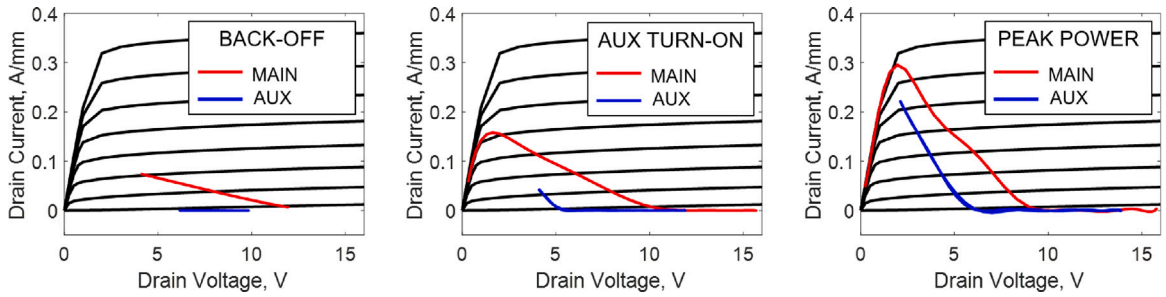

Fig. 6. Dynamic load lines for the same operating conditions of Figs. 4 and 5. BACK-OFF (left); AUX TURN-ON (centre); and PEAK POWER (right).

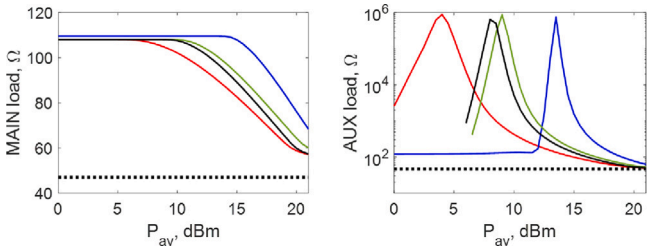

Fig. 7. Loads seen by the MAIN (left) and AUX (right) devices in the analysed cases, compared to R_{opt} (black dashed line). The load of the AUX device is significant only after the device turn on (peak of the equivalent load).

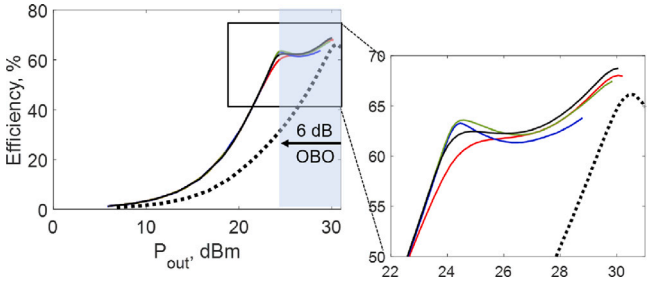

Fig. 8. Efficiency of the Doherty amplifier as a function of the output power. The inset highlights the Doherty region. Red: case A. Black: case B. Green: case C. Blue: case D. Black dots: PARALLEL class AB stage.

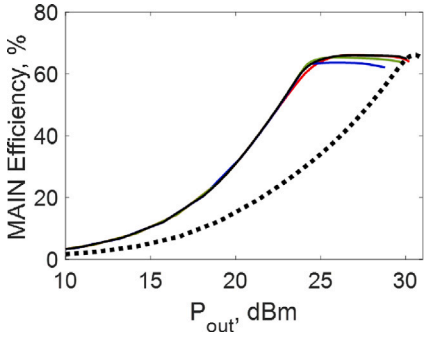

Fig. 9. Efficiency of the MAIN amplifier in the analysed configurations. Red: case A. Black: case B. Green: case C. Blue: case D. Black dots: PARALLEL class AB stage.

the maximum efficiency at approximately half of the output power swing, and maintains it high in the full Doherty region. This is exactly prescribed by a proper Doherty operation. On the other hand, the AUX efficiency starts to increase at the turn on (see Fig. 10) and keeps increasing up to the DPA compression.

All the analysed configurations seem to perform very well in terms of efficiency, despite slight differences can be seen in the zoom of

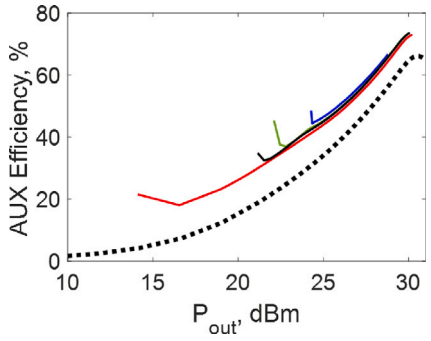

Fig. 10. Efficiency of the AUX amplifier in the analysed configurations. Red: case A. Black: case B. Green: case C. Blue: case D. Black dots: PARALLEL class AB stage.

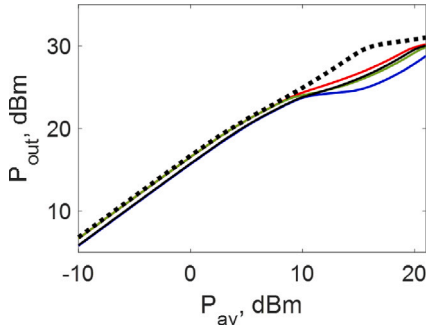

Fig. 11. Output power for the analysed configurations. Red: case A. Black: case B. Green: case C. Blue: case D. Black dots: PARALLEL class AB stage.

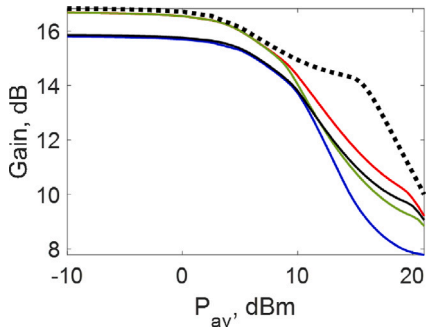

Fig. 12. Available gain of the DPA in the analysed configurations. Red: case A. Black: case B. Green: case C. Blue: case D. Black dots: PARALLEL class AB stage.

Fig. 8. The differences are instead very clear when we monitor the other DPA performances. Fig. 11 reports the output power in the 4 analysed cases while Fig. 12 the gain (due to the low frequency, the devices are highly mismatched at the input and the only significant gain is the available gain). Overall, the performance of the parallel stage is better

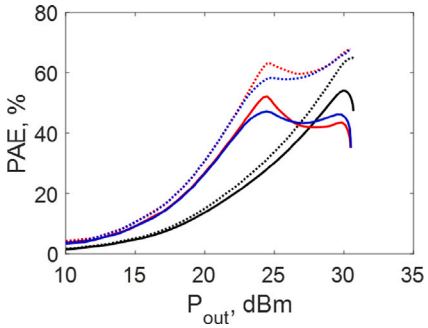

Fig. 13. Efficiency (dots) and PAE (solid lines) of the matched DPA for cases B (blue) and C (red) compared to the parallel class AB case (black). The frequency is 12 GHz.

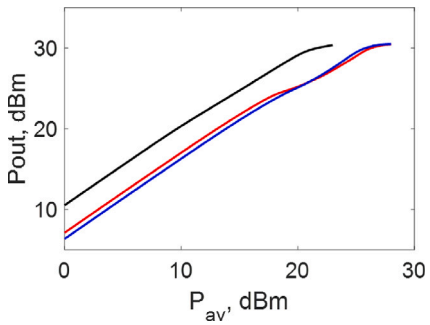

Fig. 14. Output power of matched DPA for cases B (blue) and C (red) compared to the parallel class AB case (black). The frequency is 12 GHz.

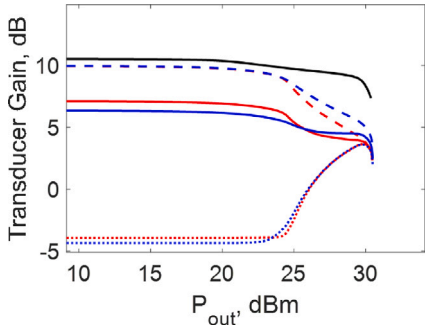

Fig. 15. Available gain of the input and output matched DPA for cases B (blue) and C (red) compared to the parallel class AB case (black). Dash lines show the MAIN gain while dotted lines the AUX gain. The frequency is 12 GHz.

than the DPA, especially in terms of the gain, which is expected to be less in back-off since the AUX amplifier is OFF, but also in terms of the maximum output power: we notice a significant decrease from case A to D, not only in back-off, but even in the whole Doherty region. Notice that the gain in back-off is dominated by the choice of the power split ratio α. This is relevant also for the DPA operation, since this is also the gain at the onset of the Doherty region.

The typical design issues of the Doherty amplifiers are clearly visible. To maintain a neat first efficiency peak, the main amplifier must be able to reach the maximum swing *right before* the turn on of the auxiliary amplifier (e.g., case C). Furthermore, when the auxiliary amplifier turns on too late (e.g., case D), the efficiency is good but the output power may not even reach the maximum level before the main amplifier compression. Anticipating the AUX turn-on too much (case A, red curve) degrades the first peak efficiency but is beneficial in terms of gain (see Fig. 12) and maximum output power. Despite being similar, due to the identical bias, cases B and C are slightly different in terms of AUX turn on: when the AUX power is higher (case B) the device turns on earlier and the slight decrease in efficiency may be compensated by higher power and gain. Hence, the power split ratio can be regarded as a parameter to be tuned to find a compromise trading efficiency, output power and gain. The AUX bias can be used similarly, but in a very limited interval, since, as we have seen, both cases A and D cannot be considered acceptable. At higher frequency, the input matching significantly alters the power absorbed by the main and auxiliary input port, even with fixed power split ratio. In the next Section, the input matching is investigated in order to identify the best trade off between efficiency, output power and gain.

5. Dynamic analysis of the doherty amplifier

In this section we move the design of the DPA to the operating frequency of 12 GHz. We restrict the analysis to cases B and C of the previous section, since they offer the best performance in terms of efficiency and output power. We now include output and input matching in our DPA analysis. The optimum termination for the input ports has been extracted from simulations of the MESFET in a stand-alone, class AB simulation. The class AB stage has been simulated with optimum load at 12 GHz, and the corresponding input reflection coefficient has been found to vary from back-off to compression. The source load of both the MAIN and AUX stages of the DPA (see Fig. 3) has been then set to conjugate match the input reflection coefficient at peak power $Z_{SM} = Z_{SP} = (8 + j23)\ \Omega$. In this way the DPA will be best matched at the higher output power range, corresponding to the Doherty region where the DPA is operated. Of course, this choice further degrades the DPA gain in back-off (which, as seen in the previous section, is already significantly lower than for the parallel class AB stage). Other choices of the input reflection coefficient are beyond the scope of this paper.

Figs. 13–15 show the performance of the fully matched DPA. Overall, the DPA efficiency is good in comparison with the class AB case, especially in back-off, despite the PAE suffers from a significant penalty due to the low DPA gain. Both configurations (B and C) reach the maximum output power as the parallel class AB stage, showing that the output load is correctly chosen. This is confirmed by the equivalent load seen by the MAIN and AUX output ports. Fig. 16 shows the output load. Here, the (small-signal) output device capacitance has been de-embedded to better highlight the behaviour of the MAIN and AUX loads compared to the ideal DPA. We clearly see that both the MAIN and AUX amplifiers converge to the optimum load (blue square) at peak power. In back-off the two devices has the correct load: the value $2R_{opt}$ by the MAIN and a high impedance for the AUX. In the intermediate region though, the loads deviate from being entirely real, and this reflects in a sub-optimum performance of the Doherty stage. This behaviour is highly dependent on the input power, and therefore is hardly address by a fixed delay line in the output combiner. Concerning the input, Fig. 17 shows the load seen at the MAIN and AUX input ports. The mark shows the conjugate of the source load of the generator. While the MAIN amplifier is slightly mismatched in back-off, it become well matched at peak power: this is expected since the source impedance was chosen exactly to match the MAIN amplifier in this condition. On the contrary, the AUX amplifier is not well matched at the input port.

In case B the AUX device is fed by 1.5 dB more input power. This reflects in an earlier turn on and in a smoothed efficiency peak in back-off. Furthermore, the overall DPA gain in back-off is lower in case B than in case C since the additional power provided to the AUX amplifier does not correspond to any output power until the AUX turns on (notice that we report the overall DPA available gain, i.e. the ratio of the output power to the available input power). On the other hand case B gain is more flat and remains higher than 5 dB in the whole Doherty region. In fact, Fig. 13 shows that while the efficiency of case B is always lower than case C, the PAE is slightly worse than case C at 6 dB OBO but becomes significantly higher from 3 dB OBO up to compression. Taking case C as reference, we conclude that the designed DPA achieves 30

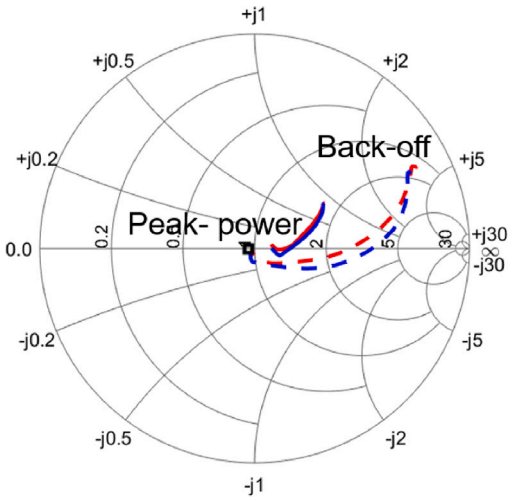

Fig. 16. Output load of the MAIN (solid lines) and AUX (dashed lines) device. The mark denotes the optimum load $R_{opt} = 47$ that, de-embedding the output capacitance, is close to the 50 Ω point of the Smith chart.

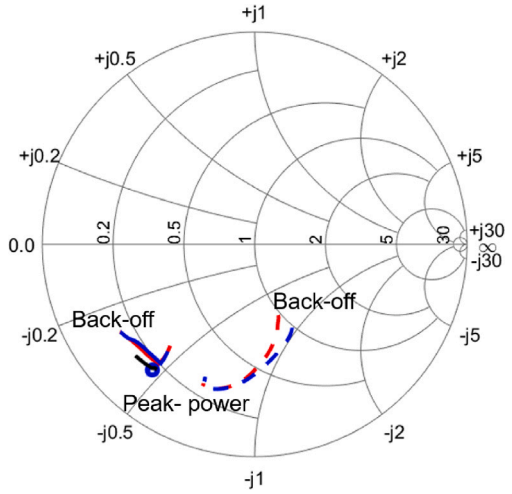

Fig. 17. Input impedance of the MAIN (solid lines) and AUX (dashed lines) device. The mark denotes the conjugate of the generator impedance used for input matching. The black line shows the parallel stage input.

dBm output power at 12 GHz with peak PAE of 52% at 6 dB OBO and 5 dB gain. This demonstrates that accurate device modelling is an excellent tool to devise the best compromise among the various DPA power performance.

6. Conclusions

This work presented a TCAD approach to the DPA analysis. TCAD device modelling is superior to the conventional analytical FET models used for the analysis of the DPA operation, often based on an oversimplified linear transcharacteristic. Here the smooth turn-on of the class C AUX stage across threshold is accurately modelled and used to address some of the main bottlenecks found in the DPA design, namely the bias selection and the power split ratio between the MAIN and AUX stages.

Concerning the FET dynamic behaviour, the input and output capacitances are seamlessly modelled from back-off to saturation, making possible the investigation of the optimum matching conditions. The correct input matching is essential for the correct AUX turn-on and to sustain the DPA overall gain.

We demonstrated that nonlinear TCAD tools are mature enough to accurately model microwave circuits starting from the physical device structure. While in this work the transmission lines and matching networks are modelled as ideal components or idlers, a complete analysis of the amplifier layout at the physical level is possible following the guidelines shown in [15], where the passives are described by means of electromagnetic simulations coupled to the TCAD tool. Apart from the DPA design, this modelling approach can also be directly used to develop accurate black box models for fast circuit simulations, while retaining the link to the underlying physical device structure. Finally, the unique advantage of the presented approach is to allow for a higher level of device optimization compared to conventional DC and small-signal TCAD, since Large-Signal analysis allows to optimize the device structure and technology directly targeting the circuit-level performance typical of complex microwave power stages. Advanced, yet not entirely mature technologies, as GaN HEMT, are the ideal test-bed to exploit this capability for device optimization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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