The LiTE-DTU: a data conversion and compression ASIC for the readout of the CMS Electromagnetic Calorimeter

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***Abstract*—The High-Luminosity phase of operation of the CERN LHC collider (HL-LHC) will pose new challenges to the detectors and their readout electronics. In particular, the CMS barrel electromagnetic calorimeter will require a full redesign of the electronic readout chain in order to cope with the increase in luminosity and trigger rate.**

In this framework, a new Application Specific Integrated Circuit (ASIC) integrating A/D conversion, lossless data compression and high speed transmission has been developed and tested. The ASIC, named LiTE-DTU, is designed in a commercial CMOS 65 nm process and embeds two 12-bit, 160 MS/s Analog to Digital Converters (ADCs), a data selection and compression logic, and a 1.28 Gb/s output serial link. The high-speed 1.28 GHz clock is generated internally from the 160 MHz input by a clock multiplication Phase-Locked Loop (PLL).

The circuit has been designed implementing radiation tolerant techniques in order to work in the harsh environment of the HL-LHC upgrade. The LiTE-DTU is currently in the pre-production phase. A sample of 600 chips has been tested and incorporated into front end boards for systems performance testing.

***Index Terms*—Data conversion, Data compression, Radiation hardening electronics**

I. Introduction

THE Compact Muon Solenoid (CMS) [1] is one of the four detectors operating at the Large Hadron Collider (LHC) facility at CERN. CMS is a general purpose detector designed to observe new physics phenomena that can be produced by the high energy collisions at the LHC as well as to perform precision measurements.

A key component of CMS is its electromagnetic calorimeter [2], which has a very important role in the reconstruction and identification of electrons and photons, as well as for the measurements of jets and missing transverse energy.

The upgrade of the LHC accelerator to the high-luminosity phase (foreseen to start in March 2029) will increase the luminosity by a factor of five, up to $\sim 5\times10^{34}$ cm^{-2} s^{-1}, thus leading to an average of 150-200 collisions per bunch crossing. This increase in luminosity will pose new challenges to the detectors and their readout electronics. In particular, the barrel part of the CMS electromagnetic Calorimeter (BCAL) will require a full redesign of its readout electronics in order to cope with the more demanding operating conditions, while the endcap part will be fully replaced with new detectors and electronics.

The BCAL is made of 61200 $PbWO_4$ crystals coupled with avalanche photodiodes (APDs), divided into 2448 readout units. Each unit is made of a matrix of 5×5 crystals, coupled to silicon APDs to convert the light into an electrical signal.

The current readout architecture [3] is based on five readout boards, named Very Front-End (VFE), connected to a Front-End (FE) board. The VFE board hosts five electronic channels made of a multi-gain charge preamplifier and a four channel, 12-bit, 40 MS/s ADC which continuously samples and converts the three outputs (all from the same APD but with different gains). The ADC data from the five VFEs are sent to concentrator ASICs hosted on the FE board. At this stage the data are pre-processed and sent to the data acquisition and trigger systems via 1.28 Gb/s optical links. The pre-processing consists of a digital pipeline covering the L1 trigger latency, a primary event buffer that can contains up to 25 full events and a trigger primitive generator.

The LHC upgrade has a number of implications for the BCAL readout electronics. The need to cope with increased pile-up, combined with a higher rate of fake signals due to the direct interaction of collision particles with the APDs, necessitate an increase by a factor of four of the sampling frequency to maintain detector performance. These direct interactions generate a signal with a rise time of less than 10 ns, which is faster than the scintillation signal produced in the crystals, which have a rise time between 15 and 20 ns. Such a difference does not allow to suppress the former via analog filtering without significantly attenuate the latter, and thus a higher sampling rate is required to reject these unwanted signals [2]. Therefore a faster front-end amplifier, combined with a high sampling rate, high resolution ADC is needed. A fourfold increase of the sampling frequency leads to a corresponding increase of the data rate, which has to be handled properly. In order to cope with these stringent requirements, a new VFE

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board has been designed. Since the crystals and the APDs are not going to be replaced, the new board will keep the same five-channel modularity of the legacy one.

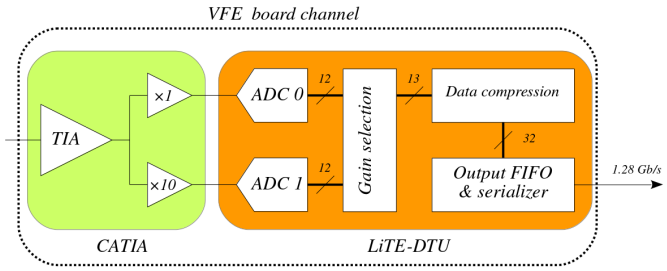

Fig. 1. VFE readout channel scheme.

The new VFE readout channel, shown in Fig. 1, is based on two ASICs, which have been developed specifically for this application. The first one, named CATIA, is a transimpedance amplifier and is connected to the APD via a short Kapton cable. The CATIA consists of a regulated cascode input stage followed by two voltage amplification stages working in parallel, with a gain ratio of 10 between the two. The second ASIC, named LiTE-DTU (Lisboa-Torino Ecal Data Transmission Unit, acquires the two CATIA outputs in parallel and converts them to digital format with two 12-bit, 160 MS/s ADCs. The resulting data streams are then fed to sample selection and data compression logic and finally transmitted to the FE board via a 1.28 Gb/s serial link.

A new FE board is also under design. This new board will host the lpGBT transceiver and the VTRx+ electro-optical converters [4], while the pre-processing functions are transferred to an FPGA-based Barrel Calorimeter Processor (BCP) board [5] located in an accessible position outside the cavern area. The lpGBT transmission rate is 10.24 Gb/s for the downlink and 2.56 Gb/s for the uplink, i.e. 10 times faster than the legacy system.

The ASICs are designed to be able to sustain a radiation level of up to 20 kGy. Their control logic part is protected against Single Event Upset (SEU) by Triple Modular Redundancy (TMR).

This paper is organized as follows: section II describes the LiTE-DTU architecture. The main building blocks, as well as the data selection and data compression algorithms are described in section III. Section IV describes the physical implementation and the techniques adopted for mitigation of radiation effects while sections V and VI show the test results.

II. LiTE-DTU ARCHITECTURE

The LiTE-DTU consists of two 12-bit, 160 MS/s ADC cores, a Data Control and Transmission Unit (DCTU) and four 1.28 Gb/s serializers. In normal operations, only one serializer is enabled. The others are used only to test the two ADC cores. Its architecture is depicted in Fig. 2.

The ADCs and the serializers require a 1.28 GHz clock, which is generated from the 160 MHz master one via a clock multiplication PLL. The LiTE-DTU operation is controlled by a set of fast commands sent via a 160 Mb/s serial link (*FastCmd* unit). These commands include separate reset signals for the LiTE-DTU units, the ADC calibration commands, and synchronization features designed to simplify the data time alignment of the full system performed by the BCP.

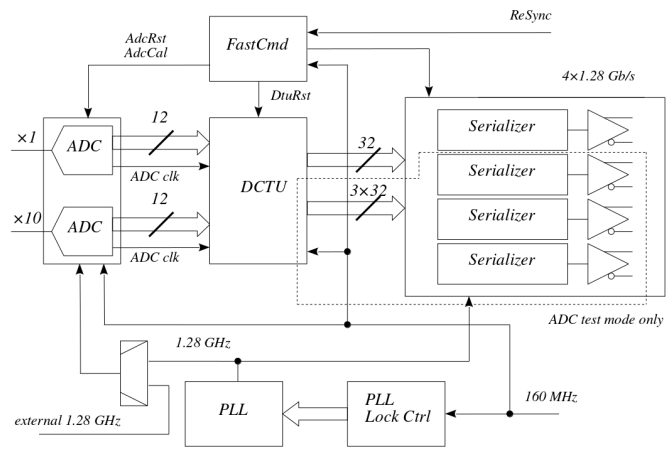

Fig. 2. LiTE-DTU architecture.

The DCTU performs data selection and compression in order to fit the data in a single 1.28 Gb/s serial link. However, it is possible to bypass the data processing and directly send the ADC raw data over four 1.28 Gb/s links. This operation mode is required in order to characterize the ADCs and makes the ASIC potentially interesting for other applications.

The LiTE-DTU can be programmed by a I^2C interface (not shown in the figure) that allows the setting of several parameters, including the selection algorithm tuning as well as enabling and setting the strength and pre-emphasis of the output drivers. The I^2C interface allows also tuning of the internal settings of the ADC and PLL IP blocks.

The main data path is depicted in Fig. 3. The two CATIA outputs are continuously converted by the two ADCs. The ADC outputs are stored in two 12-bit, 16-cells FIFOs which provide clock domain crossing (the ADCs are synchronous to the 1.28 GHz clock; their outputs are the 12 bit parallel bus and a 160 MHz output clock to be used for correct data sampling) and temporary storage to allow the data selection logic to choose the sample to be transmitted with a time window based algorithm described in section III-B. The unselected samples are discarded. After the selection process each sample is thus represented by 13 bits, since 1 bit is needed to specify the gain.

The raw output data rate from the LiTE-DTU after the sample selection logic is thus 2.08 Gb/s. However, for practical reasons, it is convenient (both in terms of reduction of the number of optical fibers and system modularity) to connect each LiTE-DTU to a single lpGBT e-link, which has a maximum data rate of 1.28 Gb/s. For this purpose a lossless data compression algorithm is implemented to fit the raw data rate into the e-link bandwidth. The algorithm takes advantage of the statistical properties of the signal from the detector, since the majority of the samples are centered on the CATIA baseline value.

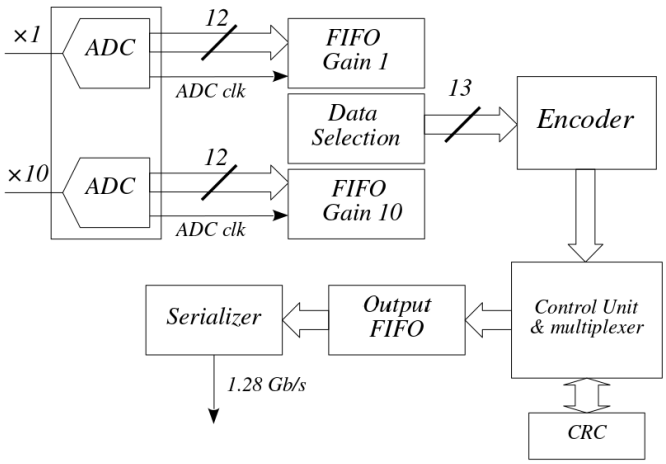

Fig. 3. LiTE-DTU data path schematic.

The compressed data are then stored in a 16-cell output FIFO, which is required to compensate for data rate fluctuations intrinsic to the compression algorithm. Detailed simulations of the LiTE-DTU Verilog code using data obtained from physics simulations as input stimuli have been performed and no data loss due to FIFO overflow has been observed in realistic conditions. The output data, formatted in 32-bit data words are transmitted in 50-word frames separated by a frame delimiter word. The latter contains the frame number, the effective number of samples present in the frame, and the Cyclic Redundancy Check (CRC) code of the frame. When no data is available for transmission, an idle word is sent to preserve the word alignment.

It should be noted that the LiTE-DTU does not trasmit the FIFO full condition. However, this condition is detected by the BCP since its input FIFO and decoder work with the same data rate as the LiTE-DTU encoder and thus mirrors the LiTE-DTU FIFO. Therefore a full condition on the LiTE-DTU corresponds to an empty condition in the corresponding BCP input channel. In this case the BCP will reset the LiTE-DTU FIFOs with a specific fast command in order to realign the data.

The LiTE-DTU can also be programmed to send data without compression. In this mode, two 13-bit samples are packed in a 32 bit word. The maximum data rate in this mode is 80 MS/s, and therefore only half the samples can be transmitted. However, this mode can be useful for very noisy channels where the compression algorithm is not efficient, since a halved sampling rate, albeit not optimal, still provides useful informations for data analysis.

The BCAL detector consists of 61200 readout channels, which have to be time-aligned at the BCP level. The synchronization is obtained by resetting all LiTE-DTUs at the same time. In order to monitor the status of the synchronization, a specific fast command is periodically sent to all LiTE-DTUs. When this command is received the LiTE-DTU controller sends the corresponding sample in a specific word, called the BC0 mark, devised to coincide with the first bunch crossing in the LHC orbit. The BCP can thus check whether all BC0 mark words arrive at the correct time and re-synchronize the channels if needed. This operation can be done by directly re-aligning the sample data in the BCP input FIFOs or by sending a flush command to all LiTE-DTU to reset the output FIFOs.

III. Building blocks

A. ADC core

The ADC core has been designed by an external company, Adesto [6]. It consists of two 12-bit, 80 MS/s cores that operate interleaved in time. Each core is a successive approximation ADC working with a 1.28 GHz master clock and a 160 MHz sampling one. The two clock frequencies must have a precise 8:1 ratio, i.e. they must come from the same source.

The ADC features a foreground calibration logic which has to be executed at the ASIC start-up and when the external conditions (mainly power supply and temperature) are changed. During calibration a constant differential signal close to the maximum range has to be provided from the outside. The calibration signal must be in the range 340÷350 mV for the positive input and 850÷860 mV for the negative one with a maximum noise of 1.6 mV r.m.s. The calibration information is stored in a set of SEU-protected registers (via TMR) and can be accessed externally both in read and write mode via an I^2C interface. In our system the calibration signal is provided by the CATIA in order to take into account effects due to the interconnections between the two ASICs.

The ADC is designed to provide a minimum ENOB of 10.2 up to the Nyqvist frequency with a power consumption below 20 mW. Table I summarize the ADC specifications.

TABLE I
ADC main specifications.

Specification	Value	Unit
N. of bits	12	
Max sampling rate	160	MS/s
Input voltage swing	±600	mV
Power supply	1.2± 10%	V
Power consumption	20	mW
Calibration time	160	μs
Min ENOB	10.2	
Max TID	20	kGy

B. Data selection

The data selection circuit operates as follows: the high gain input sample is selected unless it saturates the ADC input range. In this second case all the samples in a time window of -2/+5 sampling periods around the saturated one are selected from the low gain input. This simple algorithm ensures that whenever possible, the high gain input is selected (in order to maximize the ADC resolution) and also that samples belonging to the same detector signal are acquired from the same input gain, thus avoiding the need of a precise cross-calibration at the data analysis level.

If more than one high gain sample is saturated the window is automatically extended. The saturation threshold (i.e. the level above which the high gain sample is marked as saturated) is

programmable. Fig. 4 shows an example of signals coming from the two inputs and the corresponding gain selection output.

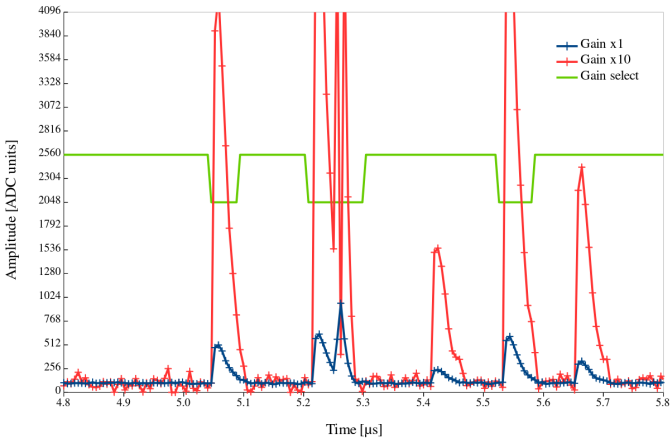

Fig. 4. Gain selection algorithm: the red and blue curves are examples of waveforms from the two inputs while the green line represents the gain selection switch.

The 8-sample window can be extended to 16 samples to have a measurement of the baseline with the same ADC, with the drawback of a decrease in the compression efficiency. Moreover, it is also possible to force the data selection logic to select a specific gain sample. Both settings are controlled by the I^2C interface.

C. PLL

The LiTE-DTU receives a 160 MHz master clock. However, both the ADC SAR logic and the serializers require a 1.28 GHz, low-jitter clock to operate. Jitter is of special concern for the ADCs, since it sets a limit on the maximum achievable ENOB for a given input frequency. A jitter lower than 5 ps r.m.s. is required to preserve the ADC resolution in the CATIA bandwidth. The 1.28 GHz frequency is provided by a clock multiplication PLL.

The PLL is based on the IP block designed for the lpGBT. The VCO runs at 5.12 GHz and is made of a LC resonator with a cross-coupled gm-cell topology in order to have low jitter. An improved variable capacitors connection scheme, proposed in [7], has been adopted to increase the tolerance to SEU. A disadvantage of this scheme is a reduced tuning range; therefore, to compensate for PVT variations, a digital control of the tuning range has been added via an array of variable capacitors that can be connected to the LC tank via switches.

D. Data compression

The data from the sample selection logic is compressed using a simplified Huffmann encoding algorithm [8]. The algorithm takes advantage of the statistical properties of the input signal, since the probability of having a sample with more than 6 significant (i.e. non-zero) bits is expected to be very low ($<2.4\times10^{-4}$). Therefore a simple compression scheme, based on the packet structure depicted in Fig. 5, has been implemented.

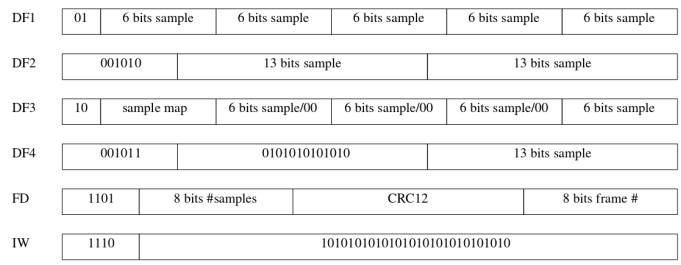

Fig. 5. LiTE-DTU output data format.

Samples below threshold are packed in groups of five in the 32-bit word, preceded by a two-bit header (DF1). The required bandwidth in this case is only 1.024 Gb/s, therefore an idle word (IW) is inserted when no data word is ready for transmission. On the other hand, if the samples are above threshold or from the low gain output, they are packed in groups of two (DF2). In this case the required bandwidth would be 2.56 Gb/s, twice that available. However, since this rate is required only for a short time, a 16-cell output FIFO is sufficient to compensate for the variation in the data rate. The algorithm has been extensively tested using both real and simulated physics data.

Data format DF3 and DF4 are used when there are not sufficient samples to fill DF1 and DF2, respectively, due to a transition between the two formats. As described in section II, a frame delimiter (FD) word is sent every 50 data words in order to provide control flow.

The compression algorithm is suboptimal since it does not take full advantage of the statistical properties of the samples; however it is simple to implement, fits into a fixed size 32-bit packet and provides compression at a level sufficient to fit into the lpGBT e-link. Since the algorithm is sensitive to the baseline level, two programmable registers which are subtracted from the input ADC values are implemented in order to provide fine tuning of the baseline value.

E. Data transmission

The output FIFO is serialized over a 1.28 Gb/s link. The serializer receives the 1.28 GHz clock from the PLL and has been implemented with standard logic cells. The serializer output drives a custom CLPS (CERN Low Power Signalling) current driver [9]. It is possible to control the driving current, pre-emphasis height and width, and polarity of the signal.

The choice of the CLPS standard for both the differential transmitters and receivers has been made to have full compatibility with the lpGBT.

IV. ASIC FLOORPLAN AND PHYSICAL IMPLEMENTATION

The LiTE-DTU ASIC has been designed in a commercial CMOS 65 nm technology. A first prototype to assess the building block performances has been designed and tested and is described in Ref. [10]. Then the final version, with the complete set of required features, has been designed and tested and is currently in the pre-production phase; 600 ASICs have been produced and tested.

Fig. 6 shows a photo of the ASIC. The die size is 2×2 mm^2 and is packaged in a QFN72 low profile package.

The ASIC has been designed to be radiation tolerant; for this purpose, no thick oxide transistor has been used and minimum W transistors have been avoided in the analog part [11]. The control logic has been protected against SEU via TMR using the TMRG tool [12]. A minimum distance of 20 μm has been forced between flip-flops of the same triplication group in order to avoid that a double upset induced from the same particle will affect the same memory bit, thus leading to a wrong correction.

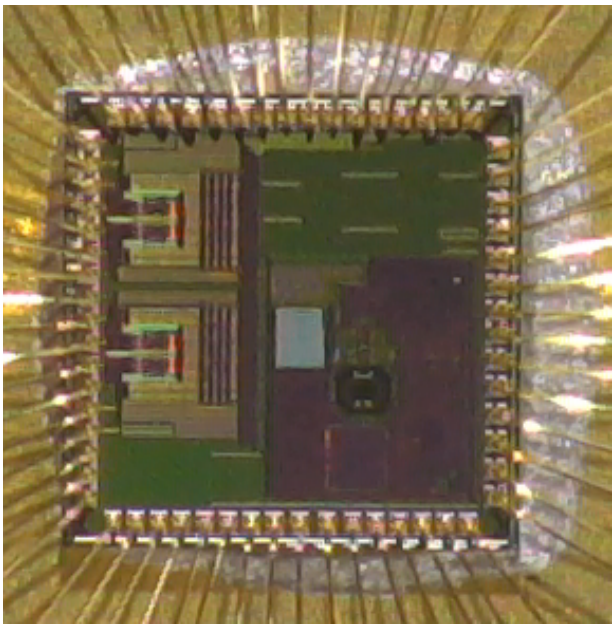

Fig. 6. LiTE-DTU photo.

A different technique for SEU protection has been implemented for the I^{2}C interface, since this block has no running clock in normal operation. Therefore an asynchronous load signal is generated when a SEU is detected in order to immediately correct the register value. The scheme is described in more details in [13]

V. Test results

The LiTE-DTU has been extensively tested both standalone and coupled with the CATIA preamplifier. In the standalone set-up, the input signal is provided by a signal generator, while the output data are read-out by an FPGA and sent to the acquisition computer via a UDP-based Ethernet link.

After assessing the functionality of the control logic and the data selection and compression system, the tests have focused on the performances of the ADCs and the PLL. The two are strictly correlated since the ADC SNDR is limited by the sampling clock jitter according to the formula [14] :

$$SNDR_{max} = 20log_{10}\left[\frac{1}{2\pi f_{sig} t_j}\right],$$

where SNDR is the Signal-to-Noise and Distortion Ratio, f_{sig} is the input signal frequency, and t_j is the r.m.s. jitter of the sampling clock. From this formula it can be seen that to obtain an ENOB of 10.2, which corresponds to a SNDR of 63 dB, the maximum jitter that can be tolerated is quite demanding: 5.6 ps for a 20 MHz signal and 2.2 ps for 50 MHz.

In order to disentangle the contribution of the internal PLL jitter from the ADC performance, the test has been performed by injecting sine waves of different frequencies [15] and providing the sampling clock both from the internal PLL and an external, very low jitter source. The FFT obtained in the two cases with an input signal of 20 MHz are shown in Figs. 7 and 8, respectively.

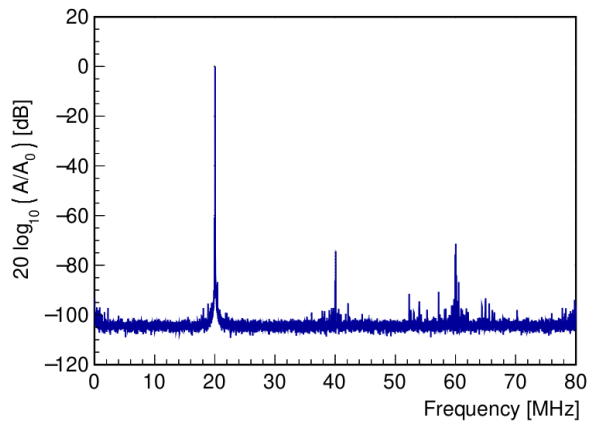

Fig. 7. FFT of the digitized signal with a 20 MHz input sine wave and internal clock.

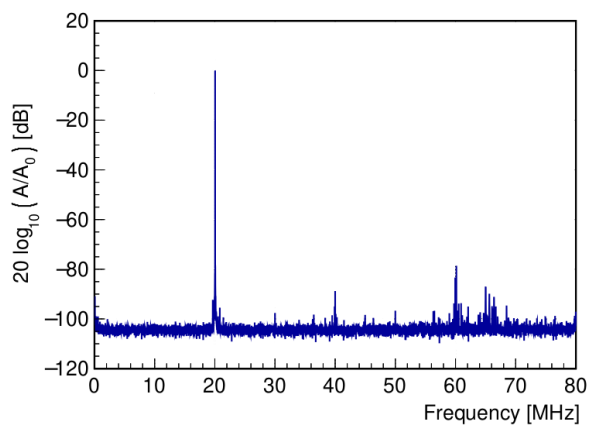

Fig. 8. FFT of the digitized signal with a 20 MHz input sine wave and external clock.

The two FFTs are quite similar and shows a very low noise floor (more than 100 dB below the fundamental tone) and a second and third harmonic below 75 dB. However, a broadening of the spectrum around the fundamental tone at 20 MHz for the first case shows that the PLL jitter is higher than the one from the external clock generator. The difference in the resulting ENOB is more visible in Fig. 9, where the ENOB is plotted as a function of the input frequency. The improvement observed with a 40 MHz input signal for the internal clock case is due to the fact that a significant component of the jitter is due to an interference of the 40 MHz

clock signal from the PLL. The resulting spurs are either superimposed on the input tone or pushed to 0 and 80 MHz (for the $f_{IN}\pm40$ MHz tones) when the input sinewave is at this specific frequency.

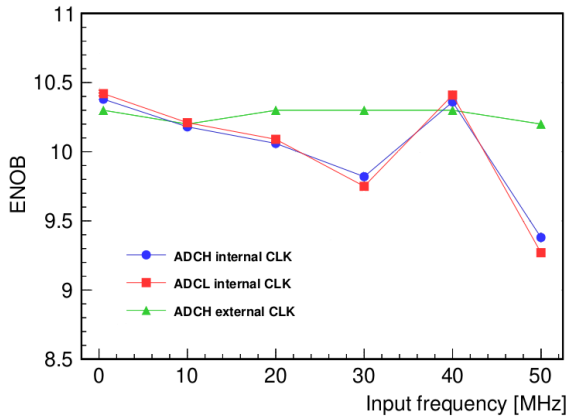

Fig. 9. ENOB as a function of the input frequency.

These measurements put an upper limit on the jitter from the external and internal clock sources of 2.2 and 4.0 ps r.m.s., respectively. Measurements on the PLL test output has shown that the main component of the PLL jitter is due to the digital activity of the other parts of the LiTE-DTU. In particular, a modulation due to the 160 MHz has been clearly observed via N-cycle jitter measurements. The reported jitter value is a significant improvement with respect to the results of the first prototype, obtained by extensive on-chip power filtering and by fully separating the PLL supply pads.

The LiTE-DTU has been intensively tested coupled with the CATIA amplifier in order to evaluate the performance of the final system in terms of time resolution and linearity. In order to evaluate the intrinsic time resolution of the system, the same input signal has been sent to all 5 channels of a VFE card. The time resolution has been calculated by taking one channel as a reference and comparing the other channels with the reference one for different input pulse amplitudes. The result is shown in Fig. 10, while Fig. 11 shows the integral non-linearity of the front-end readout chain for the two CATIA gains.

These results demonstrate that overall performance is on target for the system requirements, even with the small degradation of the ADC ENOB due to the PLL clock jitter.

VI. Radiation Test Results

The LiTE-DTU was irradiated to verify its tolerance to total ionizing dose (TID) damage with 10-keV X-rays up to 50 kGy at the INFN Padova X-ray irradiation facility. The dose rate was 15.5 Gy/s. During irradiation the ASIC was powered and with running clock. The measurements have been taken with the beam off at 5, 10, 20, 30 and 50 kGy dose intervals. The last value is approximately 2.5 times higher than the dose expected in the BCAL after 10 years of operation.

No variation has been observed in the performance of the LiTE-DTU. Indeed, the same technology has been successfully tested at much higher doses by other research groups [11].

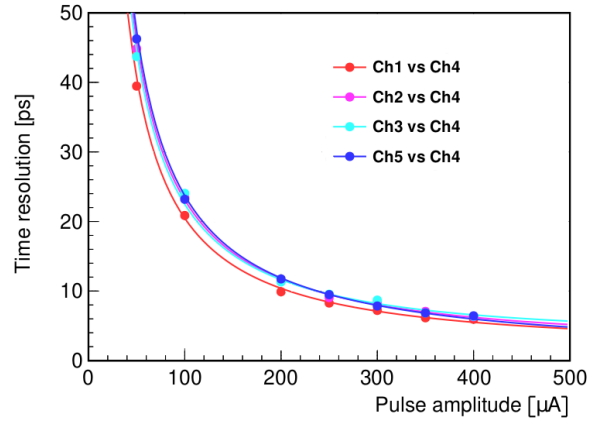

Fig. 10. Front-end intrisic time resolution.

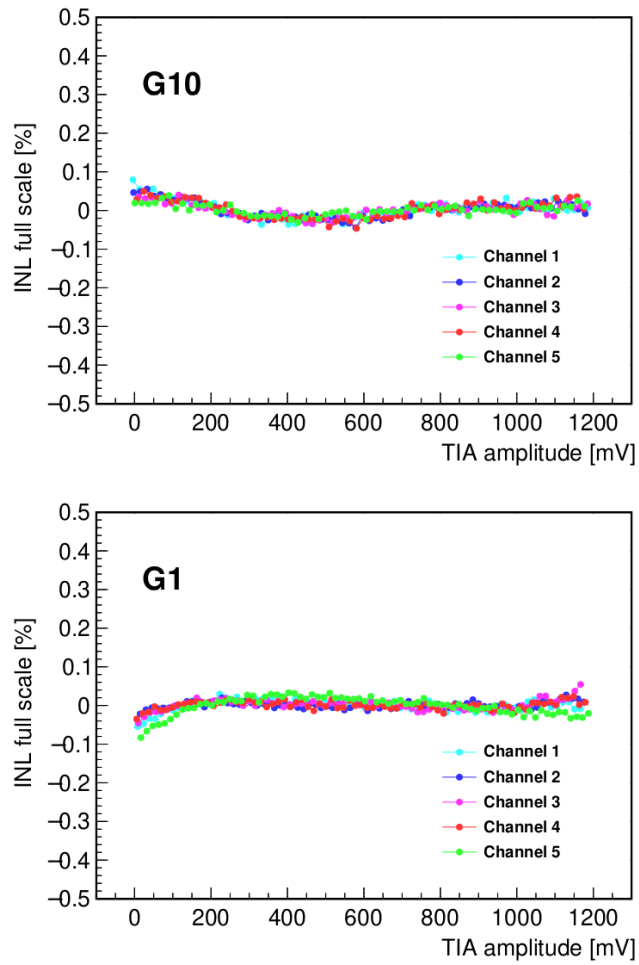

Fig. 11. Integral non-linearity for the two gains.

The LiTE-DTU has also been tested for SEU tolerance both at the CRC facility of the Université Catholique de Louvain-la-Neuve and at the SIRAD facility of the INFN Laboratori Nazionali di Legnaro. Table VI shows the cocktail of ions used for the test.

TABLE II
IONS AND ENERGIES USED IN THE SEU TESTS.

Ion	Energy [MeV]	LET [MeV cm^2/mg]	Fluence [ions/cm^2]	Facility
F	122	3.67	5.00×10^7	SIRAD
Si	157	8.59	5.01×10^7	SIRAD
Ar	353	9.90	1.67×10^7	CRC
Cl	171	12.50	1.40×10^8	SIRAD
Cl$^{(*)}$	171	14.43	4.26×10^7	SIRAD
Cr	505	16.10	1.78×10^7	CRC
Ni	582	20.40	7.14×10^6	CRC
Ni	220	28.40	4.60×10^7	SIRAD
Kr	769	32.40	4.07×10^6	CRC
Br	241	38.60	5.45×10^7	SIRAD

$^{(*)}$ *sample tilted by 30°*

Fig. 12 shows the measured cross section per bit for the I^{2}C registers. When no SEUs have been detected, a red dash, representing the measurement upper limit for the corresponding fluence, is represented. The experimental points have been fitted with a Weibull function in order to estimate the proton cross section in the LHC environment, following the methology proposed in [16].

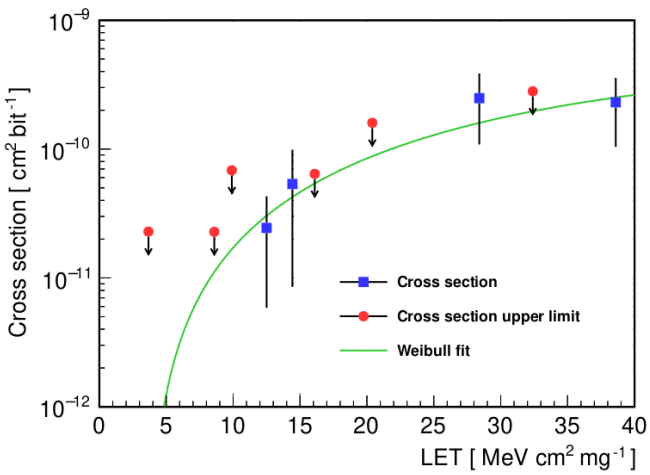

Fig. 12. Cross section and Weibull fit for the I^{2}C interface.

With the proposed method, a proton cross section of about 6.8×10^{-18} cm^2/bit has been obtained. This value corresponds to an average SEU rate of about 9×10^{-5} errors/h per chip, i.e. 5.5 errors/h in the entire BCAL. This is considered acceptable since the CMS experiment foresees a re-configuration time interval of the order of a few minutes. Owing to the large error bars, the calculated fit is affected by a significant uncertainty. However, changing the fit parameters in the error range lead to similar values of average time between SEU events.

The cross section for the LiTE-DTU data path is shown in Fig. 13. In this case the cross section is significantly higher, since the ADC data registers are not SEU-protected. However, a bit flip in the ADC corrupts just one sample and therefore is much less critical with respect to the configuration registers.

Following the same method, a proton cross section of 9.4×10^{-13} cm^2 per chip has been obtained, corresponding to

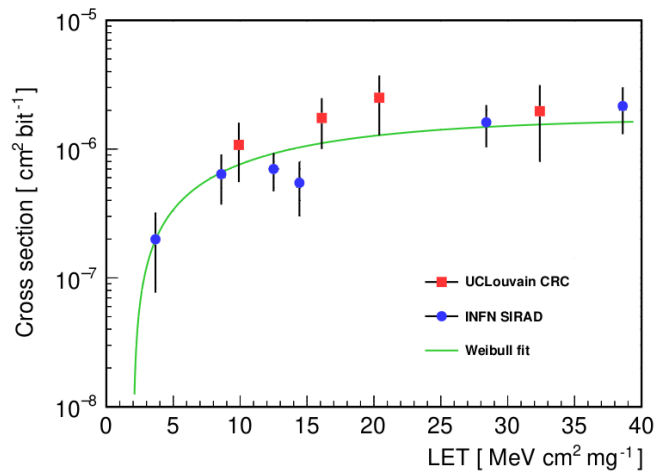

Fig. 13. Cross section and Weibull fit for the data path.

10.2×10^{-3} errors/h per chip, i.e. ~627 errors/h in the full barrel.

VII. PRE-PRODUCTION TESTS

A pre-production of 600 dice has been done in order to equip the 400 readout channels required for the large scale integration test of the CMS BCAL performed on autumn 2022. The test setup consists of a test board with a ZIF socket, a commercial FPGA test board, a low jitter clock source (<2 ps) and two arbitrary signal generators. The FPGA interface and the signal and power supply instruments are controlled by a custom test interface written in Python.

The test sequence is the following :

- Supply current check
- Bit and data alignment
- ADC calibration and sinewave acquisition
- Test pulse scan for both gain $\times1$ and gain $\times10$ inputs

Test of 553 dice resulted in 535 working ones, corresponding to a yield of 96.7%. With such a high yield, a wafer-level test is deemed not necessary, and therefore the dice will be tested only after packaging. Regarding the 18 non-working dice, 10 exhibited a noise higher than 1 ADC count r.m.s., 1 showed ADC calibration issues, 6 failed the alignment test, and 1 showed major issues in the digital logic.

VIII. CONCLUSIONS

A data conversion and compression ASIC, called LiTE-DTU, has been developed for the upgrade of the CMS electromagnetic calorimeter. The ASIC, designed in a commercial CMOS 65 nm technology, consists of two ADC cores with a resolution of 12 bits and a sampling frequency of 160 MS/s, a data processing unit to reduce the amount of data to be transmitted, a 1.28 Gb/s serializer, and a I^{2}C interface for configuration.

The ASIC, designed to be radiation tolerant, has been extensively tested both in laboratory and integrated in readout chain for beam tests. Tests show that the ASIC performance

is fully adequate for the BCAL requirements. Radiation tests have been performed in order to verify the radiation tolerance.

A sample production has been tested, showing excellent yield. This indicates that the design is ready for mass production and use in the CMS detector.

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