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# pMOS-only pW-Power Voltage Reference with sub-10 ppm/°C Trimmed Temperature Coefficient and sub-100 ppm/V Line Sensitivity

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**Abstract**—In this paper, a new ultra-low-power voltage reference based on a two-stage, all-pMOS topology operating in the subthreshold region is proposed to uniquely meet the pW-power range power consumption requirements of emerging Internet-of-Things applications without significantly compromising the Temperature Coefficient (TC) and the Line Sensitivity (LS) performance. The proposed circuit consists of the LS regulator, TC corrector, and TC trimming sections. Based on post-layout Monte Carlo simulations in 180 nm CMOS, the proposed circuit operates with 0.8 V to 2.4 V supply potential and generates a reference voltage of 206 mV with a process spread of 7.8%, achieving an average calibrated TC of 4.4 ppm/°C in the temperature range of -20 °C 80 °C, and an average LS of 51.5 ppm/V with a power consumption of 25.9 pW at 25 °C (469.1 pW at 80 °C).

**Index Terms**— Voltage Reference Generator, Low power, LS Regulator, Temperature Compensation, Subthreshold Region.

## 1. Introduction

Analog integrated circuits require voltage references as part of their design. With the IoT era's emergence, power consumption reduction in circuits is receiving more attention than ever before. Since voltage reference generators are always-on in most duty-cycled IoT nodes, their contribution to the average power budget can be easily dominant and should be reduced to the sub-nW level to allow operation from small batteries or energy harvesters [1]. Various transistors, such as BJT, MOSFET and OFET, can be used to implement voltage references [2, 3]. Bandgap Voltage References (BGRs) usually need high supply voltage and their power consumption is usually in the  $\mu$ W range or above [4]. A solution to reduce supply voltage and power consumption is to replace BJT transistors with MOSFETs in the subthreshold region for temperature compensation. However, this approach results in larger TC and generally worse performance [5]. Various effects, such as diode leakage currents and the dependence of the reference voltage on the threshold voltages, are responsible for this degradation. The TC can be enhanced by biasing the transistors in Zero Temperature Coefficient (ZTC) operation point [6]. Despite this technique's effectiveness in reducing the TC, it increases power consumption due to the required operating point. The effect of the process-related threshold voltage spread on the reference voltage is compensated by body bias in stacked nMOS transistors in [7]. Nevertheless, it does not have a favorable TC.

Various structures have been proposed to reduce the TC in sub-threshold MOSFET reference circuits [8]. However, the achieved TC is not comparable to modern BGRs, which have a TC of about 1 ppm/°C [9]. Using a combination of MOSFETs and BJTs, a high-order temperature-compensated reference circuit is presented in [10], which achieves a TC under 10 ppm/°C; however, that reference still requires hundreds of nanowatts to operate. In [11], at high temperatures, the Bulk Diode Leakage Current Modulation (BDLCM) effect of the pMOS transistor changes the curvature of the output voltage versus temperature, thus improving TC in a wider temperature range. Using different types of transistors (pMOS and nMOS) a full compensation of the mobility thermal drift is not possible with this structure.

There are some effective methods to enhance LS, such as LS regulator transistor [12] and two-stage structure [13]. By adopting a two-stage structure and increasing the length of the current source transistors in the first stage, the LS has been decreased down to 154 ppm/V in [14]. Power consumption greater than 1 nW and TC of 89.8 ppm/°C are however disadvantages of this approach [14]. The circuit presented in [15] has a suitable LS of 143.8 ppm/V and a power consumption of 19.1 pW. The desirable LS of [15] has been obtained using a two-stage structure [13] and a DIBL effect compensator [16]. Additionally, controlling the current transistor in the second stage reduces the TC to

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39.2 ppm/°C without trim and 20.8 ppm/°C with trim. Using a series connection of the switches with the trimming transistors in [14, 15] leads to an increase in the occupied area, a variable load leakage diode and increased power consumption. Therefore, a new trim circuit is needed in ultra-low power designs to reduce leakage current in off-state.

In Table 1, several voltage reference structures are summarized and qualitatively compared. As seen from the Table, two-stage structures can result in low LS values. However, the reduction of TC has not yet been thoroughly investigated in two-stage structures. Recent work shows that, if not canceled out, nwell and drain/source parasitic diode leakage currents can significantly degrade TC. Conventionally, reducing power consumption will result in a deterioration in TC. However, as seen in Table 1, with diode leakage compensation, ultra-low power voltage reference generators can be obtained with a slight degradation of TC [16]. Although the effect of leakage diodes between the body and substrate is canceled by imposing a junction voltage  $V_{j0}$ , this structure still suffers from leakage diodes between the source/drain and the body.

Table 1- Summary of quantitative comparison of low power voltage references

Reference Voltages in literatures	Structure	LS	TC	Power	Diode leakage compensation
[17]	One-stage	High	Medium	Low	×
[18]	One stage	High	Medium*	Ultra-low	✓
[14]	Two-stage	Low	Medium	High	×
[15]	Two-stage	Low	Medium	Low	×
<b>Design trend</b>	Two-stage	Low	Low	Low	✓

\*This TC is achieved in ultra-low power conditions

As reported in Table 1, the current work's design trend is to obtain low LS and low TC values in low-power voltage reference generators. For this purpose, a two-stage structure with diode leakage compensation will be presented. In this paper, the two-stage voltage reference generator uses only pMOS transistors. In the first stage, a modified version of the circuit in [17] is adopted to feed the proposed second stage reference generator. The number of stacked transistors in the first stage is adjusted as required to enhance LS while keeping a reasonably low minimum supply voltage of 0.8 V. In addition, an LS regulator transistor is introduced in the second stage to reduce the LS further. The second stage's self-biased circuit is intended for temperature compensation. By canceling out the non-idealities introduced by parasitic diodes leakage current and including a trimming network, sub-10 ppm/°C operation over the -20 °C to 80 °C temperature range under process variations and mismatch is achieved. Trimming transistors apply constant leakage diodes to the output, resulting in a constant size leakage diode regardless of the trim code.

The rest of the paper is organized as follows: the proposed design is introduced in section 2, entering into the details of the TC corrector, the LS regulator, and the TC trimming circuit. In Section 3, some design considerations for the proposed voltage reference are offered. Section 4 reports the results of the circuit simulations along with the results of the Monte Carlo analysis. A comparison with the state-of-art is also proposed in the same section. Some concluding remarks are finally drawn in Section 5.

## 2. The Proposed Voltage Reference

### 2.1 Description

Fig. 1 shows the architecture of the proposed voltage reference. Instead of using transistors of the same flavor, the circuit takes advantage of thick and thin oxide pMOS transistors to increase the output voltage by one order of magnitude, from a few tens of millivolts to about two hundred millivolts [19, 20]. Stacked thin oxide devices can be used instead of  $M_5$  at the output to produce the same amount of  $V_{REF}$ , however the drain-source potential on each transistor will be in the thermal voltage range and thus these transistors will operate in the subthreshold triode region. In this region the transistors drain current has strong dependence on the drain-source potential and the conditions required for the proposed temperature compensation method will be violated. The body effect and the effects on the thermal drift of the current flowing through the reverse-biased source-body junctions are suppressed by connecting the body to the source in all transistors.

A two-stage structure is adopted to improve the LS, as in [13-15]. When using a two-stage configuration, it is crucial to ensure that the output voltage of the first stage can provide a supply voltage for the second stage above the minimum requested for proper operation. According to Fig. 1, in particular, it should be:

$$V_{REG1} > V_{REF} + V_{SD,7}(min) + V_{SD,8}(min) = V_{REG1,min} \quad (1)$$

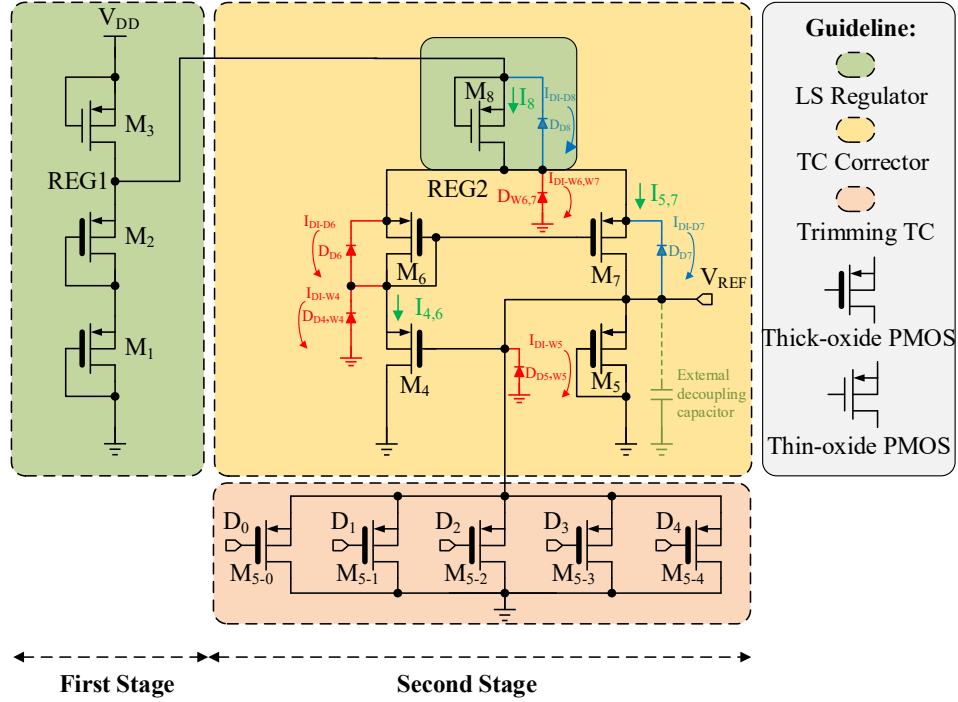


Fig. 1. The proposed voltage reference along with leakage diodes

where  $V_{REF}$ ,  $V_{SD,7}$ ,  $V_{SD,8}$  are the reference voltage, and the source-drain voltages of  $M_7$  and  $M_8$ , respectively. It will be shown that the reference voltage is obtained as the difference of threshold voltages, and is about 205 mV.  $V_{SD,7}$  is controlled by  $V_{SG,4}$  and  $V_{SG,6}$ , meanwhile  $V_{SD,8}$  is set by the aspect ratio of  $M_8$ . In the proposed design, the minimum source-drain potentials, on average, are considered to be about 200 mV, reducing the bias current's dependence on the drain-source potential [17]. Based on (1), the first stage should provide a minimum supply voltage of more than 600 mV for the second stage. In designs such as [13-15], the first stage output voltages are lower than 400 mV and are therefore too low to satisfy (1), thus resulting in a high  $LS$ . In order to meet (1), assuming a minimum voltage of 200 mV for  $V_{SD,3}$ , it follows that the minimum supply voltage of the overall circuit will be approximately 800 mV. Compared to [17], the native nMOS transistor is replaced with a pMOS. Using the same type of transistors leads to smaller output voltage variations. In addition, compared to [21] and [22], two types of transistors (thick and thin oxide) are used to produce the desired output voltage with fewer transistors. The body effect is removed from  $M_3$ , which decreases  $V_{TH3}$  and increases  $V_{REG1}$ . The aspect ratio of  $M_1$  and  $M_2$  is leveraged to set the output voltage, while the aspect ratio of  $M_3$  decides the total current of the proposed circuit. Since the temperature changes of  $V_{REG1}$  are attenuated at the output by the  $LS$  factor of the second stage, the  $TC$  of the two-stage structure is mainly related to the  $TC$  of the second stage [13, 15], and it is not necessary to compensate the temperature variation of the first stage output voltage.

## 2.2 Diode leakage compensation

Diode leakage currents play a crucial role in the temperature compensation of pW voltage reference generation circuits [8]. This current can be expressed as follows [23]:

$$I_{DI} = I_S(\exp(V_D/\eta V_T) - 1) \quad (2)$$

where  $I_S$  is the saturation current,  $V_D$  is the diode bias voltage,  $\eta$  is the ideality factor, and  $V_T$  is the thermal voltage equal to  $k_B T/q$  (with  $k_B$  the Boltzmann's constant,  $T$  the Kelvin temperature, and  $q$  the electron charge). The exponential term in (2) can be ignored in this design, since  $V_D$  is negative enough. Hence,  $I_{DI}$  can be obtained by [23] as:

$$I_{DI} \approx -I_S = -Aqn_i^2 \left( \frac{D_p}{X_p N_D} + \frac{D_n}{X_n N_A} \right) \quad (3)$$

where  $A$  is the diode junction area,  $q$  is the electron charge,  $D$  is the diffusion constant, and  $X$  is the diffusion length with a subscript of  $n$  for  $n$ -type and  $p$  for  $p$ -type silicon.  $N_D$  and  $N_A$  are the concentrations of holes and electrons respectively, and  $n_i$  is the intrinsic carrier concentration, whose dependence on temperature is given by the following expression [24]:

$$n_i(T) = 5.29 \times 10^{19} (T/300)^{2.54} \exp(-6726/T) \quad (4)$$

Due to the dependence of  $n_i$  on temperature,  $I_S$  is temperature dependent.  $V_{REF}$ 's temperature drift can be improved by canceling  $I_S$  with other second-order effects in the desired temperature range. Since the second stage plays the role of temperature compensator, all the relevant leakage diodes are included in Fig. 1. Two types of leakage diodes exist. Pull-up diodes that eventually inject current into the output node which are shown with blue color and, pull-down diodes that eventually sink current from the output node and are shown in red color. Diodes  $D_{D7}$  and  $D_{D8}$  are drain-body leakage diodes of  $M_7$ , and  $M_8$  transistors act as pull-up diodes, and other diodes including drain-body leakage diodes and  $n$ -well diodes act as pull-down diodes. Aiming to reduce the effects of leakage on the output reference voltage drift, the aspect ratio of  $M_8$  is chosen large enough, so that its nominal current is dominant compared to leakages over the whole temperature range (as the bias current increases, the effect of leakage diode currents becomes negligible up to higher and higher temperatures, since they account for a smaller percentage of the total bias current). The width of  $M_7$  is also adjusted so that  $I_{DI,W5}$  is negligible in the desired temperature range. The effectiveness of the approach will be confirmed by simulations.

### 2.3 First-order temperature compensation

In the second stage,  $M_8$  supplies a low LS current to the TC Corrector section to generate a first-order temperature compensated reference voltage, as detailed in what follows.

The proposed circuit operates in the sub-threshold region and the drain current can be therefore expressed [2]:

$$I_D = \mu_p C_d \frac{W}{L} V_T^2 \exp\left(\frac{V_{SG} - |V_{TH}|}{nV_T}\right) \left(1 - \exp\left(\frac{-V_{SD}}{V_T}\right)\right) \quad (5)$$

where  $C_d$  is depletion region capacitance,  $n$  is the subthreshold slope factor, and  $\mu_p$  is the hole mobility.  $V_{SG}$ ,  $V_{SD}$ , and  $V_{TH}$  are source-gate, source-drain, and threshold voltages, respectively. Assuming  $V_{SD} > 4V_T$ , the dependence of  $V_{SD}$  is ignored in what follows.

Based on (5), the reference voltage can be therefore expressed as

$$V_{REF} = |V_{TH,5}| + n_H V_T \ln\left(\frac{I_5}{\mu_p C_{d,H} (W/L)_5 V_T^2}\right) \quad (6)$$

where  $I_5$  denotes the drain current of  $M_5$  and subscripts  $L$  and  $H$  refer to thin/thick oxide transistors, respectively. considering that

$$I_8 = I_6 + I_7 \quad (7)$$

and

$$I_6 = \frac{(W/L)_6}{(W/L)_7} \times I_7 \quad (8)$$

The current  $I_5 = I_7$  in (6) can be expressed as

$$I_5 = I_7 = \mu_p C_{d,L} \left( \frac{(W/L)_7 \cdot (W/L)_8}{(W/L)_6 + (W/L)_7} \right) V_T^2 \exp \left( \frac{-|V_{TH,8}|}{n_L V_T} \right) \quad (9)$$

Substituting (9) in (6),  $V_{REF}$  is therefore given by:

$$V_{REF} = |V_{TH,5}| - n_R |V_{TH,8}| + n_H V_T \ln \left( \frac{C_{d,L}}{C_{d,H}} \cdot (W/L)_R \right) \quad (10)$$

where  $(W/L)_R = [(W/L)_7 \cdot (W/L)_8] / [(W/L)_5 \cdot ((W/L)_6 + (W/L)_7)]$  and  $n_R = n_H / n_L$ .

The temperature dependence of the threshold voltage can be expressed as follows [15]:

$$|V_{TH}| = |V_{TH}(T_0)| + \alpha(T - T_0) \quad (11)$$

where  $\alpha$  is the slope of the temperature variation in the threshold voltage,  $T_0$  is the reference temperature, and  $|V_{TH}(T_0)|$  is the threshold voltage at the reference temperature. The appropriate aspect ratio for temperature compensation using (11) in (10) is achieved by imposing  $\frac{\partial V_{REF}}{\partial T} = 0$  and is:

$$\left( \frac{W}{L} \right)_R = \frac{C_{d,H}}{C_{d,L}} \cdot \exp \left( \frac{q}{n_H k_B} (n_R \alpha_8 - \alpha_5) \right) \quad (12)$$

Therefore, the output reference voltage after temperature compensation is finally expressed as:

$$V_{REF} = |V_{TH,5}(T_0)| - n_R |V_{TH,8}(T_0)| + (n_R \alpha_8 - \alpha_5) T_0. \quad (13)$$

## 2.4 LS Regulator

The first stage of the proposed circuit (Fig. 1) is the initial LS regulator. A current almost independent of the supply voltage is produced from the gate-source connection of  $M_3$  [12]. Transistor  $M_8$  further improves the LS by acting as a current source for the TC Corrector section and playing the role of a second LS regulator. In this section, the expression of the LS is derived and adopted to predict the LS of the proposed design.

Considering  $V_{REG1,max}$ ,  $V_{REG1,min}$ , and  $V_{REG1,mean}$  as the maximum, minimum, and mean of the first stage output voltage, respectively, and also  $V_{DD,max}$  the maximum supply voltage, and  $V_{DD,min}$  the minimum supply voltage,  $LS_1$  is defined by [25]:

$$LS_1 = \frac{\Delta V_{REG1}}{V_{REG1,mean} \times \Delta V_{DD}} \quad (14)$$

where  $LS_1$  is LS of the first stage,  $\Delta V_{REG1} = V_{REG1,max} - V_{REG1,min}$  and  $\Delta V_{DD} = V_{DD,max} - V_{DD,min}$ . Considering  $V_{REF,max}$ ,  $V_{REF,min}$ , and  $V_{REF,mean}$  as the maximum, minimum, and mean of the reference voltage, respectively,  $LS_2$  is defined by

$$LS_2 = \frac{\Delta V_{REF}}{V_{REF,mean} \times \Delta V_{REG1}} \quad (15)$$

where  $LS_2$  is LS of the second stage and  $\Delta V_{REF} = V_{REF,max} - V_{REF,min}$ . With definitions of (14) and (15), the LS of the proposed circuit can be expressed as follows:

$$LS_{pr} = LS_1 \times LS_2 \times V_{REG1,mean} \quad (16)$$

The drain current shows some supply voltage dependence, mainly due to the DIBL effect. This effect can be expressed as

$$V_{TH} = |V_{TH0}| - \lambda_D V_{SD} \quad (17)$$

where  $\lambda_D$  is the DIBL factor, and  $V_{TH0}$  is the threshold voltage at  $V_{DS}=0$ . The small-signal equivalent circuit of the first stage is shown in Fig. 2. As  $M_1$  and  $M_2$  are of the same type and have the same drain current,  $g_m$  is nominally identical for both transistors.  $LS_1$  using (5), (14) and (17) is given by

$$LS_1 = \frac{2}{g_{m1}r_{o3}V_{REG1}} = \frac{2N_R\lambda_{D3}}{V_{REG1}} \quad (18)$$

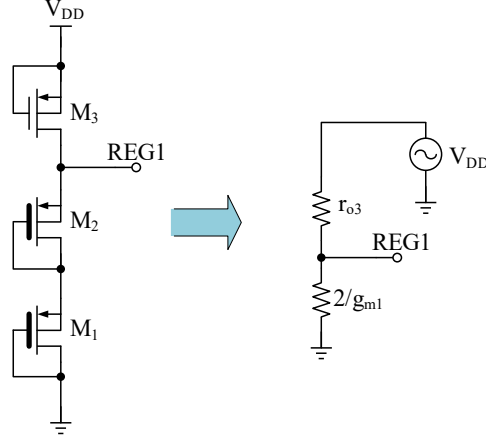


Fig. 2- Small-signal equivalent of the first stage

The second stage of the proposed circuit contains feedback of  $M_4$ ,  $M_6$ , and  $M_7$ . The small-signal equivalent resistance  $R_{th}$  is calculated based on the circuit Fig. 3 as follows

$$R_{th} = \frac{3}{(K+1)g_{m6}} \quad (19)$$

where  $K=(W/L)_7/(W/L)_6$ . Subsequently, assuming that  $K$  is large enough,  $LS_2$  can be expressed by

$$LS_2 \approx \frac{n_R\lambda_{D8}}{V_{REF,mean}} \quad (20)$$

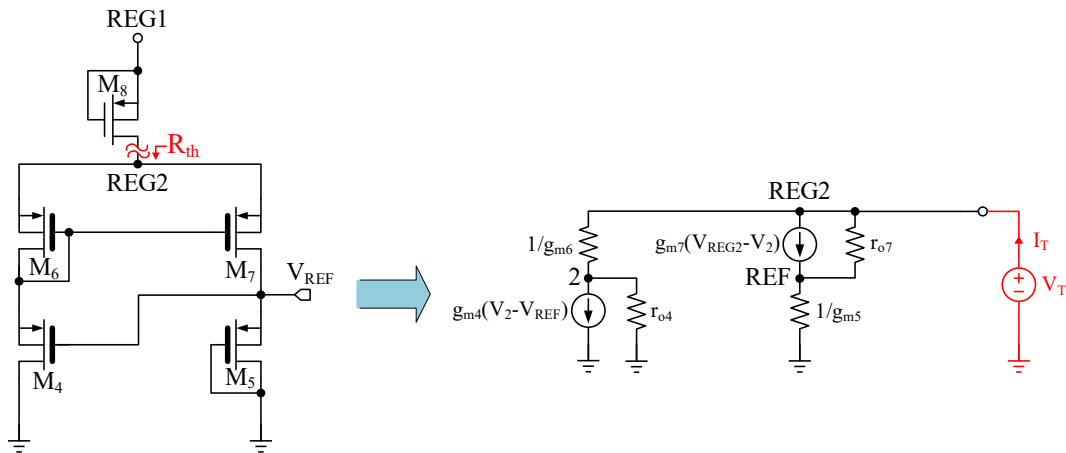


Fig. 3- Small-signal equivalent of the second stage

Thus, the  $LS$  of the whole circuit can be obtained by placing equations (18) and (20) in (16).

$$LS_{pr} = \frac{2n_R^2 \lambda_{D,3} \lambda_{D,8}}{V_{REF,mean}} \quad (21)$$

In the proposed circuit,  $\lambda_{D,3}$  and  $\lambda_{D,8}$  are  $9 \times 10^{-4}$  and  $17.7 \times 10^{-4}$ , respectively, and  $n_R$  is 1.336. Thus,  $LS_{pr}$  is estimated at 27.7 ppm/V using theoretical elaborations.  $V_{REF}$  versus supply voltage for a typical corner is plotted in Fig. 4. Non-ideal effects increase  $LS$  from the predicted value to 47.9 ppm/V for supply voltages from 0.8 V to 2.4 V.

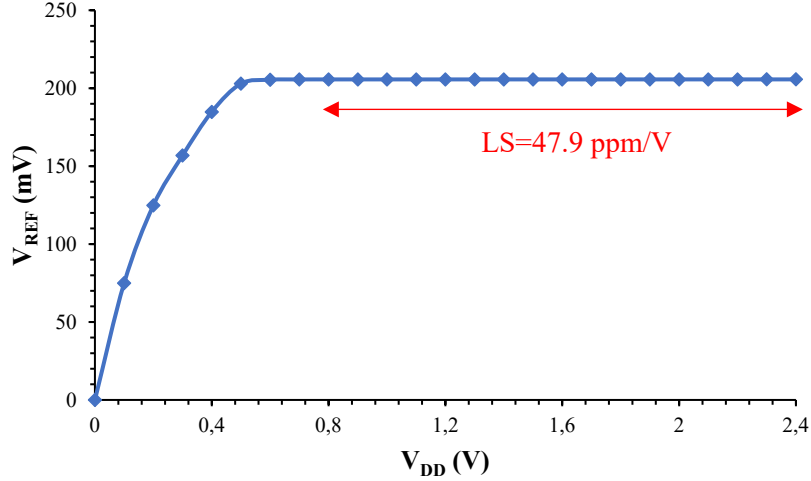


Fig. 4-  $V_{REF}$  versus supply voltage from 0 V to 2.4 V at 25 °C in a typical corner

## 2.5 TC trimming

Process variations affect transistor parameters, and as a result, the TC of a voltage reference can be degraded due to deviation from the compensation design set point. Trimming circuits can be used to tune the designed circuit under different process conditions and in order to compensate device mismatch. A 5-bit TC trim circuit for tuning the  $M_5$  aspect ratio is adopted here and shown in Fig. 1. With the increase in the number of bits, better TC would be achieved, however, at the cost of more complexity and area. Conventional trim circuits such as [14] and [16] use a switch in series with each tuning transistor. The leakage current of such switches could be in the order of a few pAs. Since this leakage current is comparable to the bias currents of the proposed low power voltage reference generator, such trimming circuits cannot be used here. Moreover, the use of additional transistors as switches also increases the occupied area, in addition to imposing additional leakage diodes on the output voltage reference. Depending on the trim code, these leakage diodes change and subsequently effect the compensation conditions. The solution presented here is to remove additional switch transistors and use enough negative value for the MOSFET overdrive voltage to reduce the subthreshold current to the required level in the off-state. This functionality is achieved by using pMOS devices with drain terminals connected to the ground, as shown in Fig. 1. If the gate terminal of the trimming transistor is connected to the ground, the trimming transistor acts similar to  $M_5$  and can be considered parallel with this device, allowing the tuning of  $M_5$  effective aspect ratio. However, when the gate terminal of each trimming transistor is connected to  $V_{DD}$ , the negative source-gate voltage produces a low enough leakage current which can be neglected compared with other branches' bias current and thus considered an open circuit. Leakage diodes  $M_{5,0}$  to  $M_{5,4}$  are incorporated into  $DD_{5,W5}$  on the output node shown in Fig. 1, which remains constant regardless of trim code changes. The TC, LS,  $V_{REF}$ , and power consumption are reported based on the best trim state for generating the minimum TC in the Monte Carlo iterations.

## 3. Design considerations

Some of the conditions for designing the voltage reference circuit have been discussed in previous sections. Here the required design considerations and constraints are summarized:

1. The output voltage of the first stage should be greater than  $V_{REF} + 2V_{SD}$ , where  $V_{SD}$  is about 200 mV.
2. The aspect ratio of  $M_7$  to  $M_6$  (K) should be considerably large, as assumed to obtain (20).



3. The aspect ratio of the second-stage transistors should be designed to achieve temperature compensation based on (12) as a first guess, and then refining the design by simulations.
4. The transistor dimensions should be large enough to reduce the threshold voltage variations related to the Short Channel Effect (SCE) and the Narrow Width Effect (NWE) [26]. All transistors' lengths in the second stage are  $2\text{ }\mu\text{m}$  except  $M_6$  and  $M_8$ . The  $M_3$  and  $M_8$  transistors are crucial in determining DIBL effects on  $LS_{pr}$ , so their channel length should be longer than other transistors. For the second constraint, the length of  $M_6$  was set to  $20\text{ }\mu\text{m}$  in the proposed design.
5. The bias currents are chosen in the pA range [27] for ultra-low power consumption.

Table 2 shows the transistor dimensions that have been chosen based on the above considerations. The channel length of  $M_3$  is chosen to be  $5\text{ }\mu\text{m}$ , and that of transistors  $M_1$  and  $M_2$  is chosen to be  $1\text{ }\mu\text{m}$ , as a compromise between area and SCE elimination. The total current at the minimum temperature ( $-20\text{ }^\circ\text{C}$ ) and supply voltage ( $0.8\text{ V}$ ) is set to be greater than  $1\text{ pA}$  as a compromise between accuracy and power consumption. As a result, by selecting a width of  $2\text{ }\mu\text{m}$  for transistors  $M_1$  and  $M_2$ , the required width of transistor  $M_3$ , which can supply this minimum current, is obtained.

Table 2- Transistor sizes of the proposed structure

Transistor	Type	size
$M_1$	Thick-oxide	$2\text{ }\mu\text{m}/1\text{ }\mu\text{m}$
$M_2$	Thick-oxide	$2\text{ }\mu\text{m}/1\text{ }\mu\text{m}$
$M_3$	Thin-oxide	$(50\text{ }\mu\text{m}/5\text{ }\mu\text{m})\times 8$
$M_4$	Thick-oxide	$20\text{ }\mu\text{m}/2\text{ }\mu\text{m}$
$M_5$	Thick-oxide	$(24.36\text{ }\mu\text{m}/2\text{ }\mu\text{m})\times 2$
$M_{5-0}$	Thick-oxide	$0.4\text{ }\mu\text{m}/2\text{ }\mu\text{m}$
$M_{5-1}$	Thick-oxide	$0.8\text{ }\mu\text{m}/2\text{ }\mu\text{m}$
$M_{5-2}$	Thick-oxide	$1.6\text{ }\mu\text{m}/2\text{ }\mu\text{m}$
$M_{5-3}$	Thick-oxide	$3.2\text{ }\mu\text{m}/2\text{ }\mu\text{m}$
$M_{5-4}$	Thick-oxide	$6.4\text{ }\mu\text{m}/2\text{ }\mu\text{m}$
$M_6$	Thick-oxide	$2\text{ }\mu\text{m}/20\text{ }\mu\text{m}$
$M_7$	Thick-oxide	$(30\text{ }\mu\text{m}/2\text{ }\mu\text{m})\times 2$
$M_8$	Thin-oxide	$(26\text{ }\mu\text{m}/6\text{ }\mu\text{m})\times 8$

To ensure that  $K$  is large enough, in the second stage, the aspect ratio of  $M_7$  to  $M_6$  is set to 300.  $M_4$  and  $M_6$  are selected to guarantee a source-drain voltage of  $M_7$  larger than  $200\text{ mV}$ . Simulations show that this voltage is  $230\text{ mV}$  after selecting the appropriate aspect ratio for temperature compensation.

To maintain a minimum supply voltage of  $0.8\text{ V}$ , the source-drain voltage of  $M_3$  is considered to be about  $165\text{ mV}$ . The appropriate aspect ratio of second-stage transistors for temperature compensation is designed based on equation (12). By placing the technology parameters, a value of  $1.55$  is obtained for this ratio. Fig. 5 shows the change in TC versus temperature when the width of transistor  $M_5$  is varied. The minimum TC is close to the predicted value.

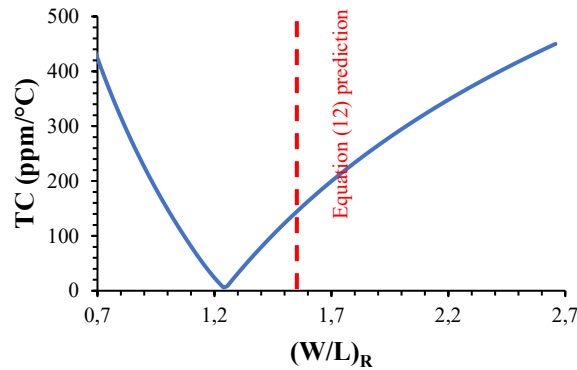


Fig. 5- TC simulation versus aspect ratio and equation (12) prediction for aspect ratio

#### 4. Simulation results

The voltage reference proposed in this paper has been designed and characterized by post-layout simulations in a 0.18  $\mu\text{m}$  CMOS technology. The layout of the proposed voltage reference is illustrated in Fig. 6, which reveals a silicon area occupancy of 10,208  $\mu\text{m}^2$ . The variations of  $V_{\text{REF}}$  with temperature (at nominal  $V_{\text{DD}}=0.8\text{V}$ ) and supply voltage (at 25°C) are reported in Fig. 7 and Fig. 8 for different process corners before and after trimming. Based on the simulations, the TC for temperatures ranging from -20 °C to 80 °C without using the trim circuit for TT, FF, SS, FS, and SF is 1.9 ppm/°C, 47.5 ppm/°C, 49.3 ppm/°C, 18.6 ppm/°C, and 11.2 ppm/°C, respectively, and by using the trim circuit for FF, SS, FS, and SF are enhanced to 1.2 ppm/°C, 5.8 ppm/°C, 4.5 ppm/°C, and 3.6 ppm/°C, respectively, which shows a significant improvement. The LS for supply voltages from 0.8 V to 2.4 V at TT, FF, SS, FS, and SF are 47.9 ppm/V, 67.8 ppm/V, 44.9 ppm/V, 42.9 ppm/V, 70.7 ppm/V, respectively, and by using trim circuit FF, SS, FS, and SF are changed to 68.9 ppm/V, 44.4 ppm/V, 42.8 ppm/V, and 71.2 ppm/V, respectively, and approximately constant before and after TC trimming. The power consumption versus supply voltage at temperatures of -20 °C and 80 °C is shown in Fig. 9. The minimum and maximum power consumptions at the typical corner are 0.9 pW and 1.41 nW, respectively. As expected, there is a higher power consumption in the FF corner and a lower power consumption in the SS corner than in the TT. In Fig. 10, the start-up time of the voltage reference is shown for different corners, as well as the minimum and maximum temperatures. A worst-case scenario occurs at -20 °C for the SS corner, where the output voltage settles at 1% of the final value in 1.4 s. In the best case, the output voltage settles at 1% of the final value in 1 ms at the FF corner and 80 °C.

Post-layout Monte Carlo analyses with 1000 runs are used to study process variations effects. The histograms of TC, LS,  $V_{\text{REF}}$ , and power before trim obtained by Monte Carlo are reported in Fig. 11 and after trim in Fig. 12. The TC is investigated in the temperature range of -20 °C to 80 °C at 0.8 V supply voltage. The LS is reported for a supply voltage change of 0.8 V to 2.4 V at 25°C. In addition, the output reference voltage and power consumption are evaluated at 0.8 V and 25 °C. Table 3 summarizes the results of the Monte Carlo analysis before and after the trimming. As seen from the results, the proposed trim circuit can significantly reduce the mean TC from 34.3 ppm/°C to 4.4 ppm/°C without having much effect on the other parameters.

Table 3- Summary of Monte Carlo analysis with 1000 runs without and using trim circuit

State		TC (ppm/°C)	LS (ppm/V)	$V_{\text{REF}}$ (mV)	Power (pW)
Without Trim	$\mu$	34.3	51.7	205.8	25.9
	$\sigma$	26.5	10.8	17.6	8.4
	$\sigma/\mu$	77.2%	20.9%	8.6%	32.4%
Using Trim	$\mu$	4.4	51.5	206	25.9
	$\sigma$	7	10	16.1	8.4
	$\sigma/\mu$	159.1%	19.4%	7.8%	32.4%

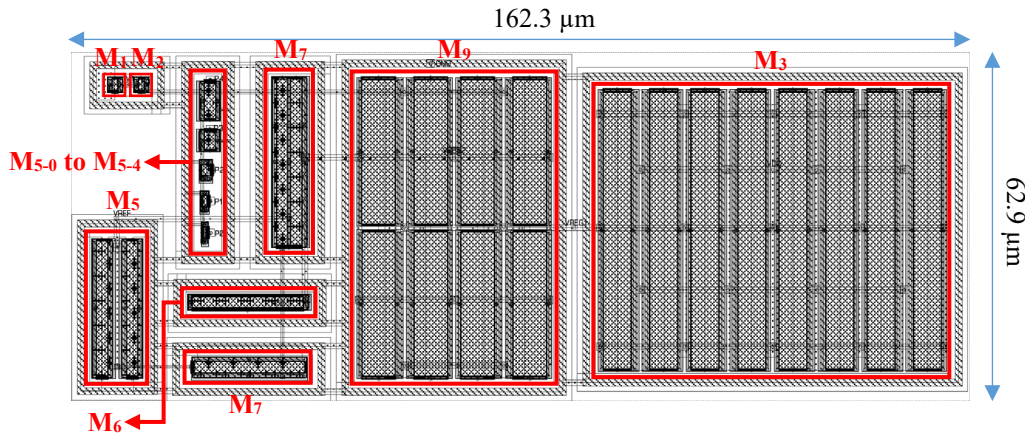


Fig. 6- Layout of the proposed voltage reference.

The proposed design does not use a decoupling capacitor. However, it is possible to use an external decoupling capacitor at the output to improve PSR and noise. The simulated PSR from 0.1 Hz to 10 MHz is reported in Fig. 13, with and without decoupling capacitors. The minimum PSR without a decoupling capacitor is -77.1 dB in 0.1 Hz. Due to the two long-channel LS regulators and the two-stage structure, a suitable reduction in PSR near dc frequencies is achieved. However, the PSR is increased up to -23.5 dB at 100 Hz. For high frequencies, the PSR is about -25.6 dB (-51.9 dB) without (with 10 pF) decoupling capacitor.

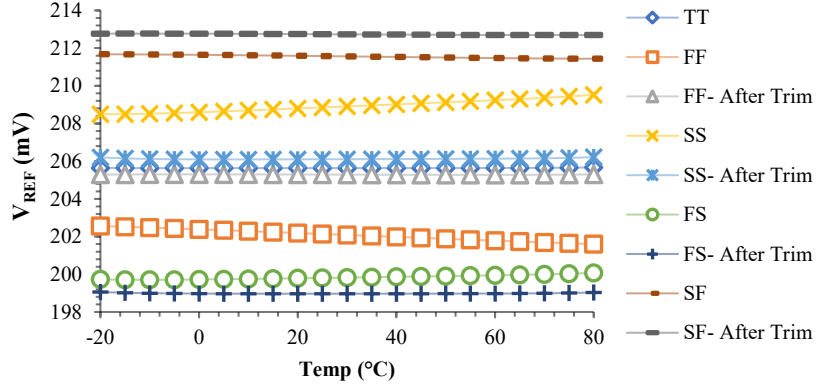


Fig. 7-  $V_{REF}$  versus temperature changes from -20 °C to 80 °C at different corners

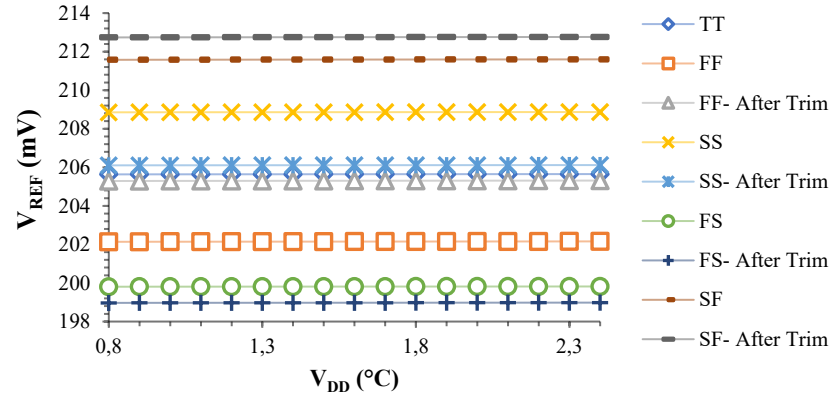


Fig. 8-  $V_{REF}$  versus supply voltage from 0.8 V to 2.4 V at different corners

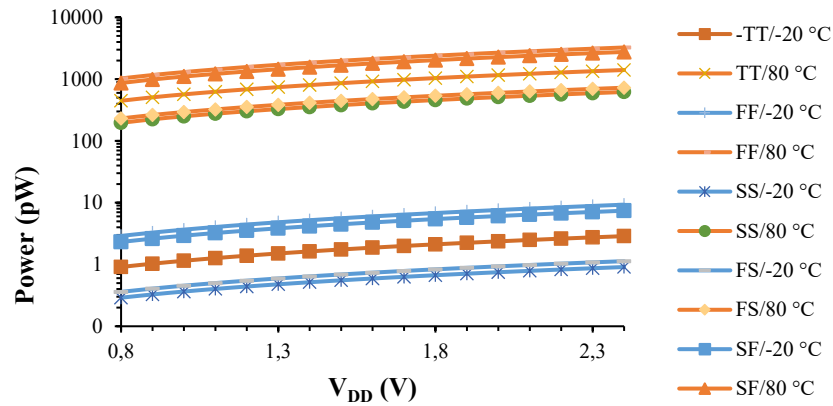


Fig. 9- Power consumption versus supply voltage changes from 0.8 V to 2.4 V at -20 °C and 80 °C and different corners

The output noise is also shown in Fig. 14. In the proposed circuit, the integrated output noise without decoupling capacitor and using 1 pF and 10 pF capacitors is 40  $\mu\text{V rms}$ , 39.6  $\mu\text{V rms}$ , and 29.3  $\mu\text{V rms}$ , respectively, for the 0.1 Hz to 10 Hz frequency range. In the same frequency band, [16] and [17] generate 55  $\mu\text{V rms}$  noise using a 10 pF decoupling capacitor and 24.4  $\mu\text{V rms}$  noise using 1.8 pF decoupling capacitor, respectively.

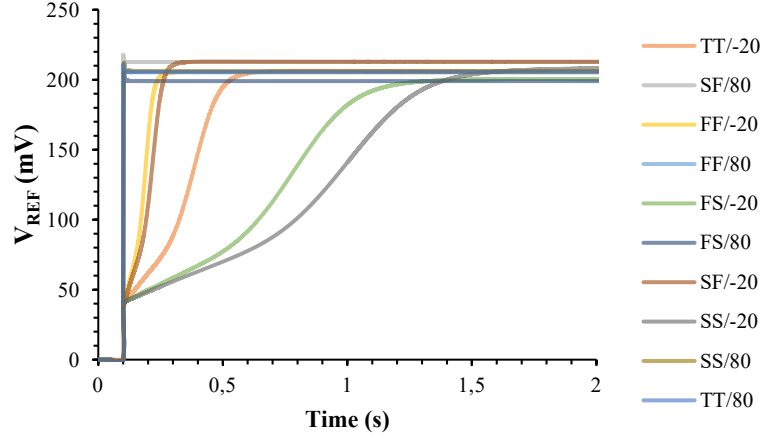


Fig. 10- Variations in the reference voltage for different corners when the supply voltage is turned on at 0.1 s

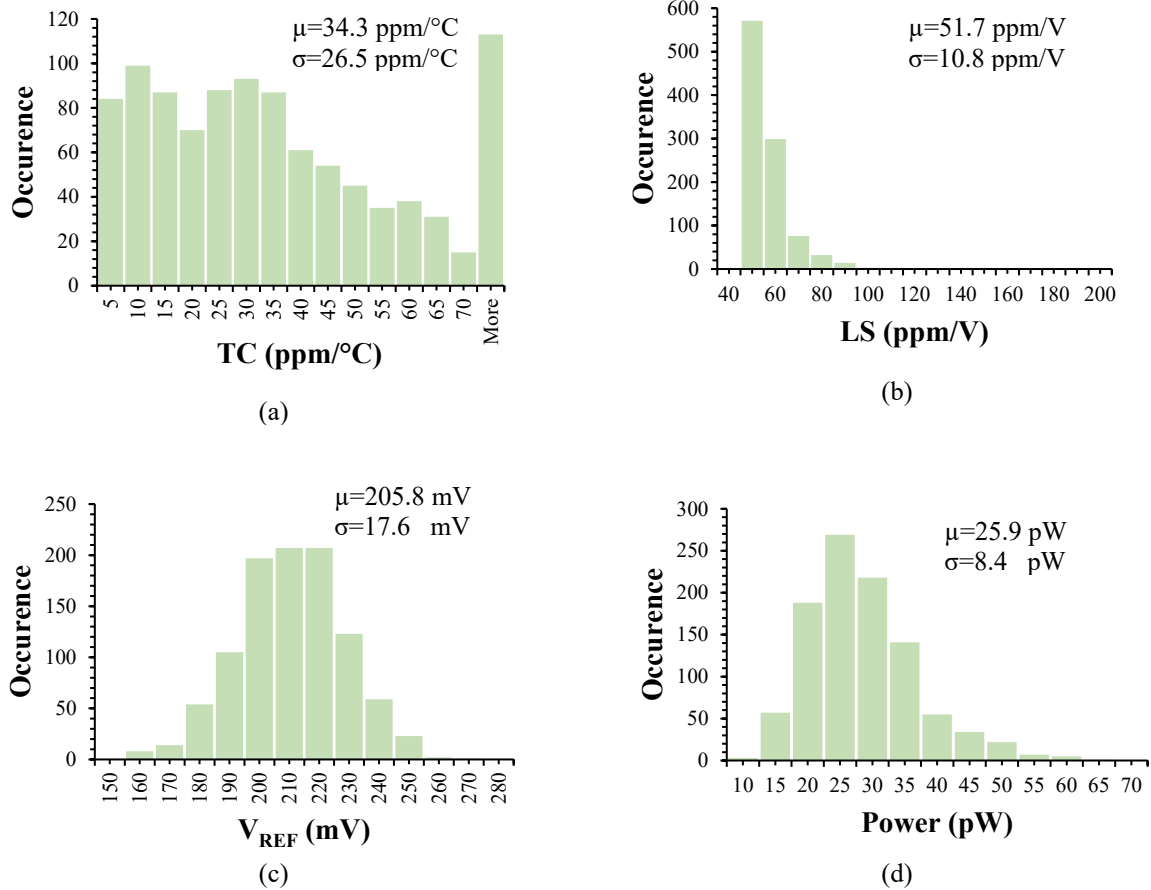


Fig. 11- The Monte Carlo analysis before trim on (a) TC, (b) LS, (c) reference voltage, (d) power consumption

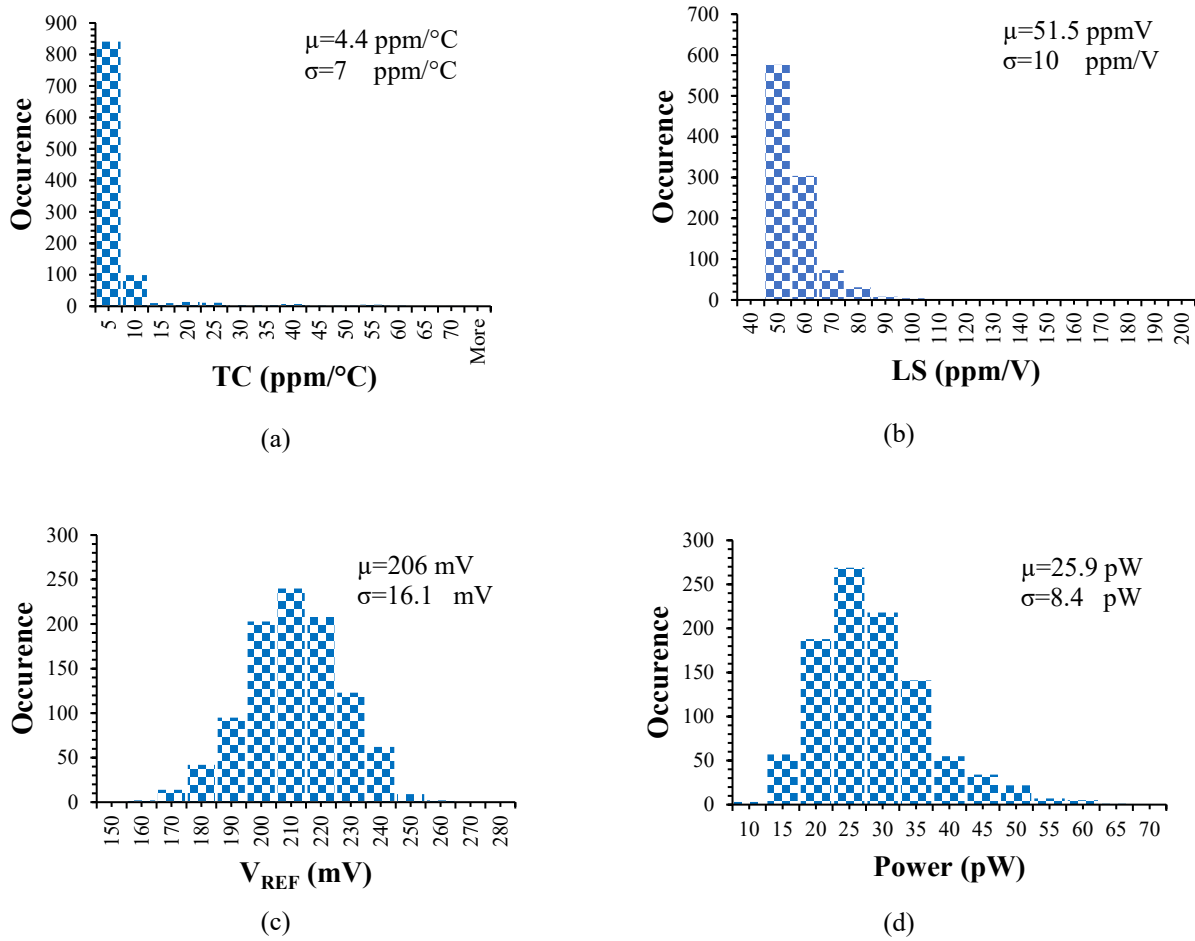


Fig. 12- The Monte Carlo analysis after trim on (a) TC, (b) LS, (c) reference voltage, (d) power consumption

Table 4- Comparison of the proposed voltage reference with other similar works

Design	This work*	[17]	[6]	[28]*	[9]*	[16]	[15]*	[14]	[8]	[18]	[25]	[10]
Tech ( $\mu\text{m}$ )	0.18	0.18	0.13	0.18	0.18	0.18	0.18	0.18	0.13	180	180	0.18
Min Supply (V)	0.8	1.4	0.3	0.12	4.4	0.6	0.4	0.4	0.5	0.25	0.6	1
LS (ppm/V)	51.5	3100	180000	2200	77	190	143.8	163	330/360 <sup>T</sup>	1600	1100	2300
Power (pW)	25.9 @25°C	35 @27°C	$4.12 \times 10^6$ @27°C	0.25 @27°C	$2.2 \times 10^8$ @NA	46/48 <sup>T</sup> @25°C	19.1 @25°C	1000 @25°C	2.2/29.5 <sup>T</sup> @25°C	5.4 @25°C	184/664 <sup>T</sup> @27°C	200000 @25°C
Temp range (°C)	-20-80	0-100	0-85	-40-120	-60-150	0-100	0-80	-40-125	-20-80	0-120	0-120	-40-140
TC (ppm/°C)	34.3 4.4 <sup>T</sup>	23 31 <sup>T</sup>	24.2	89.81	2.6	52 10.1 <sup>T</sup>	39.2 20.8 <sup>T</sup>	89.83	62 29 <sup>T</sup>	265	495 11.6 <sup>T</sup>	9.79
PSR (dB)												
@10 Hz <sup>‡</sup>	-41.2	-42.2	-28.7	-73.8	NA	-62.7	-90.9	-73	-50.5	-70	-45	-55.7
@10 kHz <sup>‡</sup>	-25.6	-42.6	-25.4	-42.6	NA	-50.2	-78	-49.3	-58.5	-83.5	-55	-39
V <sub>REF</sub> (mV)	205.8 206 <sup>T</sup>	1252 1251 <sup>T</sup>	241.8	65.7	2500	152.1* 147.9 <sup>T</sup>	119.2 NA	151	NA 176 <sup>T</sup>	91.4	378 457.1 <sup>T</sup>	345
Area ( $\mu\text{m}^2$ )	10208	2500	14000	70	NA	33200	2183	5000	9300	2200	1700	450000
FoM	2.19	0.04	$4 \times 10^{-9}$	5.18	NA	0.22	0.59	0.02	2.22	0.06	0.001	$7.2 \times 10^{-5}$
(°C <sup>3</sup> .V/mm <sup>2</sup> .W)	17.04 <sup>T</sup>	0.03 <sup>T</sup>				1.08 <sup>T</sup>	1.12 <sup>T</sup>	0.32 <sup>T</sup>			0.02 <sup>T</sup>	

\*Monte Carlo simulation

<sup>T</sup>After Trim

<sup>‡</sup> No decoupling capacitor

A figure of merit (FoM) is introduced in [25] for comparing voltage references, however, LS is neglected in this criterion. In this paper the following FoM is used for comparison:

$$FoM = \frac{(T_{max} - T_{min})^2}{TC \times LS \times Power} \times 10^{-23} \frac{^{\circ}C^3 \cdot V}{W} \quad (22)$$

Table 3 compares the proposed voltage reference with the state-of-art low power consumption and low TC designs. Owing to the BGR advantages, the TC of [9] is the lowest compared to the other works in Table 3. However, the design has higher power and supply voltage requirements than MOSFET voltage references, like the one presented in [28], which shows the minimum power consumption and supply voltage. In addition, [28] has the lowest power consumption, however, its TC and LS are not satisfactory compared to a BGR. The proposed voltage reference provides the best LS compared to the other works, which is 51.5 ppm/V after Monte Carlo analysis with 1000 runs. Furthermore, the average TC is 4.4 ppm/°C while consuming just 25.9 pW. Regarding the given FoM, the proposed voltage reference has the best performance.

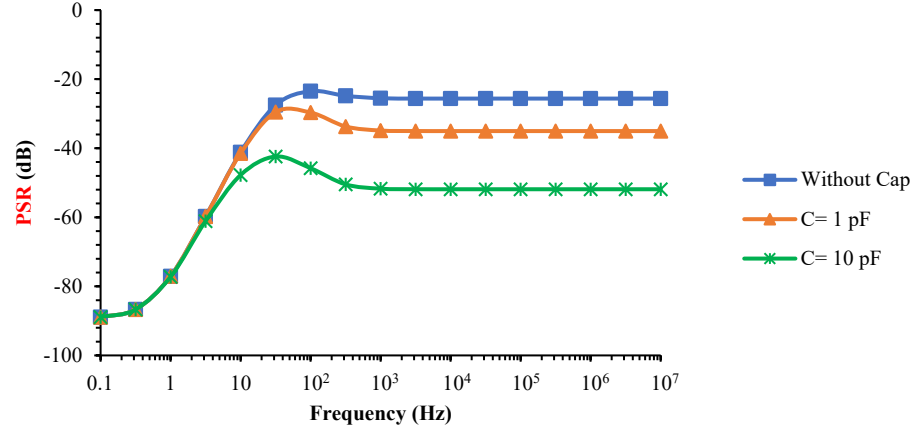


Fig. 13- PSR under  $V_{DD}=0.8$  V and 25 °C, with and without decoupling capacitors.

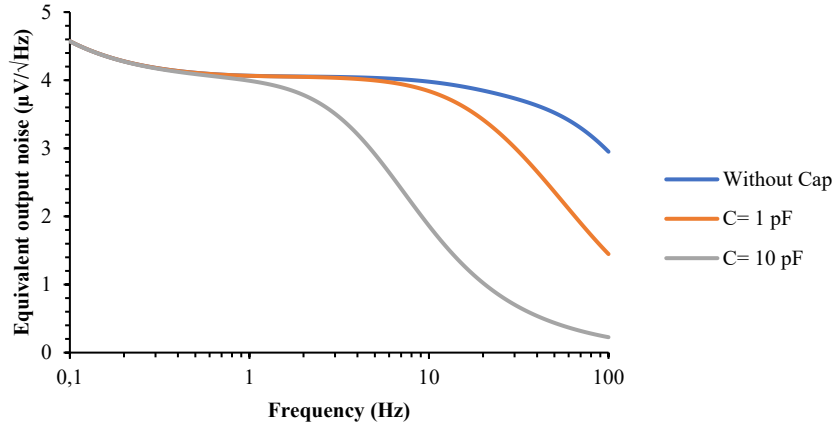


Fig. 14- Output noise from 0.1 Hz to 100 Hz for the proposed circuit with and without decoupling capacitors.

## 5. Conclusion

This paper presents an ultra-low power all pMOS voltage reference generator. While the TC and LS performance factors are competitive with BGRs, much lower power dissipation has been achieved. A TC of 34.3 ppm/°C was obtained without trimming through the TC compensation block designed for the two-stage reference generator. Using the proposed low leakage 5-bit trim circuit, the TC was improved down to 4.4 ppm/°C, and an LS of 51.5 ppm/V was obtained. Monte Carlo analyses with 1000 runs confirmed the effectiveness of the proposed structure over different processes and mismatch conditions. The power consumption of 25.9 pW under the supply potential of 0.8 V makes

the proposed voltage reference generator a good candidate for sensors and self-powered IoT devices which need to operate with low voltage and power constraints.

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