POLITECNICO DI TORINO
Repository ISTITUZIONALE

Relaxation Digital-to-Analog Converter with Radix-based Digital Correction

Original
Relaxation Digital-to-Analog Converter with Radix-based Digital Correction / Rubino, R., Musolino, F., Crovetti, P.S.. - STAMPA. - (2022), pp. 1402-1406. (2022 IEEE International Symposium on Circuits and Systems (ISCAS) Austin TX (USA) 27 May 2022 - 01 June 2022) [10.1109/ISCAS48785.2022.9937502].

Availability:
This version is available at: 11583/2978393 since: 2023-05-08T16:19:07Z

Publisher:
IEEE

Published
DOI:10.1109/ISCAS48785.2022.9937502

Terms of use:

This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

Publisher copyright
IEEE postprint/Author's Accepted Manuscript

©2022 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collecting works, for resale or lists, or reuse of any copyrighted component of this work in other works.

(Article begins on next page)

18 November 2026

Relaxation Digital-to-Analog Converter with Radix-based Digital Correction

Roberto Rubino[1], Francesco Musolino[1] and Paolo S. Crovetti[1]
[1]*Dipartimento di Elettronica e Telecomunicazioni (DET), Politecnico di Torino*, Torino, Italy
{roberto_rubino, francesco.musolino, paolo.crovetti}@polito.it

***Abstract*—A Relaxation Digital-to-Analog Converter (ReDACs) with a novel, all-digital, radix-based digital correction technique for clock-indifferent linear operation is presented in this paper. The ReDAC architecture proposed in this paper does not require dedicated circuit for frequency tuning, and achieves linearity by digitally pre-processing the DAC input code by a Radix-based Digital Correction (RBDC) algorithm. The effectiveness of the proposed RBDC approach is demonstrated by transistor level simulations on a 10-bit, 1.7MS/s ReDAC in 180nm CMOS. Thanks to the proposed RBDC, under a 16% deviation from the ideal clock period, the maximum INL of the ReDAC is improved from 79.4 to 1.01LSB, its maximum DNL is improved from 158.3 to 0.45LSB and its SNDR is increased from 22.2 (3.4 ENOB) to 58.5dB (9.4 ENOB), at the cost of an increased power consumption from 1.85μW to 9.15μW.**

***Index Terms*—Relaxation Digital to Analog Converter (ReDAC), Digital to Analog Converter (DAC), Radix-Based Digital Correction, Internet of Things.**

I. Introduction

The digital-driven developments of CMOS technology towards nanometer-scale nodes have dramatically improved performance, integration density, power and cost of digital architectures in the last years, but are making the integration of analog and mixed-signal interfaces more and more challenging and inefficient. In this context, translating analog and mixed-signal functions into digital, so that to implement them by true digital circuits taking full advantage of scaling and digital design, is more and more intensively being explored [1]–[16].

Following this trend, the Relaxation Digital to Analog Converter (ReDAC), which exploits the impulse response of a first-order RC network driven by a digital stream, has been recently proposed for digital-to-analog (D/A) conversion [17]–[20]. The ReDAC linear operation relies on a specific relation of the data clock period and of the time constant RC, which was enforced in previous work by either manual or automatic clock frequency tuning [17]–[20].

In this paper, a Radix-Based Digital Correction (RBDC) technique is proposed to achieve clock-indifferent linear ReDAC operation, without requiring voltage and/or digitally controlled oscillators [19], [20].

The paper has the following structure: in Section II, the ReDAC pinciple is briefly revised. The proposed radix-based correction is then described in Section III, and its hardware implementation is addressed in Section IV. In Section V, the circuit design and simulated performance are presented and discussed. Some concluding remarks are finally drawn in Section VI.

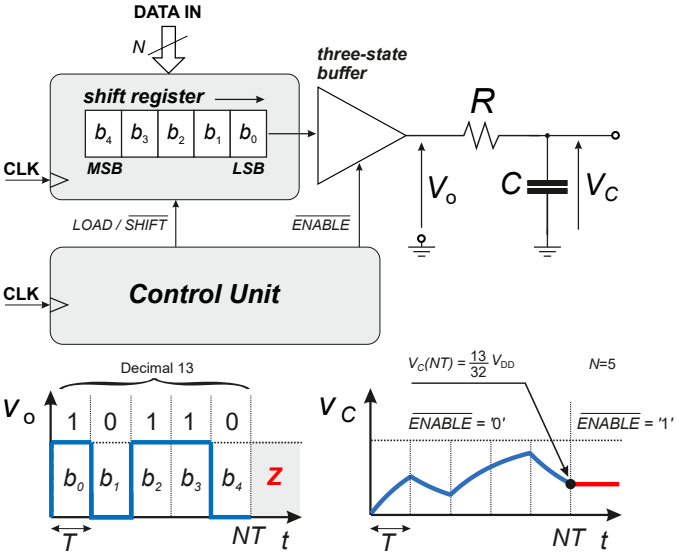


Fig. 1. Relaxation DAC operation principle.

II. Relaxation Digital-to-Analog Conversion

A. Relaxation DAC Operation Principle

A ReDAC [17]–[20] takes advantage of the exponential impulse response of a first order RC network driven by a digital stream for D/A conversion, as illustrated in Fig.1. When the RC network is driven by rectangular pulses corresponding to the bits $b_i, i = 0...N-1$ of the input code, applied LSB-first at a rate $1/T$, the capacitor voltage at the end of the N^{th} clock cycle can be expressed as [17]–[20]

$$v_{\text{C}}(NT) = V_{\text{DD}}\left(1 - e^{-\frac{T}{\tau}}\right) \sum_{i=0}^{N-1} b_i e^{-\frac{(N-i-1)T}{\tau}} \tag{1}$$

being $\tau = RC$ the time constant. If condition

$$e^{-\frac{T}{\tau}} = \frac{1}{2} \quad \Longrightarrow \quad T = T^* = \tau \log 2 \tag{2}$$

is met, the final capacitor voltage

$$v_{\text{C}}(NT) = \frac{V_{\text{DD}}}{2^N} \sum_{i=0}^{N-1} b_i 2^i. \tag{3}$$

is proportional to the digital input code as expected in a D/A converter. A ReDAC can be implemented in practice by a shift register driving a tree-state buffer, as shown in Fig. 1.

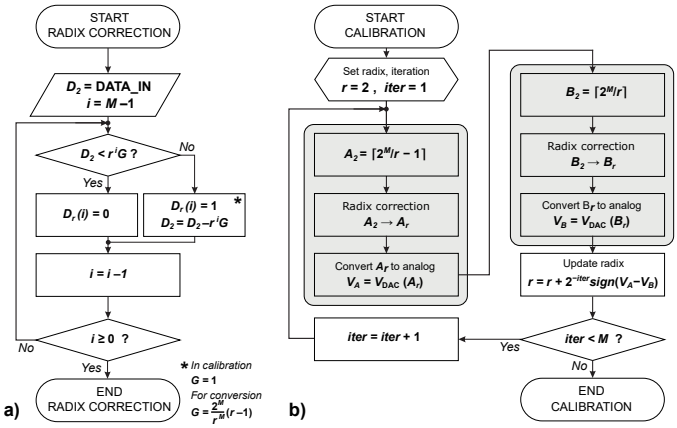


Fig. 2. Digital Calibration (a) and Radix-Based Digital Correction (b).

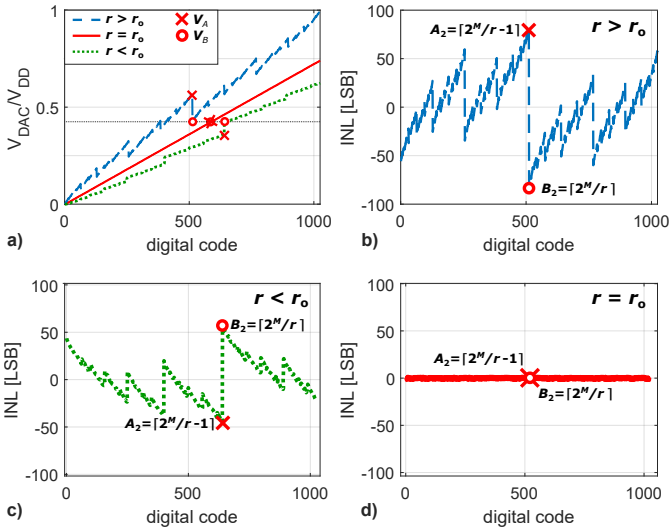


Fig. 3. ReDAC static characteristics under different r (a) and ReDAC INL for the case of $r > r_o$ (b), $r < r_o$ (c) and $r = r_o$ (d).

B. Clock Period Errors and ReDAC Linearity

When condition (2) is not met, (1) becomes

$$v_C(NT) = \frac{V_{DD}}{2^N} G \sum_{i=0}^{N-1} b_i r^i \tag{4}$$

where $G = \frac{2^N}{r^N}(r-1)$, and the ReDAC output voltage is therefore proportional to the radix-r converted input code, with $r = e^{\frac{T}{\tau}} \neq 2$. This is analogous to what happens in two-capacitors DACs with mismatched capacitors [21].

Whenever the input code is expressed in the usual radix-2 notation and condition (2) is not met, the radix-r D/A conversion inherently performed by the ReDAC results in a nonlinearity error [18]–[20], which is maximum between codes $2^{N-1}-1$ and 2^{N-1} and proportional to the clock period deviation $\Delta T = T - T^*$ from (2).

Aiming at suppressing such nonlinearity, ReDAC self-calibration techniques [19], [20] have been proposed to tune the clock period so that to enforce (2). Those techniques, however, require either controlled oscillators or clock dividers [20]. To avoid such an hardware overhead, an alternative ReDAC calibration technique is proposed in this paper.

The idea is to achieve linear ReDAC operation at fixed clock frequency by translating the ReDAC input code from radix-2 into in radix-r by a digital radix correction algorithm analogous to that proposed in [21] to compensate capacitor mismatch in two-capacitors DACs [22]–[24], and to estimate the optimal radix r_o

$$e^{-\frac{T}{\tau}} = \frac{1}{r} \quad \Longrightarrow \quad r = r_o = e^{\frac{T}{T^*}\log 2} \tag{5}$$

for linear operation by foreground digital self-calibration. Unlike in [21], where rather complex hardware is used for radix estimation, a new approach similar to that adopted in [19], [20] for ReDAC calibration, is proposed in this paper to estimate the optimal radix r_o at minimum hardware overhead.

III. Radix-Based ReDAC Correction

A. Radix-based Correction

Based on (4), ReDAC linearity can be achieved even if the clock period T does not meet (2), provided that the input code is converted from radix-2 into radix-r in accordance to (5).

For a given radix r, the conversion of a generic radix-2 code D_2 into the radix-r code D_r on M-bits can be performed by the serial, SAR-like, algorithm derived from [21] and illustrated in Fig.2a. The D_2 register is initialized with the radix-2 input code to be translated, while the index i is set to $i = M-1$. At each step, D_2 is compared with $r^i G$ and the result of the comparison gives the i^{th} bit of D_r. The D_2 register is then updated to $D_2 - r^i G$ if $D_2 < r^i G$, or kept constant otherwise. Finally, the index i is decremented for a new iteration, until all the bits of D_r are resolved, and D_r coincides with the radix-r representation of D_2.

B. Radix-based Calibration

To implement RBDC, the radix $r = r_o$ in (5) needs to be estimated in advance. While a bulky circuit [25] based on a $\Delta\Sigma$ ADC is used in [21] to pre-compute the radix of a mismatched two-capacitors DAC, a simpler approach based on the ReDAC self-calibration strategy presented in [19], [20], is proposed in this paper to estimate r_o in a ReDAC.

Generalizing the results in [19], [20], for $r \neq r_o$ the ReDAC nonlinearity error is maximum in magnitude (and opposite in sign) at input codes $A_2 = \lceil 2^N/r - 1 \rceil$ and $B_2 = \lceil 2^N/r \rceil$, as in Fig.3. Moreover, the difference between the analog outputs $V_A = V_{DAC}(A_2)$ and $V_B = V_{DAC}(B_2)$, depends monotonically on r and is positive (negative) for $r > r_o$ ($r < r_o$). These properties are exploited in this paper to estimate the unknown ReDAC radix r_o by a self-calibration strategy similar to that presented in [19], [20] to tune the ReDAC clock period. Instead of the clock period, the radix r needed in the radix correction algorithm of Sect.III-A is tuned

based on the sign of $V_{\rm A} - V_{\rm B}$, aiming to enforce condition $V_{\rm A} = V_{\rm B}$, which is sufficient to keep the ReDAC maximum INL below 0.5 LSB [20].

The calibration algorithm is illustrated in Fig.2b for an M-bit converter. At the beginning, $iter = 1$, the radix estimate r is initialized to $r = 2$, the codes A_2 and B_2 are expressed in radix-r by the radix correction algorithm in Fig.2a, and then converted by the ReDAC into the output voltages $V_{\rm A}$ and $V_{\rm B}$. Based on the sign of $V_{\rm A} - V_{\rm B}$, the MSB of the radix estimate r is updated. The same procedure is repeated M times, so that at the end of each iteration $iter$, $r = r + 2^{-iter}\text{sign}(V_A - V_B)$ until $V_{\rm A} = V_{\rm B}$ within one LSB.

IV. Circuit Implementation

The proposed Radix Correction algorithm has been adopted in the architecture in Fig.4a, which is composed by a ReDAC, a Radix-Correction block implementing the procedure in Fig.2a and a calibration block implementing the procedure in Fig.2b to estimate the radix $r_{\rm o}$.

A. Digital Architecture

The Radix Correction block includes two M-bit registers: an accumulator D_2 storing the residues and a serial-input-parallel-output (SIPO) register D_r retrieving the result of the conversion, a subtractor and a register file storing the powers r^iG needed for the radix correction. The execution flow is managed by a control unit (finite state machine) according to the flowchart in Fig.2a, as shown in the timing diagram of Fig.5 and described below.

At the beginning of radix correction, D_2 loads the input code to be radix-corrected and the internal counter i is set to $i = M - 1$. The content of D_2 and the value r^iG from the register file are applied to the inputs of the subtractor. According to the algorithm in Fig.2a, at each clock cycle, the MSB of the difference $DIFF = D_2 - r^iG$, which corresponds to its sign in two's complement, is serially-input to D_r, while D_2 is updated to $DIFF$ if $DIFF \geq 0$, and kept constant if $DIFF < 0$. The counter i is decremented and a new iteration starts until all the bits of D_r have been resolved ($i = 0$), and D_r is sampled on ReDAC_IN. While a code is being converted by the ReDAC, the next code is processed by the Radix Correction block, providing continuous ReDAC operation in a pipelined fashion, as shown in Fig.5.

B. Digital Calibration Operation

The calibration block in Fig.4, is intended to estimate the radix r based on the calibration procedure described in Sect.II-B and in Fig.2b, and is not active in normal operation. In details, the block is in charge to drive the ReDAC through the M steps of the calibration so that to convert the codes $A_2 = \lceil 2^M/r - 1 \rceil$ and $B_2 = \lceil 2^M/r \rceil$ at which the maximum positive (negative) nonlinearity error can be observed, and to update the radix estimate r based on the sign of $V_A - V_B$, which can be effectively detected by the same procedure described in [20] for the ReDAC period calibration. The same calibration block is also in charge to update the content of

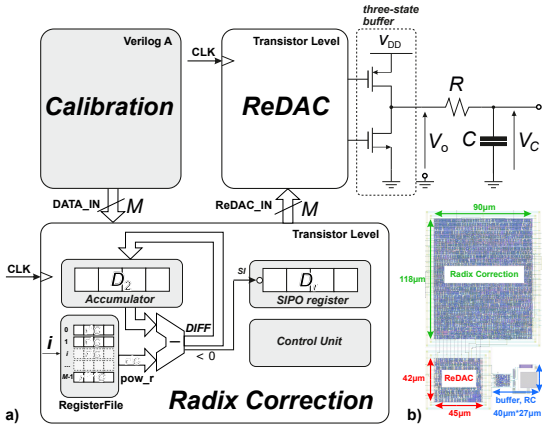


Fig. 4. ReDAC with RDBC architecture (a) and its layout in 180nm (b)

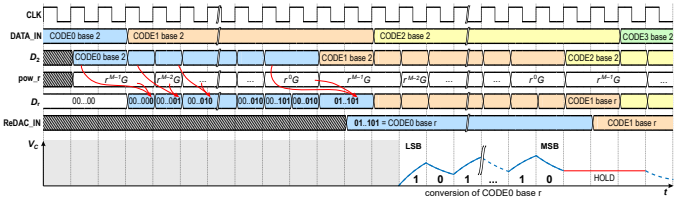


Fig. 5. Pipelined operation of Radix Correction and ReDAC conversion.

the register file with the new values r^iG at each step of the calibration procedure, as required for the operation of the radix correction block.

V. Validation

A. Circuit Design

The radix-based digital correction algorithm proposed in this paper has been validated by transistor level simulations on a 10-bit ReDAC in 180nm CMOS. The ReDAC passive RC network is made up by an $R = 140\text{k}\Omega$ hi-res poly resistor and by a $C = 450\text{fF}$ Metal-insulator-Metal (MiM) capacitor (time constant $\tau = RC = 63\text{ns}$), designed following the procedure described in [18], and it is driven by a full-customly designed three-state buffer operated at 0.7V supply voltage. The ReDAC digital core and the radix correction block in Fig.4a, both operating at 0.55V, have been automatically synthesized and implemented in standard cells from a behavioral VHDL description, then simulated at transistor level.

The whole circuit, whose layout is shown in Fig.4b, occupies a silicon area of $13,590\mu\text{m}^2$, including passives and output buffer ($1,080\mu\text{m}^2$), ReDAC core ($1,890\mu\text{m}^2$) and radix correction module ($10,620\mu\text{m}^2$).

The self-calibration procedure described in Sec.IV-B, which can be conveniently managed in practice by a microprocessor/DSP, has been implemented by a Verilog-A behavioral block. The latter includes the analog comparison network needed to detect the sign of the difference $V_A - V_B$, which could be implemented in practice as described in [20] by voltage-to-time and time-to-digital conversion.

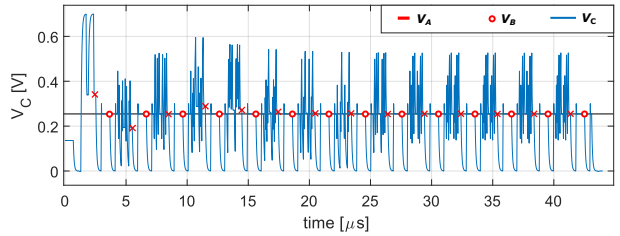


Fig. 6. Calibration waveform of the capacitor voltage.

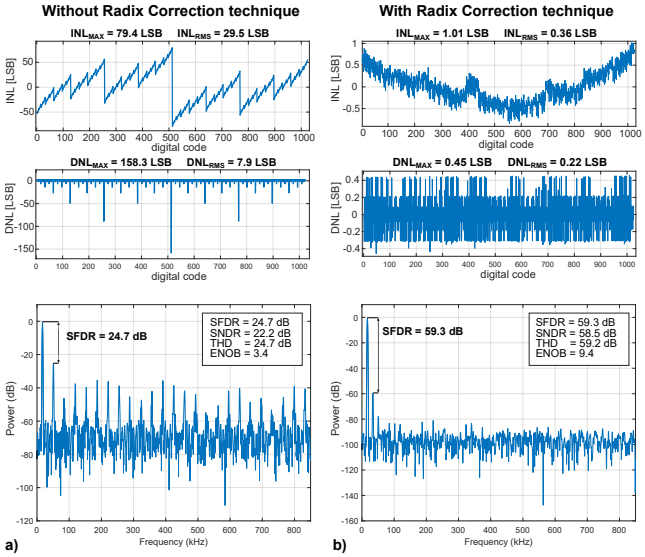


Fig. 7. Static and dynamic performance without Radix Correction (a) and after radix correction (b).

B. Digital correction performance

The 180nm CMOS ReDAC has been simulated at transistor level with and without the radix-based digital correction and self-calibration technique proposed in this paper, introducing an intentional 16% deviation of the clock period T with respect to the nominal value $T^* = 43$ns required, based on (2), for linear conversion of an input code expressed in radix-2. Such a large deviation conservatively accounts for the process spreads in R, C and in the ReDAC clock frequency generated by a low-power, low-cost relaxation oscillator. The waveform of the capacitor voltage during the calibration is shown in Fig.6 and reveals the effectiveness of the proposed dichotomic radix search approach in enforcing the equality of the ReDAC output voltage at codes $A_2 = \lceil 2^M/r - 1 \rceil$ and $B_2 = \lceil 2^M/r \rceil$.

The static and dynamic performance of the ReDAC without (with) radix-correction are shown in Fig.7a (Fig.7b), respectively. It can be observed that the radix-based correction results in improved maximum (rms) INL from 79.4(29.5)LSB to 1.01(0.36)LSB, and in maximum (rms) DNL from 158.3(7.9) LSB to 0.45(0.22)LSB.

The spectra of the ReDAC output under a full-swing sine wave input at 17kHz frequency, which corresponds to 1% of the sample rate, are also shown in Fig.7. Based on such spectra, the radix-corrected ReDAC achieves 59.3dB SFDR, 58.5dB SNDR, 59.2dB THD, corresponding to 9.4 effective bits (ENOB), more than 6 effective bits better than the non radix-corrected ReDAC, which shows 24.7dB SFDR, 22.2dB SNDR, 24.7dB THD and 3.4 ENOB. The average power consumption is 0.94μW for the output buffer driving the RC network, 0.91μW for the ReDAC core and 7.3μW for the radix correction network, thus resulting in 5.38pJ per conversion at 1.7MS/s sample rate, and in a 9.21 fJ/conv-step Figure of Merit (FOM) for the proposed ReDAC with radix correction.

TABLE I
REDAC PERFORMANCE COMPARISON

	Units	[17]	[18]	[19]	[20]	This Work
Valid.		Meas.	Sim.	Sim.	Meas.	Sim.
Techn.	nm	FPGA	40	40	FPGA	180
Supply	V	3.3	0.6	0.6	3.3	0.7/0.55
Power	μW	N/A	0.44	1.46	N/A	9.15
R	kΩ	100	288	128	4.7	140
C	pF	2,200	1	0.45	2,200	0.45
Area	μm^2	N/A	910	677	N/A	13590
Res.	bit	10	10	12	11	10
Samp. Rate	kS/S	0.3	400	2,000	10.5	1,450
$\mathrm{INL_{max}}$	LSB	2.4	0.33	0.72	1.53	1.01
$\mathrm{INL_{rms}}$	LSB	0.9	0.10	0.34	0.415	0.36
$\mathrm{DNL_{max}}$	LSB	3.3	0.2	1.27	1.0	0.45
$\mathrm{DNL_{rms}}$	LSB	0.62	0.01	0.07	0.319	0.22
SNDR	dB	43.27	61.0	58.3	63.3	58.5
SFDR	dB	51.36	76.8	62.4	71.4	59.3
THD	dB	47.52	66.7	62.2	67.9	59.2
ENOB	bit	7.13	9.9	9.4	10.2	9.4
FOM	fJ/(c.s.)	N/A	1.1	1.08	N/A	9.21
Calibr.		Manual	Manual	Auto[a]	Auto[b]	Auto[c]

[a]VCO-based clock tuning, [b]Digital clock divider clock tuning, [c]Algorithmic search of radix r.

In Tab.I, the performance of the ReDAC based on the proposed radix correction technique is compared with ReDACs featuring clock-tuning based self-calibration [19], [20] and also with optimal manual clock tuning [18]. It can be observed that it effectively achieves full ReDAC linearity without clock frequency tuning. The proposed technique results however in a power overhead of 7.3μW (7.8X the ReDAC analog power) related to the real-time radix correction block, which could be however reduced in finer technologies. Scaling the design to 40nm, for example, the active power of the radix correction block is expected to scale down by 20X, thus becoming less than the analog power.

VI. CONCLUSIONS

A radix-based digital correction technique for clock-indifferent ReDAC linear operation has been presented, and its effectiveness has been validated by transistor-level simulations on a 10-bit, 1.7MS/s ReDAC in 180nm CMOS technology, which demonstrates fully linear operation and 9.4 ENOB under 16% clock period deviation, with a power overhead of 7.3μW. Unlike previous ReDAC calibration techniques, the new approach does not require clock tuning and makes it possible to digitally estimate the unknown radix at moderate hardware overhead.

REFERENCES

[1] P. Toledo, R. Rubino, F. Musolino and P. Crovetti, "Re-Thinking Analog Integrated Circuits in Digital Terms: A New Design Concept for the IoT Era," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 3, pp. 816-822, March 2021.

[2] P. S. Crovetti, F. Musolino, O. Aiello, P. Toledo and R. Rubino, "Breaking the boundaries between analogue and digital," in Electr. Lett., vol. 55, no. 12, pp. 672-673, 13 6 2019.

[3] M. Alioto (Ed.), Enabling the Internet of Things: From Integrated Circuits to Integrated Systems, Springer, 2017.

[4] S. Oh, D. Blaauw and D. Sylvester, "The Internet of Tiny Things: Recent Advances of Millimeter-Scale Computing," in IEEE Design & Test, vol. 36, no. 2, pp. 65-72, April 2019.

[5] P. R. Kinget, "Scaling analog circuits into deep nanoscale CMOS: Obstacles and ways to overcome them," 2015 IEEE Custom Integrated Circuits Conference (CICC), 2015, pp. 1-8

[6] V. Unnikrishnan and M. Vesterbacka, "Mixed-Signal Design Using Digital CAD," 2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2016, pp. 6-11.

[7] P. S. Crovetti, "All-Digital High Resolution D/A Conversion by Dyadic Digital Pulse Modulation," in IEEE Tran. on Circ. and Syst.I: Reg. Papers, vol. 64, no. 3, pp. 573-584, Mar. 2017.

[8] O. Aiello, P. Crovetti and M. Alioto, "Standard Cell-Based Ultra-Compact DACs in 40-nm CMOS," in IEEE Access, vol. 7, pp. 126479-126488, 2019.

[9] R. B. Staszewski et al., "All-digital PLL and transmitter for mobile phones," in IEEE Journal of Solid-State Circuits, vol. 40, no. 12, pp. 2469-2482, Dec. 2005.

[10] Palumbo, G.; Scotti, G. A "Novel Standard-Cell-Based Implementation of the Digital OTA Suitable for Automatic Place and Route." J. Low Power Electron. Appl. 2021, 11, 42.

[11] V. Unnikrishnan, S. R. Pathapati and M. Vesterbacka, "A fully synthesized all-digital VCO-based analog-to-digital converter," 2015 Nordic Circuits and Systems Conference (NORCAS): NORCHIP International Symposium on System-on-Chip (SoC), 2015, pp. 1-4.

[12] P. Chen, X. Meng, J. Yin, P. -I. Mak, R. P. Martins and R. B. Staszewski, "A 529-μW Fractional-N All-Digital PLL Using TDC Gain Auto-Calibration and an Inverse-Class-F DCO in 65-nm CMOS," in IEEE Transactions on Circuits and Systems I: Regular Papers.

[13] S. Kalani, A. Bertolini, A. Richelli and P. R. Kinget, "A 0.2V 492nW VCO-based OTA with 60kHz UGB and 207 μV rms noise," 2017 IEEE International Symposium on Circuits and Systems (ISCAS), 2017, pp. 1-4.

[14] P. Toledo, P. Crovetti, O. Aiello and M. Alioto, "Design of Digital OTAs With Operation Down to 0.3V and nW Power for Direct Harvesting," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 9, pp. 3693-3706, Sept. 2021.

[15] A. Fahmy, J. Liu, P. Terdal, R. Madler, R. Bashirullah and N. Maghari, "A synthesizable time-based LDO using digital standard cells and analog pass transistor," ESSCIRC 2017 - 43rd IEEE European Solid State Circ. Conf., Leuven, 2017, pp. 271-274.

[16] J. Liu, B. Park, M. Guzman, A. Fahmy, T. Kim and N. Maghari, "A Fully Synthesized 77-dB SFDR Reprogrammable SRMC Filter Using Digital Standard Cells," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 26, no. 6, pp. 1126-1138, June 2018.

[17] P. S. Crovetti, R. Rubino and F. Musolino, "Relaxation digital-to-analogue converter," in Electr. Lett., vol.55, no.12, pp. 685-688, 2019.

[18] R. Rubino, P.S.Crovetti, O.Aiello, "Design of Relaxation Digital-to-Analog Converters for Internet of Things Applications in 40nm CMOS," in proc. 2019 IEEE Asia Pacific Conf. on Circ. and Syst. (APCCAS 2019), Bangkok, 2019.

[19] P. S. Crovetti, R. Rubino and F. Musolino, "Relaxation Digital-to-Analog Converter with Foreground Digital Self-Calibration," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020, pp. 1-5.

[20] R. Rubino, P. S. Crovetti and F. Musolino, "FPGA-Based Relaxation D/A Converters With Parasitics-Induced Error Suppression and Digital Self-Calibration," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 6, pp. 2494-2507, June 2021.

[21] J. Cao and G. C. Temes, "Radix-based digital correction technique for two-capacitor DACs," Proceedings of 2010 IEEE International Symposium on Circuits and Systems, 2010, pp. 565-568

[22] P. Rombouts, L. Weyten, J. Raman and S. Audenaert, "Capacitor mismatch compensation for the quasi-passive-switched-capacitor DAC," in IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 45, no. 1, pp. 68-71, Jan. 1998.

[23] J. Steensgaard, U. -. Moon and G. C. Temes, "Mismatch-shaping serial digital-to-analog converter," 1999 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 5-8 vol.2 1999.

[24] P. Chen and T. Liu, "Switching Schemes for Reducing Capacitor Mismatch Sensitivity of Quasi-Passive Cyclic DAC," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 56, no. 1, pp. 26-30, Jan. 2009.

[25] Yuming Cao and G. C. Temes, "High-accuracy circuits for on-chip capacitance ratio testing or sensor readout," in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 41, no. 9, pp. 637-639, Sept. 1994.