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Analysis of Doherty Power Amplifier Matching Assisted by Physics-Based Device Modelling

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Abstract: The Doherty Power Amplifier represents one of the most promising solutions for the design of high-efficiency power stages. In the widely adopted ABC scheme, the Doherty Amplifier design critically depends on the accuracy of the device model in different operating conditions, ranging from class AB to class C. For the class C case, library models are often inaccurate, while experimental characterization is difficult since it must be carried out in large signal conditions and with varying gate bias. In this paper, we propose an alternative approach, based on physics-based Technological CAD (TCAD) simulations of the complete Doherty amplifier along with the analysis of its individual MAIN (class AB) and AUXILIARY (class C) stages. TCAD simulations seamlessly provide an accurate modelling of the device behavior in all operation classes, including the device turn-on and the nonlinear capacitances, and easily account for the cross-loading effects of the MAIN and AUXILIARY devices through the output network and the effect of the device feedback (gate-drain) capacitance on the input matching. Analyzing a GaAs Doherty stage at 12 GHz, we show that the input phase of the auxiliary stage can be exploited for the Doherty power amplifier optimization in terms of gain, linearity and efficiency, showing a 9 dB gain with less than 1 dB gain variation from back-off to peak power with a power-added efficiency exceeding 45% over a Doherty region extending to a more than 6 dB output power back-off.

Keywords: TCAD nonlinear analysis; Doherty amplifier; microwave power amplifiers; MMIC circuits

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1. Introduction

The design of high-efficiency RF/microwave power amplifiers operating with signals characterized by significant envelope variations, i.e., with a high Peak-to-Average Power Ratio (PAPR), is mandatory for the successful design of modern telecom front-ends. Conventional Power Amplifiers (PAs), obtained by parallel combining several individual stages (active devices), are characterized by an efficiency that rapidly degrades when decreasing the average output power; hence, they are not suited to amplifying high PAPR signals where the average power can be 6–9 dB lower than the peak power.

Among the alternative PA schemes [1] proposed to enhance efficiency in back-off, the Doherty Power Amplifier (DPA) represents one of the most promising solutions [2,3]. The Doherty amplifier combines the power from two independent PAs, the so-called peaking (or auxiliary) and the carrier (or main). Each amplifier exploits a corresponding active device (usually an FET), hereafter denoted as the MAIN and AUX devices, for the main and auxiliary amplifiers, respectively. Rather than being isolated and operated in identical conditions, as in parallel stages, the two amplifiers are combined with a proper output network to enhance the overall efficiency over a wide power range. At lower power (back-off), only the MAIN device is active and the efficiency increases with input power, reaching its maximum value at a prescribed level of Output Power Back-Off (OBO). Above this limit, the AUX amplifier turns on, acting as an active load for the MAIN amplifier. Ideally,

the efficiency should remain high in the whole range of power from the selected OBO level up to peak power. In the symmetric case, used in this work, the MAIN and AUX are identical devices, and the high-efficiency region extends to 6 dB OBO [4]. When the goal of high efficiency must meet the further requirements in terms of high gain, linearity and wideband operation, practical realization of the Doherty amplifier exploits the so-called ABC scheme [5], where the MAIN device is biased in Class AB and the AUX in class C.

Although the Doherty scheme has attracted much attention in the most advanced RF and power technologies, including Silicon [6–9], GaAs [10,11] and GaN [12–14], the DPA design still presents significant challenges due to the difficult identification of the correct input and output matching conditions. In fact, the AUX and MAIN operating conditions continuously change with the input power drive, making it difficult to match both the stages over the whole output power range. Most studies concentrate on the output port [15], where the interplay of the matching networks and the combining network affect the correct modulation of the MAIN amplifier, calling for remedies based, e.g., on offset lines [16,17], load modulation combiners [18,19], post-matching impedance transformation [20], low-loss output networks [9], adaptive bias and device stacking [8] and outphasing [14]. Input matching is critical since it governs the DPA efficiency, gain flatness and linearity through the correct AUX amplifier turn-on. A slow AUX turn-on often leads to a significant gain drop in both back-off and the Doherty region [6,18,21]. In conclusion, the DPA design is affected by several competing constrains calling for advanced optimization methods, most recently including neural networks [22–24] and digital control [25,26].

DPA optimization at the circuit level is difficult because library large-signal models from deep class C to class AB are often inaccurate, while experimental characterization is demanding since it must be carried out under large signal conditions and varying gate bias, e.g., exploiting extensive multi-bias load- and source-pull [20].

In this paper, we propose an alternative approach, based on physics-based TCAD simulations of the complete Doherty amplifier along with an analysis of its individual MAIN and AUX stages. TCAD simulations circumvent the lack of accurate large-signal compact models and seamlessly include both resistive and reactive device behaviour as a function of the operating class (bias), starting from their microscopic origin, i.e., from the semiconductor charges and electron transport parameters. TCAD analysis of the individual MAIN and AUX amplifiers may be exploited to extract accurate circuit models, e.g., though X-parameters [27,28] or trained neural networks. On the other hand, TCAD simulations of the whole Doherty circuit provide guidelines for the input/output matching and offset lines design.

Unfortunately, conventional TCAD simulators are usually limited to DC and small-signal analyses, and not suited for power amplifiers, where the active devices are operated in large-signal nonlinear conditions. Therefore, in this work, we exploit our in-house mixed-mode drift-diffusion TCAD simulator [29], implementing the Harmonic Balance algorithm, which allows for the large-signal simulation of microwave devices in a periodic nonlinear regime. We address the analysis and preliminary design of a Doherty power amplifier developed in GaAs technology operating at 12 GHz. Various DPA schemes, differing only in terms of input matching (i.e., keeping the output matching unchanged), are simulated and compared. Simulations show that the AUX stage cannot be matched over the whole power range, since the input reflection coefficient varies significantly with power. Matching the AUX at peak power, we show that the phase of the AUX power source, akin to an input offset line [21], can be used to find the best compromise in terms of efficiency, gain and linearity. The MAIN stage is input-matched in back-off [6], where the gain is higher because of the higher load resistance with only 0.5 dB gain penalty at higher power. The final DPA at 12 GHz achieves 9 dB gain, less than 1 dB gain variation from back-off to peak power and a Power Added Efficiency exceeding 45% over a Doherty region of 6 dB OBO.

2. TCAD Simulation Setup for the Doherty Amplifier Design

In this work, we address the design of a GaAs Doherty power amplifier at 12 GHz, exploiting two MESFET devices of identical periphery (1 mm), 0.5 µm gate length and 1 µm gate-drain spacing; see [30] for details. The device output and transcharacteristics are shown in Figure 1. The MAIN amplifier is a class AB stage with 10% I_{DSS} ($V_{GS} = -3$ V) and $V_{DS} = 8$ V, bias conditions that were used in previous works [31] for the design of a single-stage class AB amplifier. The bias point is shown in Figure 1 (red square marks). The optimum power load was found to be $Z_{opt} = (45 + j10)\ \Omega$, corresponding to the optimum load resistance $R_{opt} = 47\ \Omega$ in parallel with the susceptance $B_{opt} = -5$ mS, essentially tuning out the device output capacitance, whose value is found from small-signal analysis to be $C_{out} = 65$ fF. This value will also be used for this work.

In Section 3 we, first analyze the MAIN and AUX amplifiers independently. The simulation setup for this analysis is shown in Figure 2, where the MESFET device is represented with the discretization mesh used for the physics-based analysis, including roughly 3200 nodes. The embedding external circuit is simulated self-consistently with the physical device model (mixed-mode simulations). The device is biased through ideal bias-trees by the gate (V_{GS}) and drain (V_{DS}) power supplies. The output port is loaded on a variable resistance R_{test} in parallel with an ideal tuner Z_{TL}, where $1/Z_{TL} = B_{opt}$ at the fundamental frequency while higher harmonics are shunted (tuned load). Since small-signal simulations show that the device output capacitance mildly depends on the gate voltage, we assume that it can be tuned out in all operating conditions by the output tuner, while the R_{test} value is varied to mimic the load modulation typical of the Doherty operation.

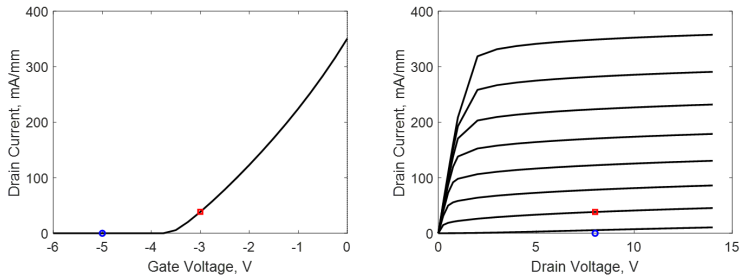

Figure 1. MESFET transcharacteristic (**left**) and output characteristics (**right**). The estimated threshold voltage is −3.75 V. Red square: Class AB bias point (10% IDSS) of the MAIN device and the class AB stage with parallel devices. Blue circle: class C bias point of the AUX device.

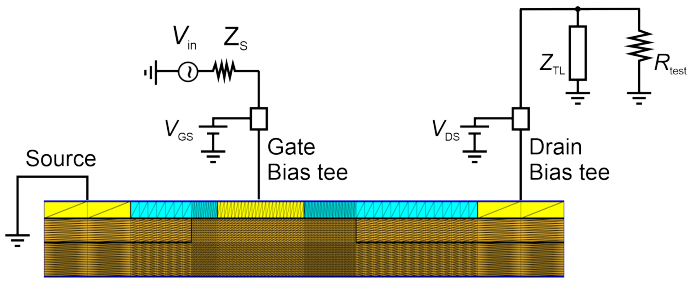

Figure 2. Circuit setup for the single-stage analysis. The resistance R_{test} is set to $2R_{opt}$ or R_{opt} to mimic the operation of the MAIN amplifier in back-off or saturation, respectively. R_{test} is set to R_{DS} or R_{opt} to mimic the operation of the AUX amplifier in back-off or saturation, respectively.

Figure 3 shows the simulation setup used for the TCAD analysis of the complete Doherty amplifier (Section 4). Two identical GaAs MESFETs are biased in class AB and C by the DC supplies V_{GSM} and V_{GSP}, while V_{DS} provides the drain bias (hereafter we will use subscript "M" to denote MAIN quantities and subscript "P" for AUX quantities, where "P" stands for Peaking). The devices are independently fed by two input voltage generators, whose amplitude is adjusted by a fixed ratio α and phase-shifted by ϕ. The available power

at the MAIN and AUX input is kept fixed (α^2) to mimic an input power splitter. In this work, we address a symmetric DPA with an even input power divider ($\alpha = 1$). The phase is first set to $\phi = 90^\circ$ and then adjusted for optimum DPA operation. The source impedances Z_{SM} and Z_{SP} are implemented by ideal tuners and provide input matching. Their value is discussed in Section 4.

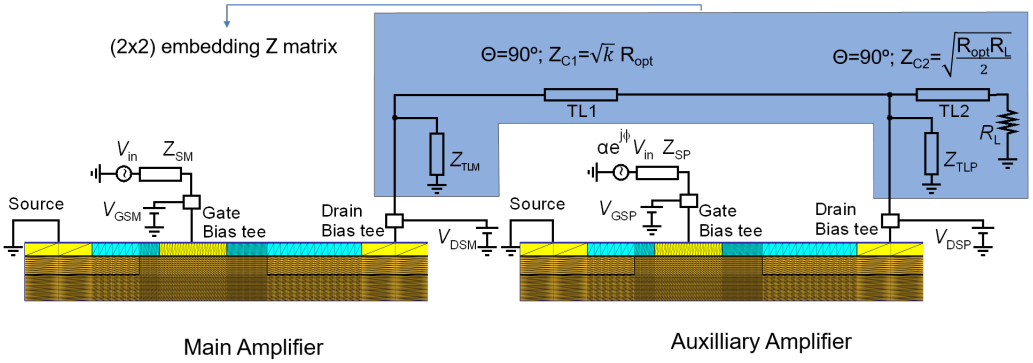

Figure 3. Circuit setup for the TCAD Doherty simulation. In TCAD simulations, the embedding circuit is substituted by an equivalent 2×2 impedance matrix coupling the drain ports of the main and auxiliary devices. The mesh for each device includes roughly 3200 nodes.

The transmission line TL2 with characteristic impedance

$$Z_{C2} = \sqrt{R_{opt} R_L / 2} \tag{1}$$

transforms the output load $R_L = 50\ \Omega$ into the common load $R_{opt}/2$. The transmission line TL1 with characteristic impedance

$$Z_{C1} = \sqrt{k} R_{opt} \tag{2}$$

inverts the impedance for the MAIN amplifier operation in back-off. An optimization parameter $k = 1.15$ is used to compensate the knee voltage reduction in back-off. The MAIN load in back-off is slightly higher than the optimum value R_{opt}.

The MESFETs are considered with no parasitic inductance, a source and drain contact resistance of $3\ \Omega$/mm and gate contact resistance of $5\ \Omega$/mm. Notice that the ideal parallel tuners used for output matching do not introduce any delay in the output combiner; hence, an output offset line is not in principle necessary.

For TCAD simulations, the external network has been converted into a passive 2-port described by its equivalent 2×2 Z matrix, as shown in Figure 3. The two MESFETs with their independent grids have been merged into a unique mesh, equivalent to a 6-terminal device with approximately 6500 grid nodes overall [30]. The two devices interact only through the external network since Neumann boundary conditions ensure isolation at the GaAs level. The Harmonic Balance drift-diffusion system including the Poisson equation, electron continuity equation and circuit external equations was solved, considering eight harmonics. The overall number of equations was 219,980 and the simulation time was approximately 15–30 min for each input power on a Core i9 8 Core PC with 3.6 GHz processor and 64 GB memory, depending on the degree of nonlinearity of the operating condition.

A first demonstration of the TCAD simulation of the Doherty stage of Figure 3 in low-frequency conditions was given in the pioneering paper [30], where a preliminary analysis could identify the AUX optimum bias for class C operation, shown in Figure 1 (blue marks), corresponding to $V_{GS} = -5$ V. The same is adopted in this work.

3. TCAD Simulation of the Main and Auxiliary Stages

We first address the analysis of the MAIN and AUX amplifiers independently, exploiting the simulation setup of Figure 2. The load resistance R_{test} is varied to mimic

the load modulation typical of the Doherty operation: for the MAIN amplifier in back-off $R_{test} = 2R_{opt}$, while in saturation $R_{test} = R_{opt}$; for the AUX stage in back-off a high impedance load is considered, while in saturation the optimum resistance is assumed to be equal to the optimum class AB value; hence, $R_{test} = R_{opt}$. We therefore identify the relevant cases

1. class AB stage ($V_{GS} = -3$ V) & ($R_{test} = R_{opt}$). This represents a conventional class AB stage (used for reference) and also the expected operation of the MAIN amplifier at high power. Hereafter, we refer to this case as "ClassAB" .
2. class AB stage ($V_{GS} = -3$ V) & ($R_{test} = 2R_{opt}$). This represents the expected operation of the MAIN amplifier in back-off. Hereafter, we refer to this case as "DohertyAB".
3. class C stage ($V_{GS} = -5$ V) & ($R_{test} = R_{opt}$). This represents the expected operation of the AUX amplifier at high power. Hereafter, we refer to this case as "DohertyC".

The output power and efficiency for the three cases is shown in Figure 4.

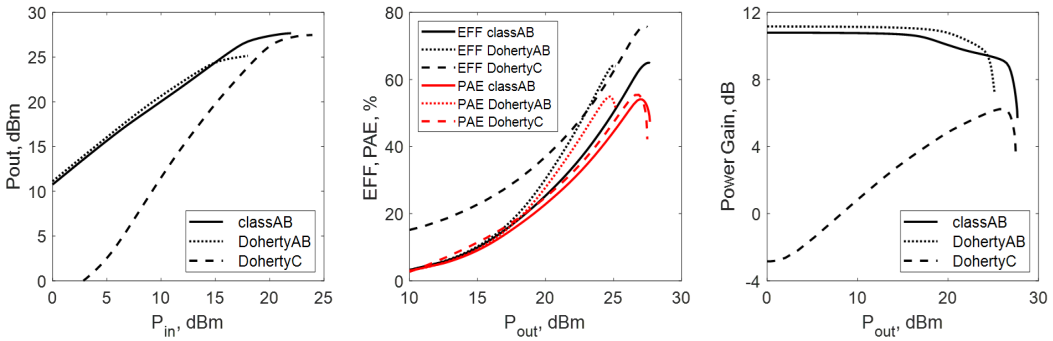

Figure 4. P_{out} (**left**), efficiency and PAE (**middle**) and power gain (**right**) for the three cases: classAB, DohertyAB and DohertyC.

The DohertyC stage, despite the lower gain and the harsher gain compression, reaches a maximum output power of 27.5 dBm, only slightly less than the classAB case (28 dBm). However, the DohertyAB case experiences early compression because of the higher load, and the maximum output power is limited to 25 dBm. The DohertyC stage achieves, as expected, the highest efficiency but, due to the lower gain, shows a significant penalty in terms of Power-Added Efficiency (PAE). The DohertyAB efficiency is higher in back-off and is similar to the classAB at peak power, while the PAE is slightly higher due to the higher gain. The DohertyAB achieves the maximum PAE of 55% at 24.5 dBm output power, roughly 3 dB less than the classAB (54% peak PAE at 27 dBm output power). Overall, the portrait confirms that the stages behave as expected for their use in the Doherty configuration.

In both classAB and DohertyAB cases, the power gain exhibits a mild compression at mid-power, typical of the class AB operation. On the other hand, the class C stage exhibits a significant gain expansion with growing self-biasing. Table 1 compares the performance of the three stages at peak PAE.

Table 1. Summary of Single Stage Amplifiers @ peak PAE.

	P_{out} (dBm)	Eff (%)	PAE (%)	Power Gain (dB)	Gain Compression (dB)
classAB	27	63	54	8.5	2.3
DohertyAB	24.7	62	55	8.8	2.4
DohertyC	26.6	73	55	5.9	N/A

Concerning the input-matching, Figure 5 (left) shows the input reflection coefficient Γ_{in} in the three analysed cases. For the quasi-linear stages, Γ_{in} varies mildly with the input power, confirming that the stage can be matched at the input port over the whole power

range without significant loss of gain. On the contrary, the input reflection coefficient of the DohertyC case shows a significant variation from back-off to saturation. Figure 6 shows the transducer gain and the input return loss resulting when the three stages are input-matched at the highest output power level (High-Power Matching (HPM)), i.e., the generator impedance Z_S of Figure 2 is the conjugate of the impedance AB-HPM (Figure 5, left) for classAB and DohertyAB, and of the C-HPM load for DohertyC. In back-off, the classAB experiences an input return loss of only 0.26 dB and the resulting transducer gain is maximally flat, since the mismatch in back-off compensates the gain compression at high power. The DohertyAB stage in back-off has a more significant return loss (0.5 dB) which, although mild, is important when designing the Doherty stage, since in back-off the Doherty amplifier gain is dominated by the DohertyAB behavior.

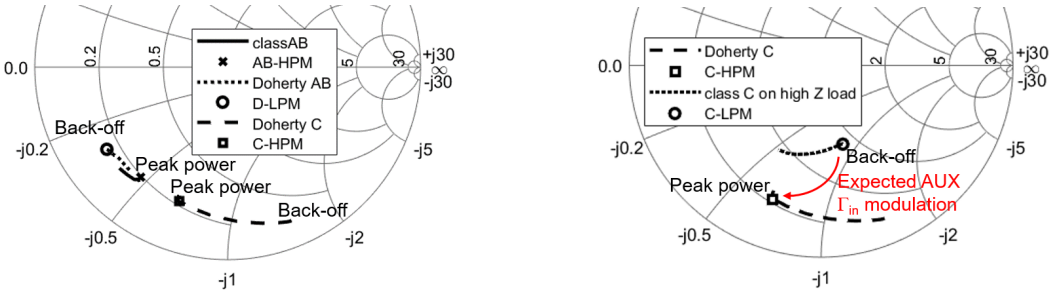

Figure 5. Left: Input reflection coefficient Γ_{in} for the three cases: classAB, DohertyAB and DohertyC. AB-HPM (class AB–High-Power Match) matches the input port of the class AB at peak power. D-LPM matches the DohertyAB amplifier in back-off and C-HPM matches the input port of the DohertyC at peak power. Right: Class C input reflection coefficient of the DohertyC (dashed line) compared to a class C stage loaded with high impedance (equivalent to R_{DS}—dotted line). Red arrow: expected modulation of the AUX amplifier input reflection coefficient in the Doherty amplifier.

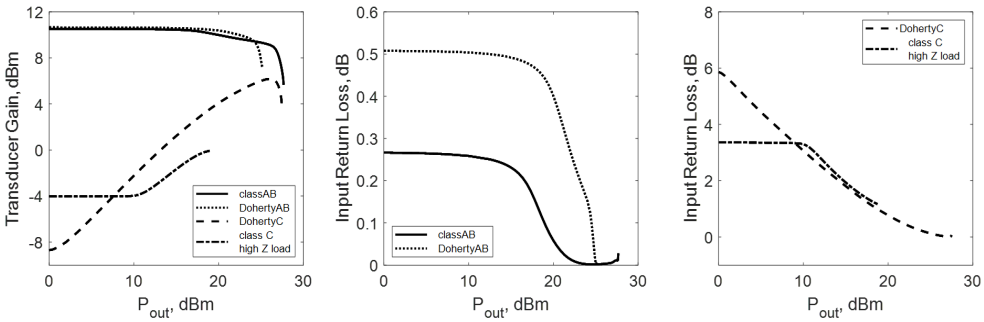

Figure 6. Transducer gain (**left**) for classAB, DohertyAB, DohertyC and classC loaded on high impedance. Input return loss for classAB and DohertyAB (**middle**). Input return loss for DohertyC and classC loaded on high impedance (**right**). All stages are input matched at peak power.

The DohertyC stage shows that the matching is satisfactory at peak power, but the return loss grows to more than 6 dB in back-off, although this is not an operative condition for the class C amplifier in the Doherty stage. In fact, the class C stage in back-off should ideally be loaded by an open circuit, whereas in this simulation, $R_{test} = R_{opt}$. To investigate the Doherty class C in back-off, we repeat the simulation with a high impedance value for R_{test}. Since an infinite impedance is not realistic because of the finite device output resistance R_{DS}, we set $R_{test} = R_{DS}$. The output resistance was extracted from small-signal simulations in the class C bias point and from the slope of the DC output characteristics: the obtained value is consistently found to be $R_{DS} = 700\,\Omega$. The results are reported in Figure 5 (right) and Figure 6 (**classC high Z load** curves). It can be seen that the input reflection coefficient in back-off significantly differs from the DohertyC case: the combination of the feedback device capacitance and of the high resistive load pushes G_{in} towards the centre of the Smith Chart. This reduces the mismatch of the class C stage in back-off and limits the

gain penalty (see Figure 6, left). On the other hand, the class C stage exhibits a more sharp turn-on, which is beneficial for the Doherty operation, but at a higher output power, which may lead to a later turn-on of the AUX stage.

4. TCAD Simulation of the Doherty Amplifier

Following the results presented in Section 3, we identify two possible Doherty configurations that differ only in the input-matching and will be compared in the following. The first choice is to input match both the AUX and MAIN to the AB-HPM load shown in Figure 5. This corresponds to a sub-optimum choice, since only the MAIN amplifier is matched at peak power. We refer to this DPA as the "HPM-DPA case" . In the second DPA, the MAIN amplifier is input matched in back-off (Z_{SM} is conjugate of D-LPM load of Figure 5), while the AUX amplifier is input matched at peak power (i.e., Z_{SP} is conjugate to C-HPM of Figure 5). We refer to this DPA as the "OPT-DPA case". Since the input reflection coefficient of the D-LPM and C-HPM loads have similar amplitudes but differ in phase by 35°, the phase of the AUX input voltage generator is changed with respect to the 90° value, akin to an input offset line, and set to $\phi = 55°$. This allows for the gate voltages of the MAIN and AUX stages to be in the correct phase for the Doherty operation. Finally, a conventional power amplifier parallel combining two identical class AB stages (hereafter the "Parallel-PA case"), loaded on optimum power load Z_{opt} and input matched to AB-HPM was simulated for comparison with the Doherty stages.

Figure 7 shows the output power and efficiency in the three cases. The HPM-DPA and OPT-DPA exhibit a first efficiency peak around 6 dB back-off, as expected, and a second one close to the output power saturation. Both stages outperform the Parallel-PA in terms of efficiency, with a more than 55% peak efficiency at 6 dB output power back-off (OBO) compared to 25% of the conventional paralleled PA. The efficiency is kept high over the 6 dB OBO range and all stages perform similarly in saturation. The maximum output power is in both Doherty amplifiers 30.3 dBm, similar to the Parallel-PA case (30.6 dBm), suggesting that the load modulation prescribed by the Doherty operation is correct in both cases. This is further confirmed by inspecting the load seen at the output port of the MAIN and AUX stages, shown in Figure 8. The reported Γ_L has been de-embedded of the output capacitance to highlight the resistive modulation at the intrinsic device. Notice that in TCAD simulation, there is no exact definition of the intrinsic device, since the device itself does not have any lumped equivalent circuit; nonetheless, bias-dependent small-signal analysis shows that the output capacitance is nearly independent from the bias; hence, it is possible to use the small-signal value of C_{out} to approximately de-embed Γ_L, neglecting the effect of the series parasitic resistances. Despite not being strictly necessary, we believe that the de-embedded results more clearly demonstrate the Doherty load modulation effect. The MAIN amplifier load in Figure 8 varies from $2R_{opt}$ to R_{opt} (i.e., roughly from 100 Ω to 50 Ω being $R_{opt} = 47\,\Omega$). The load seen by the AUX amplifier starts at about 600 Ω in back-off, approaching (despite not exactly) R_{opt} in saturation. The load modulation is best in the OPT-DPA case. Due to the good load modulation, the AUX input reflection coefficient closely follows the behaviour anticipated in Figure 5 (red arrow), with the corresponding mismatch in back-off (Figure 6).

Despite their good performance, the HPM-DPA and the OPT-DPA differ in terms of gain and PAE. Figure 9 (left) shows the power gain: overall, the Doherty amplifiers show a low gain with respect to the Parallel-PA case, and the gain loss is especially noticeable in the Doherty region. Moreover, in the Doherty region, the HPM-DPA exhibits a lower gain than the OPT-DPA, although in back-off the two amplifiers behave in the same way.

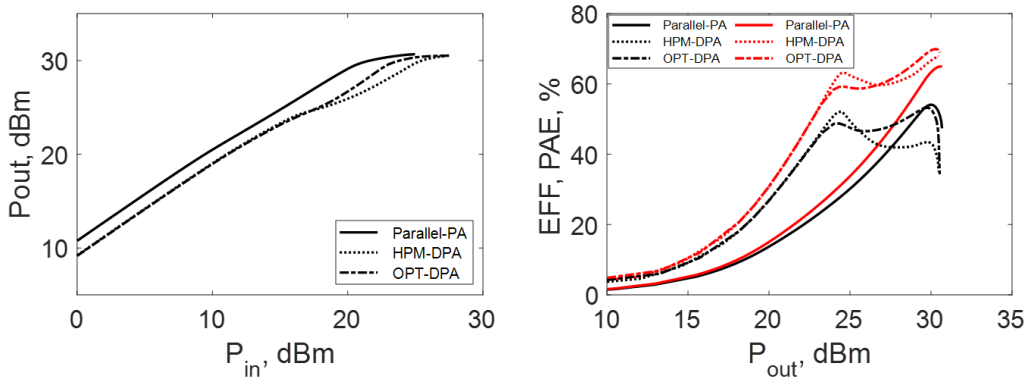

Figure 7. $P_{\text{in}} - P_{\text{out}}$ (**left**), efficiency (**right**, red) and PAE (**right**, black) for HPM-DPA, OPT-DPA and Parallel-PA cases.

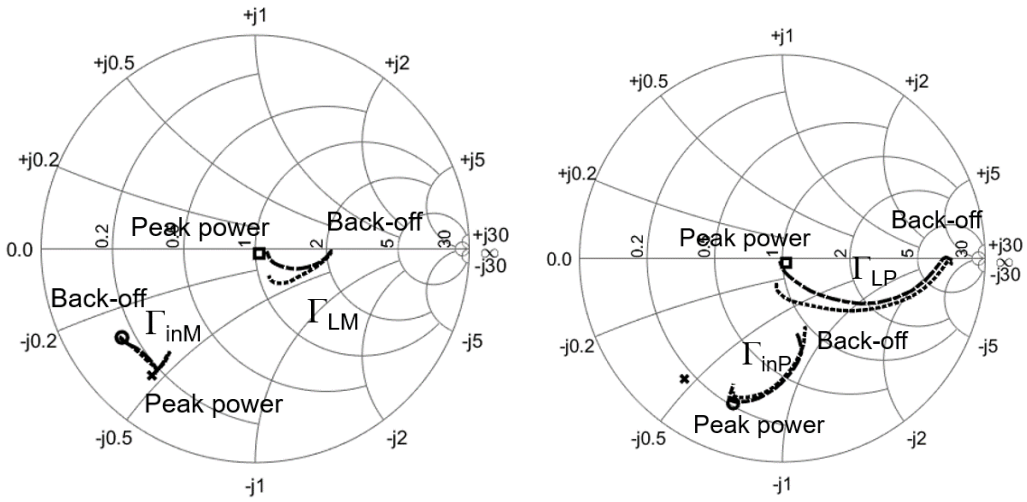

Figure 8. Input (Γ_{in}) and load (Γ_{L}) reflection coefficients seen by the MAIN (**left**) and AUX (**right**) stages for HPM-DPA (dotted line) and OPT-DPA (dashed line). Square: Optimum power load. Cross: conjugate of Z_{SM} (**left**) and Z_{SP} (**right**) in the HPM-DPA. Circle: conjugate of Z_{SM} (**left**) and Z_{SP} (**right**) in the OPT-DPA.

To understand this behavior, Figure 9 (right) reports the $P_{\text{in}} - P_{\text{out}}$ curves of the MAIN and AUX stages separately. Notice that here, the plot is against the available input power of the two stages. Clearly, the AUX of the HPM-DPA turns on later than the OPT-DPA one, due to the higher input mismatch in back-off; see Figure 10 (right). The late AUX turn-on, along with the slow gain expansion of the class C gain (Figure 4), mean that the AUX stage is not efficient in load-pulling the MAIN amplifier. The MAIN gain, in turn, starts to compress because of the knee voltage increase, resulting in a sharp reduction in the overall gain in the Doherty region. This effect is made worse in the HPM-DPA case by the worse mismatch in back-off. The HPM-DPA performance also worsens in terms of linearity, since the power gain continuously degrades in the Doherty region: in fact, as already observed in Figure 8, the AUX stage does not reach the R_{opt} load and the input matching is poor even at peak power; Figure 10 (right). On the contrary, the OPT-DPA stage is well-matched at high power (Figure 10, right) due to the good landing of Γ_{LP} onto R_{opt}.

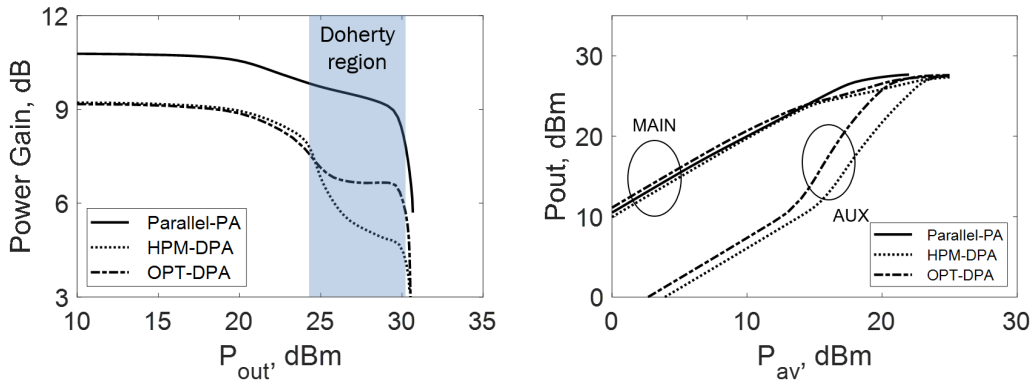

Figure 9. Power Gain (**left**) and Output power of the MAIN and AUX stage separately (**right**) for HPM-DPA, OPT-DPA and Parallel-PA cases.

Concerning the MAIN amplifier, Figure 10 (left) shows that the OPT-DPA is well matched in back-off, while the mismatch grows only mildly in saturation (up to 1 dB): this is compensated in a nearly exact way by the improved input-matching of the AUX stage, resulting in an overall gain that is nearly flat in the Doherty region (see again Figure 9).

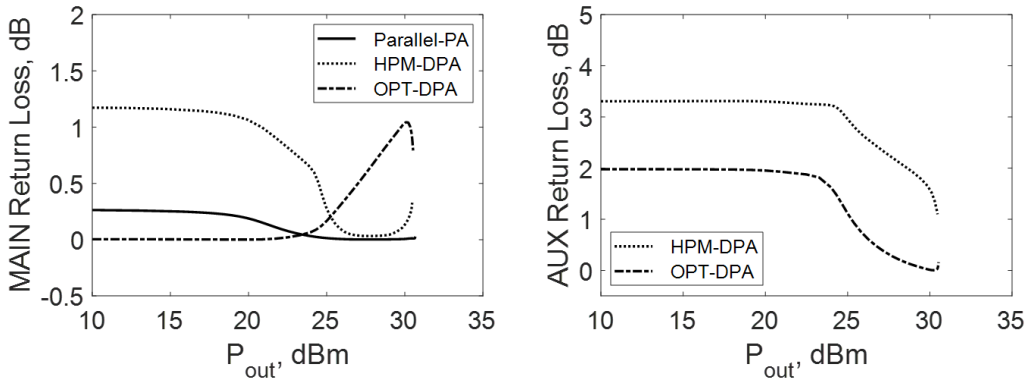

Figure 10. Input return loss of the MAIN (**left**) and AUX (**right**) stage for HPM-DPA, OPT-DPA and Parallel-PA cases.

The poor gain performance of the DPA stages in the Doherty region is reflected in the PAE behavior (Figure 7, right): due to its higher gain, the Parallel-PA outperforms HPM-DPA in the upper portion of the Doherty region, while the OPT-DPA does not offer any improvement.

Overall, the presented results show that the interplay between the input matching and back-off gain must be taken into account in the design of the DPA amplifier. Both DPAs show a late turn-on of the AUX stage, which results in an exceedingly poor gain in the Doherty region, and, overall, a poor linearity in the transition from back-off to Doherty operation. In order to counteract this trend without affecting the gain in back-off, we attempt to turn on the device earlier. By changing the input phase of the AUX amplifier (i.e., the phase ϕ of the voltage source in Figure 3), the MAIN and AUX stages are offset in phase. Figure 11 shows the gain and efficiency resulting from the simulation of a DPA with three different phases, keeping the input and output loads equal to the OPT-DPA case (in fact, the DPA with $\phi = 55°$ is the OPT-DPA itself).

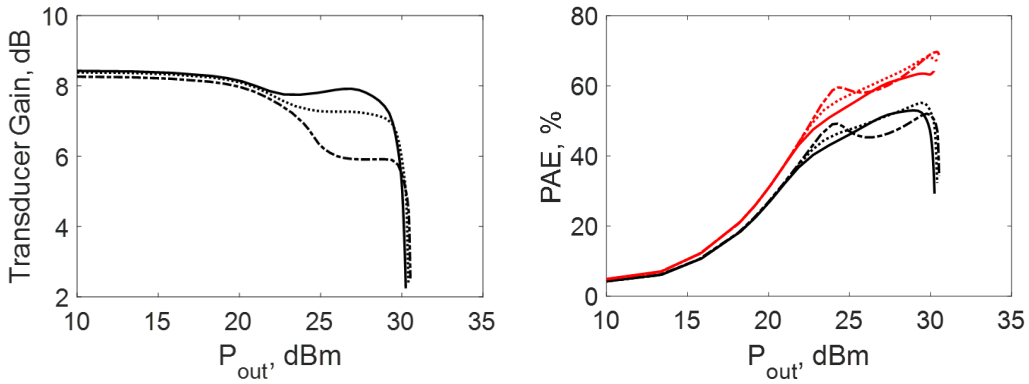

Figure 11. Transducer gain (**left**), efficiency and PAE (**right**) for three values of the AUX input phase: $\phi = 90°$ (solid line); $\phi = 75°$ (dotted line); $\phi = 55°$ (dashed line).

With $\phi = 75°$ and $\phi = 90°$ the first efficiency peak is lost, due to the earlier turn on of the AUX stage (see Figure 12), mainly due to the reduced AUX mismatch in back-off, as shown in Figure 13, where we notice a significant reduction in the G_{in} walk-out in the Smith chart from back-off to peak power. The penalty in terms of efficiency, though, is mild (within 5%), preserving the overall DPA performance. The PAE of the phase-shifted DPAs is ameliorated with respect to the OPT-DPA case ($\phi = 55°$), and does not exhibit the efficiency minimum in the middle of the Doherty region.

Besides efficiency, the gain is also significantly improved and becomes nearly flat in the whole power range for $\phi = 90°$, or reflects a residual mild reduction of 1 dB in the Doherty region for $\phi = 75°$. Despite the load modulation not being perfect—see Figure 13—the DPAs with $\phi = 75°$ reaches a saturated output power only 3% less than the OPT-DPA case ($\phi = 55°$), with a PAE reduction of 5% at 6 dB OBO (see Figure 14). For higher values of the phase offset (e.g., $\phi = 90°$), the modulation of the MAIN load is too poor and the output power is affected by a reduction of nearly 10%, which is considered unacceptable. Overall, the DPA with $\phi = 75°$ achieves 9 dB gain with less than 1 dB gain variation from back-off to peak power and a PAE exceeding 45% 6 dB OBO.

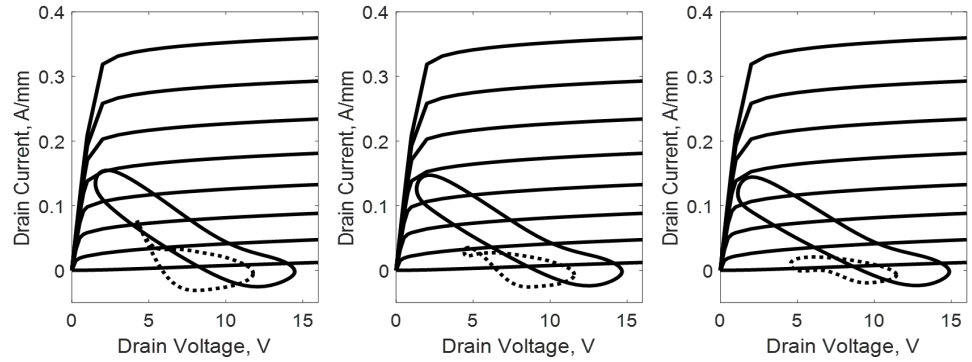

Figure 12. DPA MAIN (solid) and AUX (dotted) dynamic load lines at the AUX turn-on for the three values of the AUX input phase: $\phi = 90°$ (**left**); $\phi = 75°$ (**middle**); $\phi = 55°$ (**right**). The available input power is the same, the output power is 24.8 dBm (**left**), 24.3 dBm (**middle**) and 23.9 dBm (**right**).

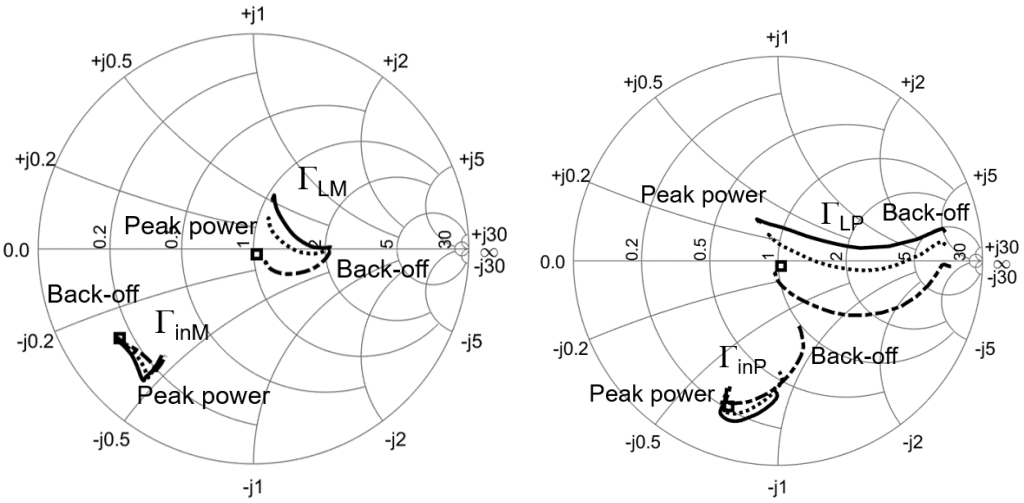

Figure 13. Input and load reflection coefficients seen by the MAIN (**left**) and AUX (**right**) stages for three values of the AUX input generators: $\phi = 90^\circ$ (solid line); $\phi = 75^\circ$ (dotted line); $\phi = 55^\circ$ (dashed line).

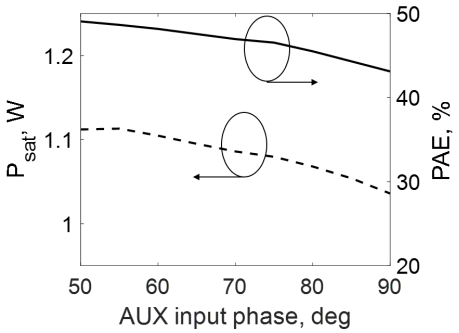

Figure 14. DPA-saturated output power (solid line) and peak efficiency (dotted line) as a function of the AUX input phase.

5. Conclusions

In this work, we have shown that our in-house mixed-mode drift-diffusion TCAD simulator [29], recently extended to simulate microwave circuits including multiple active devices [30], is an effective tool to investigate the optimum design of Doherty amplifiers. We have presented, for the first time, a comprehensive analysis of a GaAs Doherty amplifier, focusing in particular on the input matching and the resulting DPA gain. We emphasize that all the results presented in this paper were obtained uniquely by TCAD large-signal simulations. In particular, this is the first time TCAD simulations are also presented for the comprehensive analysis of a class C amplifier. In fact, TCAD simulations of the individual MAIN and AUX stages have shown that the DPA performance critically depends on the accuracy of the class C capacitive modelling, and particularly on the device feedback capacitance, which impacts the AUX input-matching network.

This work provides a means for advanced analyses of the Doherty stage using the additional capabilities of the in-house software, such as the Small-Signal Large-Signal and conversion Green's Function analyses, which have already proved to be extremely useful for the optimization of microwave stages [32], for the sensitivity analysis of microwave device performance against technological variations [33], and for the development of accurate circuit level models, e.g., through X-parameters, both for the individual MAIN and AUX stages and for the complete DPA.

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Conflicts of Interest: The authors declare no conflict of interest.

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