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The atmospheric neutron poses a serious hazard to nanoscale electronics reliability. Spallation neutron irradiations on a nanoscale system on chip (SoC) were conducted applying the China Spallation Neutron Source (CSNS), and the results were compared and analyzed using Monte Carlo simulation. The contribution from thermal neutron on the SoC single event effect (SEE) was analyzed. Analysis indicated the SoC atmospheric neutron SEE vulnerability can be reduced by 44.4% if the thermal neutron was absorbed. The influences of the B and Hf elements on the SEEs were evaluated, too. It can be concluded that ^{10}B interacting with thermal neutron is the reason for thermal neutron inducing SEE in the SoC. Although the Hf element has no contribution to the 28 nm SoC atmospheric neutron SEE cross section, it increases the total dose risk 5 times during atmospheric neutron irradiation.

Keywords: Spallation Neutron; Monte Carlo; System on Chip; Thermal Neutron; Single Event Effect

1. Introduction

In 2001, Robert C. Baumann first reported ^{10}B interacting with thermal neutron is a dominant factor in soft errors for deep-submicron static random access memory with boro-phospho-silicate glass (BPSG) packages.[1] Since then, advanced integrated circuit development makes the chip packages get rid of the BPSG package.[2-3] The nanoscale electronics, however, even though the BPSG package is not available anymore, they have to face the risk from ^{10}B interacting with thermal neutron once again.[4-7] The reason is ^{10}B still existing in the semiconductor contact and doping processes, and the rapidly developed semiconductor manufacturing technology pushes their supply voltages and single event effect (SEE) critical charges lower and lower.

In [6], C. Weulersse examined a variety of memories taking advantage of multi neutron sources and pointed out the related reliability problem. SEE, induced by ^{10}B in nanoscale memories via interacting with thermal neutron, is even close to that caused by high energy neutrons. In [8], the 65 nm microcontroller unit (MCU) without BPSG was irradiated with thermal and high energy neutrons, and the influence of ^{10}B on SEE was investigated. The results demonstrated that the contribution of ^{10}B interacting with thermal neutron even dominated the atmospheric neutron SEE in the device. Specifically, the SEE ratio induced by thermal and higher energy neutrons on the 65 nm MCU reached 1.89:1.[8]

The 65 nm MCU test results signify that the interaction of ^{10}B with thermal neutron is still serious to advanced integrated chips. For the 28 nm SoC, besides the boron contamination, another is also introduced: the hafnium (Hf) element. Compared with boron (B), the neutron cross section with Hf is higher at several eV intervals. Fig.1 displays the neutron cross section spectrums of ^{10}B, ^{178}Hf, and ^{28}Si.[9] It can be viewed the peak cross section of ^{178}Hf even achieves 10^5 barns. The cross sections of ^{178}Hf with thermal neutron are also higher than that of ^{28}Si by two orders of magnitudes. Another significant fact is that the B element exists in the

28 nm SoC as the contamination from manufacturing processes, while the Hf element is a component of the metal gate in the 28 nm SoC. This process makes the 28 nm SoC atmospheric neutron SEE evaluation become more complicated.

For the 28 nm SoC atmospheric neutron SEE, the first irradiation test has been conducted at the China Spallation Neutron Source (CSNS)-BL09.[10] In the irradiation, the neutron beam hited the chip directly without any shield, and the neutron spectrum covered the thermal and high energy neutrons. To explore the atmospheric neutron SEE on the 28 nm SoC further, the second irradiation on the SoC was performed once more. But a 2 mm cadmium (Cd) slat was used to absorb the thermal neutron before the irradiated chip compared with the previous. By comparing the two irradiation results, thermal neutron's contribution to the 28 nm SoC can be investigated. Meanwhile, the B and Hf elements' influence can be analyzed from the irradiation and the Monte Carlo simulations.

2. Irradiation Tests

The actual atmospheric neutron SEE test is time-consuming, and the spectrum of the spallation neutron source is the closest to the real one. Thus, it is considered the ideal atmospheric neutron source.[11] Scale-down manufacturing technology makes it urgent to undertake more available atmospheric neutron SEE irradiation studies. The China spallation neutron source was implemented in 2018 and made it come true to launch atmospheric neutron SEE tests using a spallation neutron source in China.[12] Fig.2 shows the calculated differential flux of the neutron beam of CSNS (10^9 of Peking ground).

Based on the CSNS-BL09, two SEE irradiation tests were conducted on the 28 nm SoC. In [10], the first irradiation test was performed, and the SoC was irradiated by the neutron beam directly without any shield. In the second irradiation test, that is the current work, a 2 mm Cd slat was placed between the beam ejection stop and the tested chip to absorb thermal neutrons. Fig.3 displays the neutron spectrum at the terminal with and without the 2 mm Cd slat [8]. It can be seen that the 2 mm Cd slat absorbs the neutrons effectively whose energies are below 0.5 eV.

The on-chip memory (OCM) block of the Xilinx Zynq-7000 SoC was tested in two irradiations. The 64 kB data in the OCM were tested dynamically. The check pattern data, 0xA5A5A5A5, were written into the OCM addresses and read back by the SoC, and the SoC compared the readback one with the check pattern data to determine whether a SEE took place. The comparison results was moved to PC and refreshed in a termial. It requires to compare results with the first irradiation, where the normal condition is examined without any mintigation techniques. Hence, the same condition is available in this effort.

In both irradiations, the test establishments are the same except the 2 mm Cd slat. A 2260B programming DC power supplied the test board. The real-time current was monitored and recorded by the remote host computer, and the possible single event latch-up was also investigated. The host computer and the test board communicated through a universal serial bus cable, and the running messages were recorded in real-time.

3. Results and Discussions

Four kinds of soft errors were detected in both irradiations, including the single bit upset (SBU), dual cell upset (DCU), multi-cell upset (MCU), and single event functional interruption (SEFI). No abnormal current was detected, which means no latch-up event emerged in the 28 nm SoC atmospheric neutron SEE irradiation tests. However, there are some differences between the two irradiations in terms of SEE cross section. This discrepancy signifies thermal neutron impacts the 28 nm SoC atmospheric neutron SEE.

3.1. The Detected Events

In the second irradiation, 19 events were detected. Table I lists the number of each type of error. The number of SBU events is more than others. It is similar to that in the first irradiation.

During the second irradiation, the neutron flux above 1 MeV was about 6.85×10^5 $n\cdot cm^{-2}\cdot s^{-1}$ and the corresponding fluence was 2.47×10^{10} $n\cdot cm^{-2}$. Hence, the SBU cross section is $(5.26\pm0.26)\times10^{-10}$ cm^2 and $(1.00\pm0.05)\times10^{-15}$ $cm^2\cdot bit^{-1}$ for the irradiation with few thermal neutrons.

Table I. The detected SEE in irradiation with few thermal neutrons

SBU	DCU	MCU	SEFI
13	2	2	2

Table II. The detected SEE in irradiation with thermal and high energy neutrons.[10]

SBU	DCU	MCU	SEFI
21	4	2	5

Table II presents the detected SEE in the first irradiation. It can be seen the number of SBU events is 21 in the irradiation, which is also more than others. In Table I and II, it is evident that SBU events dominate the detected soft errors in both irradiations.

Table III presents the SBU cross sections in two irradiations. The neutron fluence of the second irradiation is 2.47×10^{10} $n\cdot cm^{-2}$, higher than that of the first irradiation by 11.26%, however, the number of SBU event in the second irradiation is 13 instead of more than 21. This phenomenon implies thermal neutron has a contribution to the 28 nm SoC atmospheric neutron SEE. The discrepancy between the bit cross sections is 0.8×10^{-15} $cm^2\cdot bit^{-1}$. Since the critical difference between two irradiations is containing thermal neutron or not, it can be speculated thermal neutron causes the discrepancy. It attests the SEE sensitivity of the 28 nm SoC can be reduced by about 44.4% by shielding thermal neutron with a 2 mm Cd slat. All these demonstrate that risks from thermal neutron cannot be neglected, even though the nanoscale chips get rid of BPSG in packages.

Table III. The SBU cross sections in two irradiations.

Neutron Beam	Fluence 10^{10} cm^{-2}	SBU	Cross section 10^{-10} cm^2	Bit cross section 10^{-15} $cm^2\cdot bit^{-1}$
CSNS-BL09 [10]	2.22	21	9.46±0.47	1.80±0.09
CSNS-BL09+2mm Cd	2.47	13	5.26±0.26	1.00±0.05

3.2. B Influence

The 65 nm MCU atmospheric neutron irradiation results indicated that the secondary particles from thermal neutrons interacting with ^{10}B could result in SEU on advanced electronic systems. Compared with the 65 nm memory cell, the SEU critical charge of the 28 nm memory cells is lower, and thermal neutron is easier to induce soft errors in the 28 nm process cells.

$$^{10}B+n_{th}\rightarrow{}^{7}Li(1.01\ MeV)+\alpha(1.78\ MeV) \qquad (3\text{-}1)$$

$$^{10}B+n_{th}\rightarrow{}^{7}Li(0.84\ MeV)+\alpha(1.47\ MeV)+\gamma(0.48\ MeV) \qquad (3\text{-}2)$$

Formulas (3-1) and (3-2) describe the mechanisms of thermal neutron (n_{th}) reacting with ^{10}B. The probability of (3-1) is 6.3%, and that of (3-2) is 93.7%.[13] It means the key of thermal neutron inducing SEE in the 28 nm SoC is $^7Li(0.84$ MeV) and α(1.47 MeV) particles. They deposit energy in the sensitive volumes. Table IV shows the ranges in silicon and the linear energy transfers (LETs) of the two secondary particles.[14] The ranges in silicon of α(1.47 MeV) and $^7Li(0.84$ MeV) are just 5 μm and 2.5 μm, which are much less than the thickness of the 28 nm SoC from top passive layers to substrate's surface.[15] This phenomenon preliminarily reveals that the B contamination exists inner the chip and approaches sensitive volumes of the

SoC. The SEE LET threshold of the 28 nm cell is approximately 0.50 MeV·cm^2·mg^{-1}.[16] For ^{7}Li(0.84 MeV) and α(1.47 MeV), the LETs are 2.10 MeV·cm^2·mg^{-1} and 1.15 MeV·cm^2·mg^{-1}, respectively. They are higher than the threshold, which means both secondary particles can induce SEE in 28nm SoC.

Table IV. The ranges and LETs of secondary particles of ^{10}B with the thermal neutron.

Rang in silicon/μm		LET/MeV·cm^2·mg^{-1}	
^{7}Li(0.84 MeV)	α(1.47 MeV)	^{7}Li(0.84 MeV)	α(1.47 MeV)
2.5	5	2.10	1.15

It is different from the 65 nm MCU, the Hf element also exists inner the 28 nm SoC, and the cross section of Hf with thermal neutron is even higher than that of silicon. Thus, it cannot conclude the difference is induced by ^{10}B directly.

3.3. Hf Influence

^{10}B, in the 28 nm SoC, interacts with thermal neutron inducing SEE, that mainly comes from the high probability of nuclear reaction. However, as Fig.4 displays, the primary interaction of thermal neutron and the Hf element is the (n, γ) reaction,[9] and the γ rays usually results in total ionization dose rather than SEE in the device.[17] Because the generated γ rays cannot cause SEE directly and have to interact with other atoms to produce secondary heavy ionization particles, this possibility is relatively low.

Compared with high energy neutrons, cross sections of ^{178}Hf interacting with the eV level neutrons even achieve 10^5 barns. In this case, whether the hafnium element contributes to 28 nm SoC atmospheric neutron SEE, required to be comprehensively assessed.

In Fig.4, the peak's reaction of ^{178}Hf with several eV neutrons is elastic or (n, γ). As mentioned above, the contribution from (n, γ) reaction to induce SEE in 28nm SoC is rather low. Neutron in elastic interaction can transfer energy to hafnium atoms, it might increase the probability of causing SEE. The maximum transfer energy to the Hf atom from neutron can be calculated with the formula (3-3). [18]

$$\mathrm{Et} = \frac{4\mathrm{MnMt}}{(\mathrm{Mn+Mt})^2}\mathrm{En} \quad (3\text{-}3)$$

Et is the max energy transfer to Hf atom with keV, Mn is the mass of the neutron, which is 1.67×10^{-27} kg, Mt is the Mass of Hf and it is 2.96×10^{-25} kg, and En is the energy of neutron with keV.

The current work mainly discusses soft error in the 28 nm SoC induced by thermal neutron reacting with the boron and hafnium elements. As stated in Section 2, the neutron with energy less than 0.5 eV are obsorbed by a 2 mm Cd slat. For the 0.5 eV neutron, the maximum transferred energy to Hf atom is about 0.01 eV. Meanwhile, considering the peak elastic cross section in Fig. 4, even though it extends the neurton energy to the rightmost peak, the corresponding max transferred energies are lower than 0.03 keV. Considering their LETs (the corresponding LETs are less than 0.50 MeV·cm^2·mg^{-1}), these are all impossible to lead to SEE on the SoC. It testifies the high cross section elastic interaction from Hf with thermal and eV neutrons does not affect 28nm SoC atmospheric neutron SEE.

Hence, it can be concluded the soft error difference between the two irradiations is mainly caused by ^{10}B.

3.4. Monte Carlo Simulation

The cut cross section of the chip is investigated and captured, as shown in Fig. 5, the thickness and materials of the passive layers were obtained.[10, 15] Meanwhile, the 28 nm High-k metal gate (HKMG) technology gate contains TiN(8 nm), HfO_2(10 nm), and SiON(1.2 nm),[19] and the ultra-thin SiON layer can also be an ultra-thin SiO_2 layer in the HKMG technology.[20] Relying on these effort and information, two Geant4 Monte Carlo simulation models were constructed to examine the Hf element's influence.[21, 22] In Fig.6, the TiN and ultra-thin SiO_2 layers are considered only in the first model, while the TiN, HfO_2, and ultra-thin SiO_2 layers are considered simultaneously in the second model in Fig.7. Others are the same for the two simulation models.

The spectrum of neutron sources in the simulation is the same as in the first irradiation test, which includes thermal and high energy neutrons. The number of neutrons is 10^7, and the surface area of the model is 10 μm×10 μm. 32×32 sensitive volumes (SVs) are placed, the size of the volume is 130 nm×130 nm×130 nm, and the critical charge is 0.18 fC. During the simulation, if the deposited energy in an SV overs the critical charge in an EventAction, which means an SEU emerged.

The number of the upset event in the cells and deposited doses in the ultra-thin SiO_2 layer were recorded in both simulations and shown in Table V. It can be seen the number of the upset event and the cross section are the same in both simulations. Still, the deposited dose in the ultra-thin SiO_2 layers differs by almost 5 times. The simulation results verify that the Hf element does not influence 28 nm SoC atmospheric neutron SEE. However, the existence of hafnium may increase the total dose risk during atmospheric neutron SEE irradiation. In Fig.4, the high (n, γ) cross section also underlines this possible outcomes, because more γ rays means more possible total ionization dose risk. And the simulation results is consistent with that. It suggests total dose risk monitoring is necessary in much more fluence atmospheric neutron SEE irradiation tests for the SoC.

Table V. The upset number and deposited doses in two simulations.

Upset number		Bit cross section/$cm^2 \cdot bit^{-1}$		Deposited Dose/rad	
First Model	Second Model	First Model	Second Model	First Model	Second Model
5	5	5×10^{-16}	5×10^{-16}	12.6	63.3

Up to now, we evaluated the 65 nm MCU and 28 nm SoC atmospheric neutron SEE depending on CSNS. In the future, more SEE irradiations and assessments will be explored further.

4. Conclusion

The 28 nm SoC was irradiated twice at CSNS-BL09. In the first irradiation, the specture covered the thermal and high energy neutron, while thermal neutrons were shielded in the second. The differences in the results were analyzed. The discrepancy between the two irradiation tests is caused by ^{10}B interacting with thermal neutron. If thermal neutron in the atmospheric environment is shielded by a 2 mm Cd slat, the 28 nm SoC SEE sensitivity can be decreased by 44.4%. The hafnium element does not influence the 28 nm SoC atmospheric neutron SEE, although it also has a high interaction cross section with thermal neutron. The evaluation illustrated attention should be paid to total dose hazard during the 28 nm SoC atmospheric neutron SEE irradiation, since the hafnium element increases the total dose risk.

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