ALICE Zero Degree Calorimeters. The new readout system in LHC Run 3

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The new readout system in LHC Run 3

S.C. Zugravel[a,b], P. Cortese[c,b], G. Cotto[d,b], N. De Marco[b], P. De Remigis[b], L. Lombardo[a,b], G. Mazza[b], C. Puggioni[e], E. Puleo[d,b], L. Quaglia[d,b] and M. Sitta[c,b]

[a] *DET del Politecnico, Torino, Italy*
[b] *Sezione INFN, Torino, Italy*
[c] *DISIT dell'Università del Piemonte Orientale, Alessandria, Italy*
[d] *Dipartimento di Fisica dell'Università, Turin, Italy*
[e] *Sezione INFN, Cagliari, Italy*

E-mail: stefan.zugravel@to.infn.it

Abstract: The Zero Degree Calorimeters (ZDC) were designed to provide the measurement of the event geometry and luminosity in heavy-ion operation. The readout system was redesigned in order to operate in continuous mode without dead time at 2.5 MHz event rate. The new acquisition chain is based on a commercial 12 bit digitizer with a sampling rate of about 1 GSps, assembled on an FPGA Mezzanine Card. The signals produced by the 26 ZDC channels are digitized, and samples are processed through an FPGA to extract information such as timing, baseline average estimation and luminosity.

Keywords: Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Front-end electronics for detector readout

Contents

1 Introduction

The ZDC of the ALICE experiment consists of two identical sets of calorimeters located on both sides of the interaction point IP2 (side A and C), 112.5 m away from it [1, 2]. In that region the two LHC beams circulate in two different pipes. Each set of detectors consists of a neutron (ZN) and a proton (ZP) calorimeter. The ZN is placed at zero degree with respect to the LHC axis, between the two beam pipes, while the ZP is positioned externally to the outgoing beam pipe. Collisions may occur in fixed time slots named bunch crossings (BC) that are separated by $\sim$ 25 ns. ZDC is mainly sensitive to spectator nucleons. The spectator protons are separated from the ion beams by means of a dipole magnet, while spectator neutrons fly at zero degrees without further changing direction. The ZDC detector is completed by 2 forward EM calorimeters (ZEM) placed at about 7.35 m from IP2, on side A. The ZDCs are quartz-fiber spaghetti calorimeters with silica optical fibers as active material embedded in a dense absorber. The main purpose of these calorimeters is to provide an independent measurement of the time of the collision, of the vertex position, centrality, event plane and to measure the luminosity in heavy-ion collisions [3–6]

2 The ZDC readout system and challenges

In order to exploit the potential offered by the LHC increased luminosity in Run 3, the ALICE experiment upgraded its trigger and readout system, to be able to acquire all collisions in self-triggered mode without dead time[7–9]. The purpose of the ZDC readout upgrade was to enable the detector to cope with the increased event rate while preserving its time and charge resolution performance. The operating conditions for the ZDC are extremely challenging, in particular concerning Pb-Pb collisions, due to the presence of electromagnetic dissociation processes (EMD) [10, 11]. When running in self-triggered mode the ZDC system will need to sustain a readout rate of $\sim$ 2.5 MHz for the channels of the most exposed calorimeters that compares to the foreseen hadronic rate of 50 kHz sustained by the other detectors. The previous electronics, based on Charge-to-digital converters (QDCs), with a fixed dead time of ∼ 10 μs, and on readout through VME bus, could not cope with such a high rate [12]. Moreover a crucial aspect of the ZDC operation in Run 3 is acquiring the events with a reduced bunch spacing of 50 ns (lower than the length of the signal of ∼ 60 ns) in the presence of a large signal dynamics (from a single neutron to ∼ 60 neutrons).

3 The readout architecture

Given the low number of channels of the detector (26), the new readout is based on commercial FPGA Mezzanine Card (FMC) digitizers that allow a continuous sampling of the signal waveform followed by a real time analysis on a FPGA. The chosen digitizer is the ADC3112 from IOXOS, each mounting two TI ADS5409 ADC. Every FMC module has 4 channels, a maximum sampling rate of 1 GSps, 12 bit resolution (with an ENOB of 10 bit) and can be configured with 50 Ω termination [6]. The ADC is configured applying a low pass filter and subsequent 2x decimation filter, with the purpose to reduce the total noise and the sampling rate down to 480 MSps. Thanks to the adequate bandwidth available through the FMC connection from the digitizer to the FPGA the full waveform can be analyzed, thus the time and charge resolution of the previous system can be preserved while still allowing the required acquisition rate for Run 3. Each digitizer is mounted on a commercial IFC1211 VME carrier from IOXOS. The VME format was chosen in order to exploit the existing infrastructure. The readout, however, will not be carried out via VME, but on CERN developed 4.8 Gbps bi-directional optical links (GBT)[13] implemented through commercial TAS-A2NH1-P11, multimode, 850 nm, SFP+ transceivers. Each carrier contains a Xilinx FPGA Kintex Ultrascale xcku040-1ffva1156 and a PowerPC processor. A fast trigger logic is executed on the FPGA and the interesting portions of the waveform are transferred to the acquisition and reconstruction system through the GBT links. Each readout module uses two GBT links, namely Link 0 and Link 1. Link 0 is used for channel 0 and 1 data transmission and for receiving the orbit number information, trigger messages from the Central Trigger Processor (CTP)[14], start/stop commands and synchronization signals, while Link 1 is used for channel 2 and 3 data transmission and for receiving configuration commands from the Detector Control System (DCS). Each channel can be selectively enabled or disabled for readout by means of a configurable 4 bit readout mask. A scheme of a readout module is shown in figure 1. The complete detector readout system uses a total of 8 modules, thus having a maximum of 32 usable channels. Digitized data are aligned with the appropriate BC by means of two delay parameters for each channel and, if the auto-trigger algorithm is satisfied, data from the corresponding BC is flagged for acquisition[15].

4 The trigger algorithm

A trigger algorithm has been developed and tested with digitized data [15]. The algorithm involves differences between samples that are compared to a threshold t. Indicating with y_i the i^{th} ADC sample and considering that the signal has negative polarity, the trigger can be evaluated with a double (eq 4.1) or triple (eq 4.2) condition, the first one being more sensible to pile-ups, while the second one offering better protection from the electronic noise.

$$T = (y_i - y_{i+k} > t) \wedge (y_{i+1} - y_{i+k+1} > t) \tag{4.1}$$

$$T = (y_i - y_{i+k} > t) \wedge (y_{i+1} - y_{i+k+1} > t) \wedge (y_{i+2} - y_{i+k+2} > t) \tag{4.2}$$

The choice between double and triple condition is configurable and can be changed on the fly before the data taking without firmware modifications. Typical values for the algorithm parameters are $k = 4$ and $t = 10$. The trigger algorithm runs on every channel and sets the auto-trigger flags independently for each channel. The logic reads the auto-trigger flags of the different channels of each module and puts them in logic AND with a configurable trigger mask. If the result is not zero this provides the global trigger decision for the module.

5 Firmware architecture

The main firmware blocks are summarized in figure 1. The logic is working at ~ 240 MHz, thus six clock cycles are available to process the information produced in a bunch crossing. The Link 0

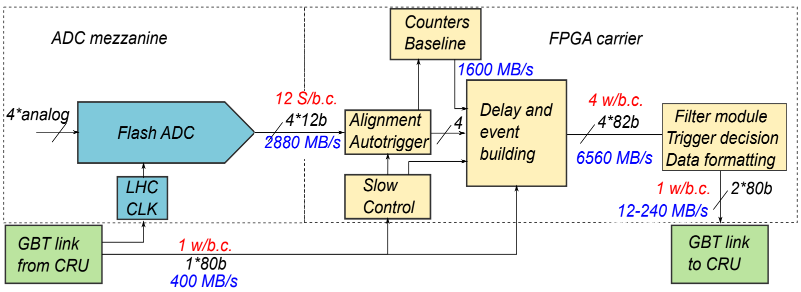

Figure 1. The rate of information for each link is shown in red text, in black the number of lanes multiplied by the bus width and in blue the data bandwidth[15].

upstream payload coming from the Common Readout Unit (CRU)[16], conveying trigger messages, is 80 bit for each bunch crossing and is fanned-out to the processing pipelines of each channel. The Link 1 upstream payload is reserved for 80 bit Single Word Transfer (SWT) messages which are used for slow control board management, in particular for writing or reading configuration parameters, for sending reset commands, for triggering the auto-calibration of the delays, for reading the status of the two links or the FIFOs memories and for enabling or disabling a "special run" data acquisition mode, where a larger portion of the waveform is transferred. Each word passes through a handler which is connected to the main event building module. The digitized data, after decimation, result in 12 words of 12 bit per channel and per bunch crossing. Firstly, the signals are aligned in the center of the bunch crossing with a resolution of 1 sample by means of a shift register of configurable length. This procedure is done automatically by the firmware logic at every new fill of LHC and it works by calculating the average sample at which an auto-trigger fires and the subsequent compensation delay value. After synchronization, a configurable number of trigger differences from eq 4.1 or eq 4.2 (between 0 and 12) are evaluated in a window of 12+2 samples related to the current crossing and the beginning of the next one. If the selected trigger condition is satisfied, then the bunch is flagged for acquisition. Information from an internal orbit counter, bunch crossing counter, and number of hits along the orbit are also inserted in the data stream for every channel. Collisions at the IP can occur only in well-defined bunch crossings, depending on the active LHC filling scheme. This feature is exploited to identify the bunch crossings that are free from any signal and can be used to evaluate the average baseline for each orbit. The first stage of the event building combines the different pieces of information into four words 82 bit long for each channel by means of a ring buffer delay that synchronizes the output of the digitizer with the ALICE trigger information and with locally computed quantities. The full information of each bunch crossing is then passed to the second stage of event building using a FIFO. The final filter module verifies the presence of auto-trigger or ALICE trigger flags, checks if there are interactions in the three preceding bunch crossings (pile-up) and verifies the presence of the "special run" condition. At this point the data can be formatted and transmitted to the CRU. If the filter module does not detect any trigger flag then the event is discarded from the FIFO. In auto-trigger mode, each active channel produces a payload of six 80 bit long words, out of which three are for the signal and the other three are the samples of the previous bunch crossing (with respect to the triggered bunch crossing), that are used to perform a more accurate baseline subtraction during reconstruction and to detect the presence of pile-up. The payload bandwidth ranges from ~ 12 MBps for the modules with lower occupancy (connected to the detectors sensitive mainly to hadronic collisions) to about ~ 240 MBps for the four modules dedicated to the readout of the neutron calorimeters.

6 Detector segmentation and cabling

The auto-trigger strategy takes advantage of the segmentation of the detectors. The light produced by the hadronic showers is collected in such a way that half of the signal is readout by a common photomultiplier (TC) and the other half by fibers that are bundled to divide the detector into four towers [15, 17] readout by four different photomultipliers (T1, T2, T3, T4). In normal operation the auto-trigger of each neutron calorimeter is based on the TC signals since it has the best energy resolution. These signals are therefore fanned-out to two modules but readout only once. The analog signals of the four towers are summed (SUM) to provide an alternative auto-trigger in case of failure of the common photomultiplier and therefore are fanned-out to two modules too. The remaining four free channels are dedicated to the readout of the four towers. For the proton calorimeters the redundancy requirement is less stringent. A cabling scheme is shown in table 1. In order to exploit the full input dynamics of the digitizer, the input signals are shifted by ~ 450 mV.

7 Performance and conclusions

The readout chain and the auto-trigger algorithm were tested using a pulse generator in laboratory during development and using a laser to stimulate the photomultipliers during the testing at the ALICE site. Tests on the maximum trigger rate throughput were performed with different configurations of readout mask and auto-trigger mask. This resulted in a maximum trigger frequency of ~ 5.5 MHz in the best case scenario and ~ 2.1 MHz for the worst case scenario. In September 2022 a first commissioning phase with LHC p-p collisions at 13.6 TeV was performed. This allowed to asses the performance of the readout in real world conditions, in particular regarding the auto-trigger algorithm and the GBT based data transmission. Regarding the link stability, it was observed that

	MODULE 0	MODULE 1	MODULE 2	MODULE 3
ch 0	ZNA_TC(T)	ZNA_TC (OT)	ZNC_TC(T)	ZNC_TC(OT)
ch 1	ZNA_SUM(S)	ZNA_SUM	ZNC_SUM(S)	ZNC_SUM
ch 2	ZNA_T1	ZNA_T3	ZNC_T1	ZNC_T3
ch 3	ZNA_T2	ZNA_T4	ZNC_T2	ZNC_T4
	MODULE 4	MODULE 5	MODULE 6	MODULE 7
ch 0	ZPA_TC(T)	ZPA_TC (OT)	ZPC_TC(T)	ZPC_TC(OT)
ch 1	ZEM1(T)	ZPA_SUM	ZEM2(T)	ZPC_SUM
ch 2	ZPA_T1	ZPA_T3	ZPC_T3	ZPC_T1
ch 3	ZPA_T2	ZPA_T4	ZPC_T4	ZPC_T2

Table 1. [15] Cabling of each IFC1211 module of the upgraded ZDC readout system. T = (Trigger) triggering channel. OT = (Only Trigger) channel used for trigger, but not for readout. S = (Spare) Channel not used for trigger nor for readout.

during the full data taking the links never lost connection and regarding the data throughput it was in line with what was calculated for a 50 KHz hadronic interaction rate at ~ 160 MBps for the full readout. Several tests were performed with different thresholds and readout configurations in order to evaluate the optimal working conditions for p-p and Pb-Pb interactions. Figure 2 shows a single waveform acquired by stimulating a photomultiplier by means of a laser, while waveforms from a single p-p interaction, observed by the ZN side C (ZNC), are reported in figure 3.

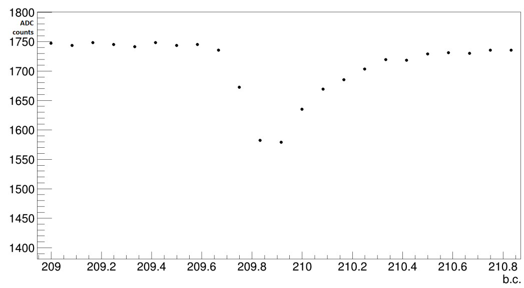

Figure 2. Signal waveform of ZNC_TC stimulated by a laser.

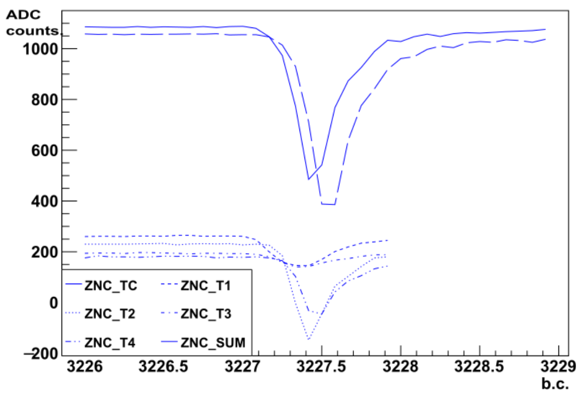

Figure 3. Signal waveforms from ZNC calorimeter during p-p interaction.

In conclusion, from preliminary tests in the laboratory and with beam, it seems that the FMC digitizer with FPGA data processing is working as expected. Further commissioning is scheduled for November 2022 with p-p and Pb-Pb interactions.

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