POLITECNICO DI TORINO
Repository ISTITUZIONALE

NS-GAAFET Compact Modeling: Technological Challenges in Sub-3-nm Circuit Performance

Original
NS-GAAFET Compact Modeling: Technological Challenges in Sub-3-nm Circuit Performance / Mo, F., Spano, C.E., Ardesi, Y., RUO ROCH, M., Piccinini, G., Vacca, M.. - In: ELECTRONICS. - ISSN 2079-9292. - ELETTRONICO. - 12:6(2023), p. 1487. [10.3390/electronics12061487]

Availability:
This version is available at: 11583/2977314 since: 2023-03-22T21:06:00Z

Publisher:
MDPI

Published
DOI:10.3390/electronics12061487

Terms of use:

This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

Publisher copyright

(Article begins on next page)

25 November 2026

electronics

Article

NS-GAAFET Compact Modeling: Technological Challenges in Sub-3-nm Circuit Performance

Fabrizio Mo †, Chiara Elfi Spano †, Yuri Ardesi, Massimo Ruo Roch, Gianluca Piccinini and Marco Vacca *

Department of Electronics and Telecommunication, Politecnico di Torino, 10129 Torino, Italy
* Correspondence: marco.vacca@polito.it
† These authors contributed equally to this work.

Abstract: NanoSheet-Gate-All-Around-FETs (NS-GAAFETs) are commonly recognized as the future technology to push the digital node scaling into the sub-3 nm range. NS-GAAFETs are expected to replace FinFETs in a few years, as they provide highly electrostatic gate control thanks to the GAA structure, with four sides of the NS channel entirely enveloped by the gate. At the same time, the NS rectangular cross-section is demonstrated to be effective in its driving strength thanks to its high saturation current, tunable through the NS width used as a design parameter. In this work, we develop a NS-GAAFET compact model and we use it to link peculiar single-device parameters to digital circuit performance. In particular, we use the well-known BSIM-CMG core solver for multigate transistors as a starting point and develop an *ad hoc*resistive and capacitive network to model the NS-GAAFET geometrical and physical structure. Then, we employ the developed model to design and optimize a digital inverter and a five-stage ring oscillator, which we use as a performance benchmark for the NS-GAAFET technology. Through Cadence Virtuoso SPICE simulations, we investigate the digital NS-GAAFET performance for both high-performance and low-power nodes, according to the average future node present in the International Roadmap for Devices and Systems. We focus our analysis on the main different technological parameters with regard to FinFET, i.e., the inner and outer spacers. Our results highlight that in future technological nodes, the choice of alternative low-K dielectric materials for the NS spacers will assume increasing importance, being as relevant, or even more relevant, than photolithographic alignment and resolution at the sub-nm scale.

Keywords: NS-GAAFET; compact modeling; digital circuits; low-K dielectrics; photolithography; process variations; sub-3-nm nodes

check for updates

Citation: Mo, F.; Spano, C.E.; Ardesi, Y.; Ruo Roch, M.; Piccinini, G.; Vacca, M. NS-GAAFET Compact Modeling: Technological Challenges in Sub-3-nm Circuit Performance. *Electronics* **2023**, *12*, 1487. https://doi.org/10.3390/electronics12061487

Academic Editors: Fotis Plessas, Costas Psychalinos and Pedro Toledo

Received: 28 February 2023
Revised: 17 March 2023
Accepted: 20 March 2023
Published: 21 March 2023

Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

Planar Field-Effect Transistors (FETs) have become obsolete during the last decade, making way for three-dimensional FETs [1]. Fin-shaped FETs (FinFETs) have been developed and successfully commercialized in their multi-gate configuration, pursuing Moore's law while reducing short-channel effects (SCEs) [2–4]. This success allowed FinFET to become the dominant technology until the latest 3-nm node. However, nowadays, FinFET technology is facing many challenges in performance, layout, and cost for further scaling, determining its end in the sub-3-nm technological node [5–8]. Novel TCAD tools, improving the electronics industry toolchain, are currently being developed to investigate cost-effective solutions to still pursue more-than-Moore integration [5]. Nevertheless, power performance appears often as a limiting factor for FinFET-based ICs at ultra-scaled technological nodes, and optimizations in the energy delay product are difficult and still searched for [6]. In addition, FinFET-based IC reliability is an addressed problem at the current level of scaling, and different solutions, such as SOI devices, are considered despite their increased costs [7].

In this scenario, vertically stacked NanoSheet Gate-All-Around FETs (NS-GAAFETs) have been recognized as the most promising candidates to replace FinFETs at a reduced

technology transition cost, since they can be mass-produced using almost the same manufacturing processes and instrumentation [9,10]. Indeed, thanks to their superior electrostatic channel control that minimizes SCEs, larger drive current per layout footprint, low operational voltage and design flexibility, vertically stacked NS-GAAFETs constitute the near-term future of integrated circuits [11]. Furthermore, the increased design flexibility of NSGAAFETs in comparison to FinFETs is proven. Thanks to the fine tuning of the device width and through stacked transistors, NSGAAFETs are good candidates to manage the problematic power–performance optimization [9]. Despite the technological challenges, significant experimental advances show the high competitiveness of NSGAAFETs for future technology nodes. Furthermore, NSGAAFET technology has already been successfully demonstrated with a fully working, high-density SRAM, showing superior performance with regard to the FinFET implementation [10], and demonstrating also that the NSGAAFET technology is close to mass production.

The current literature presents many fabrication processes and device-level studies on NS-GAAFETs [12–15]. In contrast, only a few studies are carried out at the circuital and application levels, mainly due to the lack of compact models essential for digital design. Moreover, and to the best of our knowledge, there still need to be studies dedicated to linking the system-level performance to technological parameters such as photolithographic process variations and spacer dielectric properties.

The important demand for NSGAAFET investigation as a promising near-term future technology for integrated circuits, and the need for its assessment at the circuital and application levels to be linked to the technological parameters of this emerging technology, motivate the present paper. For these purposes, in this work, we adapt the well-established BSIM Common MultiGate (CMG) SPICE model [16] to the case of the vertically stacked NS-GAAFET technology. In particular, while we keep the efficient surface potential solver for the coupled Poisson's equation with Boltzmann's statistics for carriers under the Gradual Channel Approximation, we modify and remap the resistive network and the capacitive network to account for the geometrical differences in the NSGAAFETs with regard to the FinFETs or cylindrical GAAFET currently available in the BSIM CMG model. Furthermore, thanks to our customized compact model, we quantify the impact of device-level parameters and parasitics on the circuital and system-level operating frequency, providing valuable guidelines for future technological considerations and optimizations. In particular, our simulation results show the significant sensitivity of the operating frequency of the analyzed five-stage ring oscillator (RO) on the parasitic capacitances of the inner spacers, demonstrating the more considerable importance of advanced low-k dielectric materials rather than the inner and outer spacers' alignment for future research investments.

The paper is organized as follows. Section 2 explains the modeling of the vertically stacked NS-GAAFET technology. For clarity, additional details and the equations to be modified or additionally included in the BSIM-CMG model are reported in Section 3. In Section 4, we present the methodology and the design and characterization strategies that we adopt. In Section 5, the model is tested in Cadence Virtuoso® and the results are presented and discussed.

2. Model

To accurately describe NS-GAAFETs through a compact model, we adapt the well-established BSIM-CMG SPICE model [16] to the case of NS-GAAFETs. The BSIM-CMG 110.0.0 compact model is a surface-potential-based model in which all the physical quantities, including the terminal currents, are calculated from the surface channel potentials at source (S) and drain (D) terminals. It is organized into two main components: a core model that solves Poisson's equation with Boltzmann's statistics for carriers and exploits the ideal Gradual Channel Approximation (GCA)—a long channel device—and the set of real-device sub-models that account for all non-idealities, such as quantum mechanical models, and all the SCEs and parasitics affecting the performance of real and short-channel devices. Details can be found in [16].

We use the BSIM-CMG Quadruple-Gate-FET (QG-FET) as a starting point, i.e., a gate-all-around structure. Figure 1a–c report the NS-GAAFET structure, together with the variable names in BSIM-CMG and the corresponding quantities in NS-GAAFET. We use some of the existing BSIM-CMG variables to describe the NanoSheet (NS) geometry. In particular, we remap the fin thickness T_{fin} as the NS width $W_{NS} = T_{fin}$, and the fin height H_{fin} as the NS height $H_{NS} = H_{fin}$. We then characterize the NS-GAAFET through the number of NS per stack N_{NS}, the vertical spacing between adjacent NS T_{sp}, the total height of the stack $H_{stack} = N_{NS}[H_{NS} + T_{sp}]$, and its effective width $W_{eff} = N_{NS}[2W_{NS} + 2H_{NS}]$. We also account for the different geometrical structures of NS-GAAFETs with regard to FinFETs in the device's parasitic resistance and capacitive networks, as described in the following.

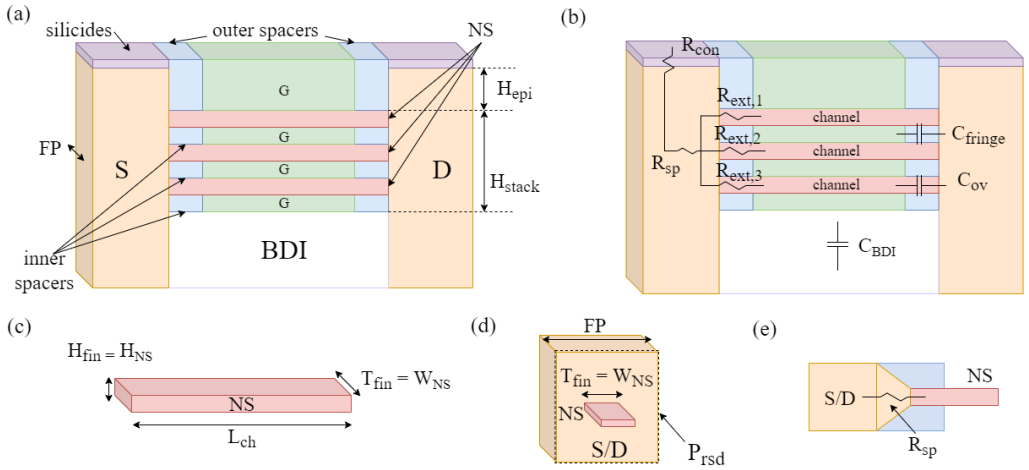


Figure 1. (**a**) NS-GAAFET structure—in green, we show the gate stack. (**b**) Sketch of the parasitic resistance and capacitance contributions. (**c**) NS geometrical parameters and dimensions. (**d**) Fin Pitch (FP) definition. (**e**) Spread resistance R_{sp} geometrical origin.

While many non-ideality effects, such as quantum confinement and tunnelling, velocity saturation, high-mobility fields, or doping degradation, are automatically accounted for in BSIM-CMG for NS-GAAFETs once the model is remapped and modified as described above, the parasitic resistance and capacitance contributions are not. We thus focus on modeling and correcting the existing parasitic resistive and capacitive networks for the case of NS-GAAFETs.

The contact resistance R_{con} and the spreading resistance R_{sp} account for the S/D resistances—including the silicon–silicide interface—and for the S/D resistances due to the current spreading from the S/D thin extension to the large S/D regions (and vice versa)—see Figure 1d. In the case of NS-GAAFETs, the penetration length of the carrier's fluxes into the S/D epitaxial regions depends on the specific NS position with regard to the substrate. It will be the longest for the NS at the bottom of the stack and the shortest for the one at the top. We thus correct the R_{con} and R_{sp} considering in their explicit expressions an average carrier path in the S/D regions—see Equations (1) and (2)—corresponding to half of the total stack height ($H_{stack}/2$). As in FinFETs, also in NS-GAAFETs, extensions are needed to avoid short circuits of the gate with the S/D—see Figure 1a, inner spacers. In the case of stacked NS, we model the total $R_{ext,tot}$ as the parallel of the single NS extension resistances—see Equation (3). Figure 1e summarizes the parasitics resistive network of NS-GAAFETs.

For the capacitive network, we use the most accurate modeling approach in BSIM-CMG, namely the physically based one. The fringe capacitance represents the total capacitive coupling among the gate, extensions, and S/D regions. In NS-GAAFETs, N_{NS} channels are present. The side component is thus modified to account for the effect of the N_{NS} parallel channels—see Equation (4)—while the top and corner fringe capacitance are unchanged in the NS configuration. The S/D-to-gate overlap capacitances are modified to

account for the NS effective width W_{eff} as in Equation (5). Furthermore, in the NS-GAAFET structure, inner spacers are aimed at separating the gate from the S/D regions, avoiding short circuits. Nevertheless, spacers give rise to additional capacitive contributions between the S/D regions and the inter-channel metal gates through the spacers themselves. Thanks to the planar geometry arising from the NS structure, we calculate the additional spacer capacitance through the parallel plate model, and then we sum the single contributions since capacitances are in parallel—see Equation (6). Such contributions are formally included in the fringe capacitive network. Finally, the capacitance contribution toward the substrate through the Bottom Dielectric Insulator (BDI) is unchanged for the NS-GAAFET. The modified capacitances are highlighted in Figure 1e.

Finally, we refer to our modified version of the BSIM-CMG model as BSIM-CMG-NS.

3. Model Equations

In this section, we report the model equations that we modify to account for the differences in NS-GAAFETs with regard to FinFETs.

Contact resistance:
We use the oiginal BSIM-CMG expression for the contact resistance [16]:

$$R_{con} = L_T \cdot \frac{\rho_{S/D}}{A_{rsd}} \cdot \frac{cosh(\alpha_{av}) + \eta\ sinh(\alpha_{av})}{sinh(\alpha_{av}) + \eta\ cosh(\alpha_{av})} \tag{1}$$

where $\rho_{S/D} = \frac{1}{q\ NSD\ \mu}$ is the S/D resistivity, q is the elementary charge, NSD the S/D doping, and μ the mobility. We modify the geometrical factors A_{rsd} and P_{rsd} to account for the different NS-GAAFET geometry—see Figure 1—and we consequently modify L_T, α_{av}, and η:

$$\begin{aligned}
A_{rsd} &= FP \cdot \frac{H_{stack}}{2} + W_{NS} \cdot H_{epi} + C_r \cdot (FP - W_{NS}) \cdot H_{epi} \\
P_{rsd} &= (H_{stack} + 2 \cdot FP) + \left(FP + 2 \cdot \sqrt{H_{epi}^2 + \frac{(FP - W_{NS})^2}{4}} \right) \\
L_T &= \sqrt{\frac{\rho_{con,sili}\ A_{rsd}}{\rho_{S/D}\ P_{rsd}}} \\
\alpha_{av} &= \frac{LRSD}{L_T} \\
\eta &= \frac{\rho_{S/D}\ L_T}{\rho_{con,sili}}
\end{aligned}$$

where $\rho_{con,sili}$ is the contact resistivity at the silicide/silicon interface, P_{rsd} is the transverse perimeter of S/D regions, A_{rsd} is the S/D transverse cross-section area, $LRSD$ is the S/D region longitudinal length, FP is the Fin Pitch, and C_r is the ratio of the S/D epitaxial region corner area filled with silicon to the total corner area.

Spreading resistance:
We modify the spreading resistance expression according to the NS-GAAFET S/D region geometry and extension presence. Only the contribution Θ is unaltered from the BSIM-CMG original model (i.e., we consider the same geometrical dispersion of current density to access the channel from S/D):

$$\begin{aligned}
R_{sp} &= \Theta \cdot \left(\frac{1}{\sqrt{W_{NS} H_{stack}/2}} - \frac{2}{\sqrt{A_{rsd}}} + \frac{\sqrt{W_{NS} H_{stack}/2}}{A_{rsd}} \right) \\
\Theta &= \frac{\rho_{S/D}\ cot(\theta)}{\sqrt{\pi}}
\end{aligned} \tag{2}$$

where θ is the spreading angle at which the current spreads in the raised S/D (usually around 55°).

Extension resistance:
We modify the extension resistance $R_{ext,tot}$ to account for the N_{NS} number of parallel channels:

$$R_{ext,tot} = R_{ext,1}||R_{ext,2}||...||R_{ext,i}||...||R_{ext,N_{NS}} \tag{3}$$

where $R_{ext,i}$ corresponds to the default BSIM-CMG extension resistance [16], which, in NS-GAAFETs, corresponds to the single-NS extension resistance.

Fringe Capacitance:
Thanks to the names given to NS dimensions—see Figure 1b—the only fringe capacitance component to be modified with respect to the original expression present in BSIM-CMG is the side one, which we calculate as follows:

$$\begin{aligned} C_{FR,sidest} &= C_{FR,side} \cdot (N_{NS}\, H_{NS}) \; + \; C_{cg1,side} \cdot H_{stack} + \\ &+ \; C_{cg2,side} \cdot H_{stack} \end{aligned} \tag{4}$$

where $C_{FR,side}$, $C_{cg1,side}$, and $C_{cg2,side}$ are left unchanged as defined in BSIM-CMG [16].

Overlap capacitance:
Once the effective width is redefined for the NS geometry, the overlap capacitance is automatically updated to the correct value. They are still evaluated as the numerical derivatives with respect to V_{GS} and V_{DS} of the charge due to the lateral diffusion of dopants, as in the original BSIM-CMG model [16]:

$$\begin{aligned} &Q_{gs,ovst}(W_{eff}) \;\; , \;\; Q_{gd,ovst}(W_{eff}) \\ &with: \quad W_{eff} = N_{NS}[2W_{NS} + 2H_{NS}] \\ &overlap \;\; capacitances \;\; \longleftrightarrow \;\; \frac{\partial Q_{gs,ovst}}{\partial V_{GS}} \;\; , \;\; \frac{\partial Q_{gd,ovst}}{\partial V_{DS}} \end{aligned} \tag{5}$$

Inner spacer capacitance:
We calculate the additional inner spacer capacitances (not present in BSIM-CMG) at one S/D side as

$$\begin{aligned} C_{inner,sp} &= \frac{\epsilon_{inn,sp}}{L_{inn,sp}} \cdot T_{sp} \cdot FP + \frac{\epsilon_{inn,sp}}{L_{inn,sp}} \cdot H_{NS} \cdot (FP - W_{NS}) \\ C_{inner,sp,TOT} &= N_{NS} \cdot C_{inner,sp} \end{aligned} \tag{6}$$

where $\epsilon_{inn,sp}$ is the dielectric constant of the inner spacer material, $L_{inn,sp}$ is the inner spacer length (longitudinal to transport direction), and T_{sp} is the inner spacer height (spacing between adjacent NS).

4. Methodology, Figures of Merit, and Characterization

We use the developed model to understand how the device parameters affect the system-level performance in sub-3-nm nodes. Thus, we resolve to link the digital circuit performance to technological and device-level parameters. For the sake of generality and to understand the eventual differences, we address both high-performance (HP) processes and low-power (LP) processes [11]. The latter also corresponds to memory applications [11]. We choose the typical geometrical and physical parameters from the average ones reported in [11], for generic sub-3-nm nodes. Table 1 reports our choices. The only difference between HP and LP devices is the NS width W_{sh}, which corresponds to different driving currents. The quantities t_{OX} and ϵ_{OX} are the thickness and the relative dielectric constant of the gate oxide, whereas $\epsilon_{inn,sp}$ and $\epsilon_{out,sp}$ are the relative dielectric constant of the inner and outer spacer materials, and N_{body}, N_{SD}, N_{SDE} are the typical doping values for the channel,

S/D regions, and S/D extensions, respectively. According to [11], we consider a supply voltage V_{DD} = 0.7 V. In addition, we consider various low-K materials to be used as spacer dielectrics. In particular, we consider values of $\epsilon_{inn,sp}$ and $\epsilon_{out,sp}$ of the most promising low-K materials for electronic devices, also considering their mechanical properties, according to [17–19]. The considered values are reported in Table 2 with the corresponding low-K materials.

Table 1. Geometrical and physical parameters for the simulated n-type NS-GAAFET.

N_{NS}	3	t_{OX}	3.2 nm
W_{NS}	20 nm (HP); 30 nm (LP/Memory)	ϵ_{OX}	25
H_{NS}	7 nm	$\epsilon_{inn,sp}$	3.9
L_{ch}	14 nm	$\epsilon_{out,sp}$	3.9
FP	49 nm	N_{body}	10^{17} cm^{-3}
H_{epi}	10 nm	N_{SD}	10^{21} cm^{-3}
T_{sp}	10 nm	N_{SDE}	10^{19} cm^{-3}

Table 2. Low-K materials considered in this work.

Material	**Relative Dielectric Constant**
vacuum (air)	1
porous SiO_2 and/or polymeric materials	2
carbon-doped oxide	2.8
SiO_2	3.9
SiOCN	5.2
Si_3N_4	7.5

We investigate the impact of technological parameters on digital circuits' performance in Cadence Virtuoso. First, we use the developed VerilogA model BSIM-CMG-NS to simulate and optimize the n-NS-GAAFET device in Cadence Virtuoso—refer to Section 5.1. Then, we design the p-NS-GAAFET to have a symmetric transcharacteristic with respect to the n-type device, and we design and optimize the digital inverter—see Section 5.2. To address the performance study, we exploit the de facto standard ring oscillator (RO) with five stages (five cascaded inverters) [20,21]. Then, to link the digital circuit performance and device-level parameters, we calculate and extract the RO oscillating frequency sensitivity to device technological parameters—see Section 5.3. Finally, we simulate and measure the oscillating frequency in Cadence Virtuoso for different technological parameters. In particular, we investigate the inner and outer spacer dielectric constants and length and the NS spacing since they are not present in conventional FinFETs and significant outcomes may arise from this analysis. In order to identify which parameter more strongly influences the RO oscillating frequency and digital circuit performance, we vary one parameter at a time while the others are fixed to the nominal values in Table 1. To generalize the obtained results, we repeat the previous steps for the 30 nm (HP) n-NS-GAAFET and for the 20 nm (LP) one and compare the results.

We characterize the considered devices through the following Figures of Merit (FoM):

- Drain-Induced Barrier Lowering (DIBL): We calculate this from its definition as

$$DIBL = -\frac{V_{TH}|_{V_{DD}} - V_{TH}|_{V_{low}}}{V_{DD} - V_{low}} \quad (7)$$

where V_{DD} is the supply voltage, V_{low} is a low voltage value that we fix to 50 mV, and $V_{TH}|_{V_i}$ is the obtained threshold voltage with the voltage V_i, where $V_i = V_{DD}, V_{low}$. We calculate V_{TH} through the second-order derivative of the transcharacteristic, i.e., the maximum transconductance method [22,23].

- Subthreshold Slope (SS): This is defined as

$$SS = \left[\frac{\partial log_{10}(I_{DS})}{\partial V_{GS}}\right]^{-1} \tag{8}$$

For simplicity, we calulate it as $SS = [\Delta log_{10}(I_{DS})/\Delta V_{GS}]^{-1}$, where Δ indicates an interval (i.e., a difference), and considering an I_{DS} excursion $\Delta log_{10}(I_{DS})$ of one decade.

- I_{ON}: Driving ON current, obtained with $V_{DS} = V_{GS} = V_{DD}$;
- I_{OFF}: subthreshold leakage OFF current, obtained with $V_{DS} = V_{DD}$ and V_{GS} = 0 V;
- I_{ON}/I_{OFF} ratio.

We characterize our design through the sensitivity to technological parameters. We calculate the sensitivity S and the percentage sensitivity $S_{\%}$ of the quantity Q with regard to the parameter p as

$$S = \frac{\partial Q}{\partial p} \approx \frac{\Delta Q}{\Delta p} \ , \ S_{\%} = \frac{\partial Q}{\partial p} \cdot \frac{\overline{p}}{\overline{Q}} \cdot 100 \approx \frac{\Delta Q}{\Delta p} \cdot \frac{\overline{p}}{\overline{Q}} \cdot 100, \tag{9}$$

where the operator ∂ represents the partial derivative, Δ is the difference operator, and $\overline{p}$ and $\overline{Q}$ are the nominal parameter value and nominal quantity value, respectively.

5. Design, Simulations, and Results

5.1. n-Type NS-GAAFET

Figure 2 shows the simulated transcharacteristics $I_{DS}(V_{GS})$ in a semi-logarithmic scale as a function of the NS width W_{NS}. The inset of Figure 2 shows the I_{ON}/I_{OFF} ratio by varying W_{sh}. Table 3 reports the extracted FoM for the curves in Figure 2.

An abrupt performance variation occurs when passing from W_{sh} = 20 nm to W_{sh} 30 nm. The corresponding transcharacteristics in Figure 2 are more spaced than the ones corresponding to 40 and 50 nm, and the I_{ON}/I_{OFF} deterioration is more marked with regard to a successive W_{sh} increase. The same trend is present in Table 3. A significant DIBL deterioration occurs when W_{sh} is increased from 20 nm to 30 nm. For successive increases, the DIBL presents less worsening. The same applies to I_{ON}/I_{OFF}—as mentioned above—which decreases by one order of magnitude from 20 to 30 nm of W_{sh}, while a minor deterioration is present for a successive increase in W_{sh}. In contrast, SS is the only FoM presenting a linear deterioration passing gradually from W_{sh} = 20 nm to W_{sh} = 50 nm. The I_{ON} is almost doubled passing from W_{sh} = 20 nm to W_{sh} = 30 nm, whereas, for a successive increase in W_{sh}, it increases.

For an HP node, the I_{ON} with W_{sh} = 20 nm is too low, so an n-NS-GAAFET width of 30 nm is the optimal compromise between a high driving current I_{ON} and good device performance in terms of DIBL, SS, I_{ON}/I_{OFF}. This agrees with the device design guidelines in [11]. For an LP node, W_{sh} = 20 nm is a good compromise between low I_{OFF} leakages and optimal device FoM in terms of DIBL, SS, I_{ON}/I_{OFF}.

Furthermore, our results match the literature's theoretical and experimental results for the different target applications [5,10,12,14]. Thus, we consider the developed model reliable since it correctly predicts the experimental results in [5,10,12]

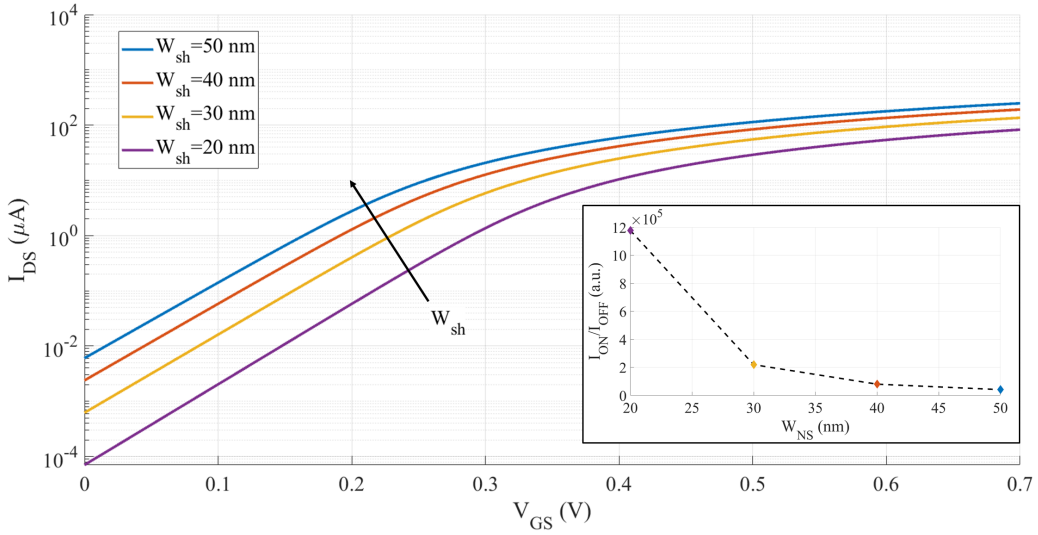


Figure 2. Parametric n-NS-GAAFET transcharacteristics $I_{DS}(V_{GS})$ in semi-logarithmic scale with different nanosheet width W_{sh} values; the inset shows the corresponding I_{ON}/I_{OFF} ratios.

Table 3. Calculated FoM for each considered NS width W_{sh}.

W_{sh} (nm)	20	30	40	50
DIBL (mV/V)	12.3	30.8	43.1	52.3
SS (mV/dec)	67	69	72	73
I_{ON}/I_{OFF} (a.u.)	$1.18 \cdot 10^6$	$2.19 \cdot 10^5$	$8.02 \cdot 10^4$	$4.12 \cdot 10^4$
I_{ON} (µA)	87	148	202.5	263

5.2. Digital Inverter

We design the logic inverter by finding the width W_p of the p-type NS-GAAFET that leads to the most symmetric inverter transcharacteristic. We start from $W_p = W_n$, where W_n is W_{NS} for the n-type device, as discussed previously. Then, we decrease W_p until the optimum is found, which corresponds to fully symmetric n-type and p-type transcharacteristics.

Notice that we decrease W_p with regard to W_n since we suppose the silicon NS growth direction to be [110] and thus to obtain the largest faces of the NS with hole mobility greater than electron one and smallest faces with hole mobility lower than electron one, leading to a total effective hole mobility larger than electron one. This choice is also typical in FinFETs, due to typical technological situations. In general, the choice to have the NS growth direction parallel to [100] is also possible, leading to electron mobility larger than hole one and therefore a $W_p > W_n$. These features can be selected through a flag in the original BSIM-CMG model [16] and also in the proposed BSIM-CMG-NS one.

5.2.1. HP Node

For the HP process, we find the optimum W_p to be 22 nm. The inverter transcharacteristics obtained by varying W_p are reported in Figure 3, and the inset shows an enlargement of the dashed box region. We find the most symmetric inverter transcharacteristic for a p-type width W_p = 22 nm, and thus we choose it to implement the inverter logic gate. A ratio $\beta_p = W_p/W_n$ = 0.767 is thus assumed. The relative n-type and p-type NS-GAAFET single device transcharacteristics with W_n = 30 nm and W_p = 22 nm are reported in Figure 4 in logarithmic scale. Good symmetry is present for the chosen transistor widths. The inset

of Figure 4 shows the same transcharacteristics in linear scale, highlighting a good match also for ON currents, with n-type $I_{ON,n}$ = 148 µA and p-type $I_{ON,p}$ = 147.4 µA.

Notice that the effective drive current of the inverter [24], calculated with the three-point method [25], for the HP node is I_{eff} = 28.7 µA.

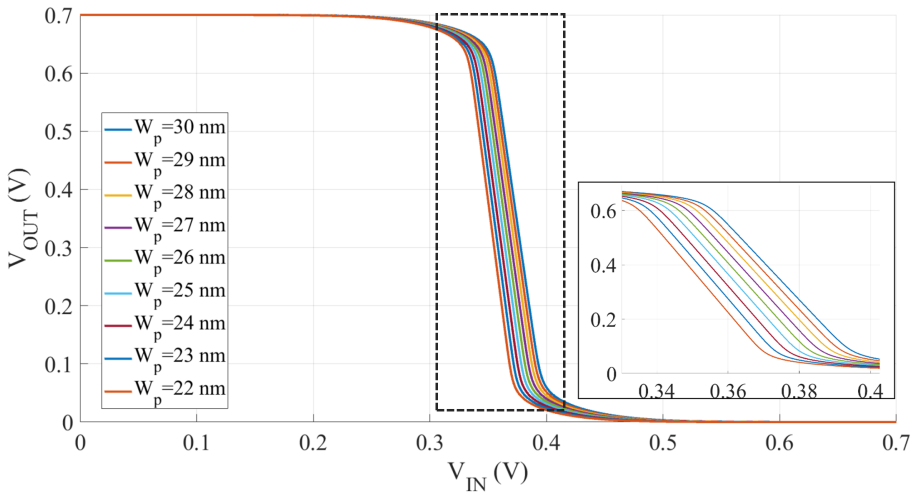


Figure 3. Parametric inverter transcharacteristics V_{OUT}/V_{IN} with different p-type nanosheet width W_p and with W_n = 30 nm; the inset shows an enlargement of the dashed box portion.

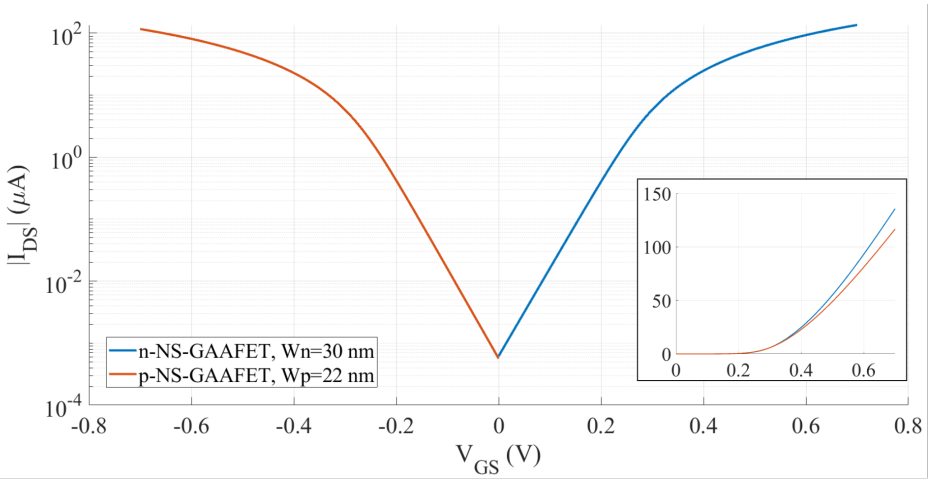


Figure 4. Optimized NS-GAAFET transcharacteristics $I_{DS}(V_{GS})$: n-type (W_n = 30 nm)—blue curves; p-type (W_p= 22 nm)—orange curves; the inset highlights the same NS-GAAFET transcharacteristics $I_{DS}(V_{GS})$ in linear scale.

5.2.2. LP Node

We repeat the same for the LP process and we find an optimum W_p of 14 nm. The inverter transcharacteristics obtained by varying W_p are reported in Figure 5; the inset shows an enlargement of the dashed box region. The ratio $\beta_p = W_p/W_n$ is 0.7. The relative n-type and p-type NS-GAAFET transcharacteristics with W_n = 20 nm and W_p = 14 nm are reported in Figure 6 in logarithmic scale. Again, good symmetry is present for the chosen transistor widths.

The effective drive current of the inverter [24], calculated with the three-point method [25], for the LP node is I_{eff} = 17.1 µA.

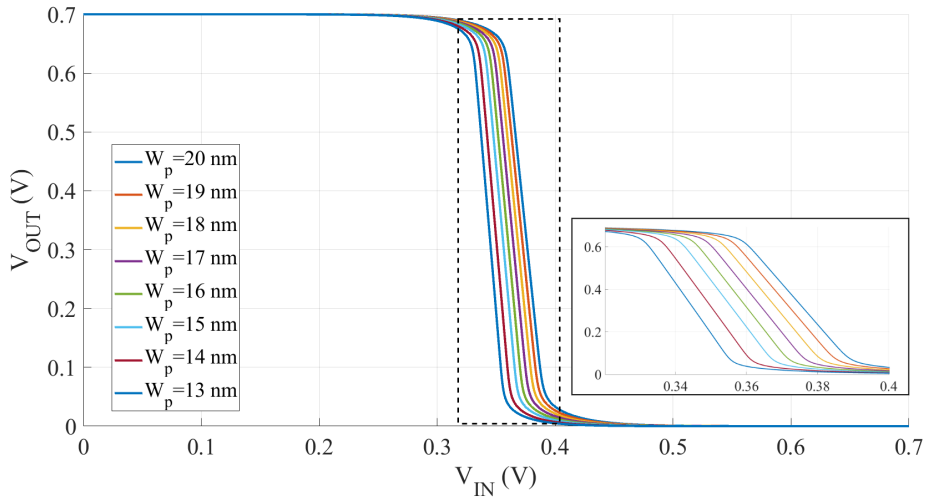


Figure 5. Parametric inverter transcharacteristics V_{OUT}/V_{IN} with different p-type nanosheet width W_p and with W_n = 20 nm; the inset shows an enlargement of the dashed box portion.

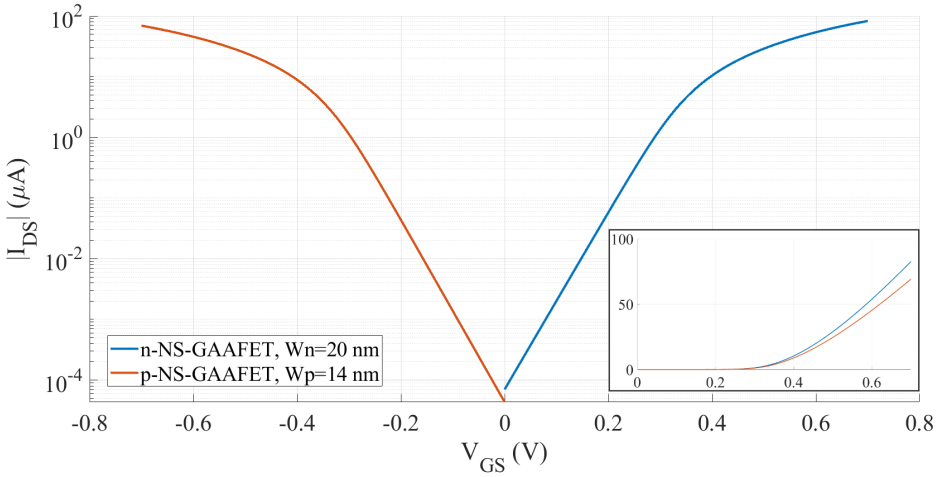


Figure 6. Optimized NS-GAAFET transcharacteristics $I_{DS}(V_{GS})$: n-type (W_n = 20 nm)—blue curves; p-type (W_p = 14 nm)—orange curves; the inset highlights the same curves in linear scale.

5.3. Five-Stage Ring Oscillator

We use the designed digital inverter to implement a five-stage RO—i.e., 5 cascaded inverters—and then we use the RO to extract the digital circuit performance, according to what commonly is done in the literature [20,21].

5.3.1. LP Node (W_n = 20 nm)

Figure 7a reports the RO oscillating frequency f_{osc} as a function of both $\epsilon_{inn,sp}$ and $\epsilon_{out,sp}$. We consider the (relative) dielectric constants in Table 2. An increase in the spacer dielectric constant leads to an increase in inner and outer spacer capacitance. Therefore, a frequency reduction occurs. There is no compromise with other NS-GAAFET parameters and the only upper limit to f_{osc} is dictated by the lowest possible dielectric constant, theoretically equal to 1 vacuum. Nevertheless, the structural and mechanical properties make it difficult to build suspended NS, and dielectric materials are used to guarantee structural stability and prevent the gate and S/D short circuits.

Figure 7b reports the RO oscillating frequency f_{osc} as a function of both $L_{inn,sp}$ and $L_{out,sp}$. The blue curve is related to a variation in both $L_{inn,sp}$ and $L_{out,sp}$, which are assumed to be equal. This case represents different photolithographic processes with different spacing between the channels and the S/D regions. The orange curve is related to a variation in $L_{inn,sp}$ when the $L_{out,sp}$ is fixed. This case may happen due to photolithographic

process variations and NS misalignment. A longitudinal trapezoidal device cross-section would appear in case of misalignment, as experimentally verified in some cases [5,10,12]. A larger f_{osc} excursion is present when both $L_{inn,sp}$ and $L_{out,sp}$ are varied. Nevertheless, a significant f_{osc} excursion is also present in the case of misalignment. In particular, being the spacer capacitance inversely proportional to the S/D and channel spacing, i.e., to $L_{inn,sp}$ and $L_{out,sp}$, the longer are the inner/outer spacers, the lower are the relative capacitances and the higher is f_{osc}. For the considered generic sub-3-nm node, the nominal $L_{inn,sp}$ and $L_{out,sp}$ value is 6 nm, for which the blue and orange curves are overlapped. Although the longer the spacers are, the better the performance is, a trade-off is present with the channel access resistances that are inversely proportional to the spacer length, corresponding also to the NS portion between the S/D and the region underneath the gate. Longer spacers and NS access regions decrease the ON current and increase the OFF leakage since the portion of the NS that is not under gate control is lengthened.

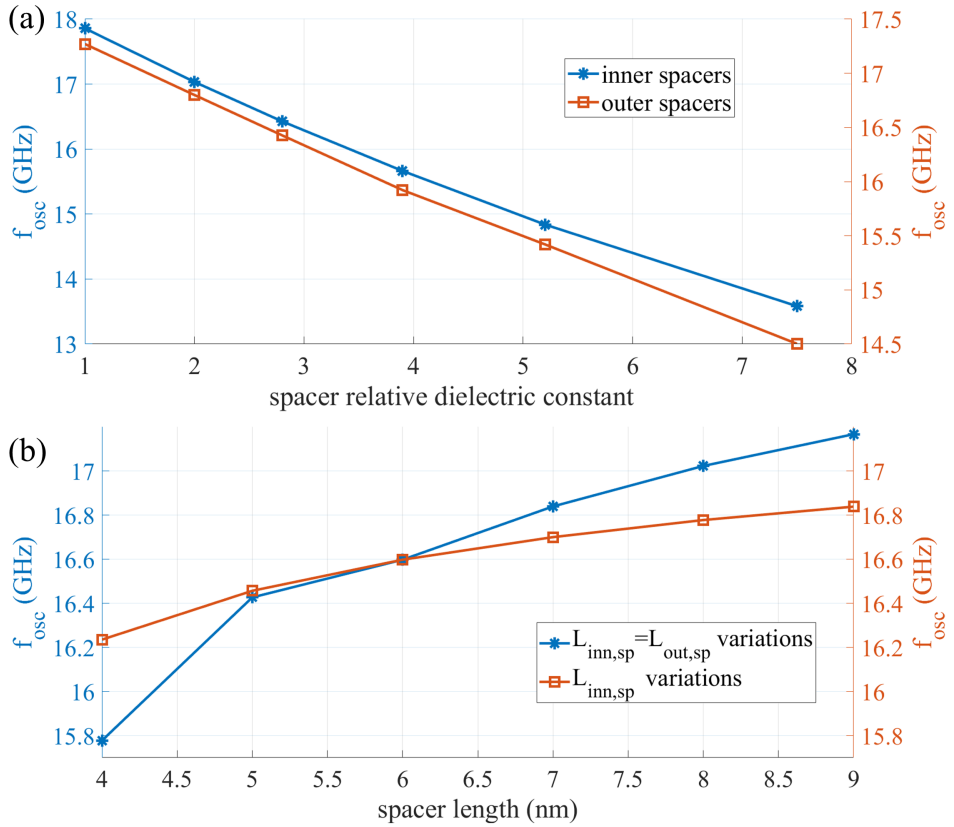


Figure 7. (**a**) Five-stage RO oscillation frequency as function of the inner and outer spacer material dielectric constants—when a dielectric constant is changed, the other is fixed at 3.9. (**b**) Five-stage RO oscillation frequency as function of the inner and outer spacer lengths.

5.3.2. HP Node and Comparison with LP Node

We repeat the RO design and f_{osc} extraction for the HP node (W_n = 30 nm). Similar trends and considerations hold for the HP node case when f_{osc} is considered for $\epsilon_{inn,sp}$, $\epsilon_{out,sp}$, $L_{inn,sp}$, and $L_{out,sp}$ variations. Then, we calculate the f_{osc} sensitivity to $\epsilon_{inn,sp}$, $\epsilon_{out,sp}$, $L_{inn,sp}$, $L_{out,sp}$, and also to T_{sp} (i.e., the vertical NS spacing)—see Equation (9). To understand when f_{osc} variations become significant, we compare the obtained sensitivities, with HP and LP nodes, in Table 4.

Interestingly, the f_{osc} sensitivity to all considered parameters but T_{sp} is greater for the LP node than for the HP node. For T_{sp}, the two sensitivities are comparable, with the HP one greater than the LP one. We suppose that the larger W_{NS} in the HP node mitigates and reduces the f_{osc} sensitivity to $\epsilon_{inn,sp}$, $\epsilon_{out,sp}$, $L_{inn,sp}$, and $L_{out,sp}$. Indeed, the difference

between HP and LP sensitivity is marked for $L_{inn,sp}$, meaning that a geometrical factor is the main cause of the sensitivity differences.

Furthermore, considering that power dissipation is the driving force toward the next technological node design, and considering that the future scaling of digital nodes is approaching the LP/memory nodes, we expect the future technological nodes to resemble the average LP one considered in this work more than the HP one. Thus, Table 4 shows that process control at the nano-scale strongly impacts the expected digital circuit performance, with a 10 to 20% performance variation possible due to different fabrication strategies or process variations. Again, the f_{osc} sensitivity to the spacer dielectric constant is comparable or even greater than the one to the spacer length and alignment. Therefore, in future technological nodes, to address performance deterioration, the choice of alternative low-K materials to conventional SiO_2 or Si_3N_4 might become more important than controlling the photolithographic patterning at the sub-nm scale.

Table 4. Calculated percentage sensitivity values for oscillating frequency.

	$\epsilon_{inn,sp}$	$\epsilon_{out,sp}$	$L_{inn,sp} = L_{out,sp}$	$L_{inn,sp}$	T_{sp}
20 nm	19.9%	24.8%	20.22%	10.51%	2.44%
30 nm	11.39%	13.34%	14.89%	5.31%	3.83%

6. Conclusions

We adapted the well-established BSIM-CMG model for the NS-GAAFETs case by developing an ad hoc NS-GAAFET SPICE compact model. In particular, we preserved the efficient core solver of the BSIM-CMG compact model, and, by considering the different vertically stacked, rectangular section NS-GAAFET structure with respect to the FinFET one, we modified the resistive and capacitive networks of the model to account for the differences. Then, we employed the developed compact model to design the basic logic gate, i.e., the digital inverter, and to implement a five-stage RO to test the digital performance of the future sub-3-nm nodes in a standard framework. We focused our attention on the NS spacers, which are not present in conventional FinFETs, to understand their impact on digital circuit performance and to understand whether different design and fabrication strategies should be adopted in the near future.

Our results show that the spacer dielectric material choice is increasingly crucial for future digital nodes. The performance sensitivity to low-K dielectric materials is comparable to (HP nodes) or even greater (LP/memory nodes) than the performance sensitivity to photolithographic alignment and resolution at the sub-nm scale.

Our results motivate future research efforts and investments in alternative dielectric materials, rather than overcoming the photolithography approach's intrinsic limits.

Author Contributions: Conceptualization, F.M., C.E.S., Y.A., M.V. and G.P.; methodology, F.M., C.E.S., Y.A., M.V. and G.P.; software, F.M. and C.E.S.; validation, F.M. and C.E.S.; formal analysis, F.M. and C.E.S.; investigation, F.M., C.E.S., Y.A., M.V. and G.P.; resources, M.R.R.; data curation, F.M. and C.E.S.; writing—original draft preparation, F.M. and C.E.S.; writing—review and editing, Y.A., M.V. and G.P.; visualization, F.M. and C.E.S.; supervision, Y.A., M.V. and G.P; project administration, M.R.R. and G.P.; internal funding acquisition, M.R.R. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Taur, Y.; Ning, T.H. *Fundamentals of Modern VLSI Devices*, 3 ed.; Cambridge University Press: Cambridge, UK, 2021. https://doi.org/10.1017/9781108847087.
2. Colinge, J. *FinFETs and Other Multi-Gate Transistors*, 1 ed.; Springer: New York, NY, USA, 2007. https://doi.org/10.1007/978-0-387-71752-4.
3. Saha, S. *FinFET Devices for VLSI Circuits and Systems*, 1 ed.; CRC Press: Boca Raton, FL, USA, 2020. https://doi.org/10.1201/9780429504839.
4. Vacca, M.; Turvani, G.; Riente, F.; Graziano, M.; Demarchi, D.; Piccinini, G. TAMTAMS: An open tool to understand nanoelectronics. In Proceedings of the 2012 12th IEEE International Conference on Nanotechnology (IEEE-NANO), Birmingham, UK, 20–23 August 2012; pp. 1–5. https://doi.org/10.1109/NANO.2012.6322086.
5. Kwon, U.; Park, Y.; Kim, Y.S.; Yoo, J.; Kim, D.S. TCAD challenges and opportunities to find a feasible device architecture for sub-3 nm scaling. In Proceedings of the 2021 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Dallas, TX, USA, 27–29 September 2021; pp. 5–10. https://doi.org/10.1109/SISPAD54002.2021.9592554.
6. Yoon, J.S.; Jeong, J.; Lee, S.; Lee, J.; Lee, S.; Baek, R.H.; Lim, S.K. Performance, Power, and Area of Standard Cells in Sub 3 nm Node Using Buried Power Rail. *IEEE Trans. Electron Devices* **2022**, *69*, 894–899. https://doi.org/10.1109/TED.2021.3138865.
7. Linten, D.; Hellings, G.; Chen, S.H.; Groeseneken, G. ESD in FinFET technologies: Past learning and emerging challenges. In Proceedings of the 2013 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 14–18 April 2013; pp. 2B.5.1–2B.5.8. https://doi.org/10.1109/IRPS.2013.6531950.
8. Riente, F.; Hussain, I.; Ruo Roch, M.; Vacca, M. Understanding CMOS Technology Through TAMTAMS Web. *IEEE Trans. Emerg. Top. Comput.* **2016**, *4*, 392–403. https://doi.org/10.1109/TETC.2015.2488899.
9. Barraud, S.; Lapras, V.; Previtali, B.; Samson, M.P.; Lacord, J.; Martinie, S.; Jaud, M.A.; Athanasiou, S.; Triozon, F.; Rozeau, O.; et al. Performance and design considerations for gate-all-around stacked-NanoWires FETs. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017; pp. 29.2.1–29.2.4. https://doi.org/10.1109/IEDM.2017.8268473.
10. Bae, G.; Bae, D.I.; Kang, M.; Hwang, S.; Kim, S.; Seo, B.; Kwon, T.; Lee, T.; Moon, C.; Choi, Y.; et al. 3nm GAA Technology featuring Multi-Bridge-Channel FET for Low Power and High Performance Applications. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018; pp. 28.7.1–28.7.4. https://doi.org/10.1109/IEDM.2018.8614629.
11. IEEE International Roadmap for Devices and Systems, 2021 Edition — Executive Report. Available online: https://irds.ieee.org/ (accessed on 28 January 2023).
12. Zhang, J.; Frougier, J.; Greene, A.; Miao, X.; Yu, L.; Vega, R.; Montanini, P.; Durfee, C.; Gaul, A.; Pancharatnam, S.; et al. Full Bottom Dielectric Isolation to Enable Stacked Nanosheet Transistor for Low Power and High Performance Applications. In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019; pp. 11.6.1–11.6.4. https://doi.org/10.1109/IEDM19573.2019.8993490.
13. Li, J.; Li, Y.; Zhou, N.; Xiong, W.; Wang, G.; Zhang, Q.; Du, A.; Gao, J.; Kong, Z.; Lin, H.; et al. Study of Silicon Nitride Inner Spacer Formation in Process of Gate-all-around Nano-Transistors. *Nanomaterials* **2020**, *10*, 793. https://doi.org/10.3390/nano10040793.
14. Shen, T.; Watanabe, K.; Zhou, H.; Belyansky, M.; Stuckert, E.; Zhang, J.; Greene, A.; Basker, V.; Wang, M. A new technique for evaluating stacked nanosheet inner spacer TDDB reliability. In Proceedings of the 2020 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 28 April–30 May 2020; pp. 1–5. https://doi.org/10.1109/IRPS45951.2020.9129258.
15. Yakimets, D.; Bardon, M.G.; Jang, D.; Schuddinck, P.; Sherazi, Y.; Weckx, P.; Miyaguchi, K.; Parvais, B.; Raghavan, P.; Spessot, A.; et al. Power aware FinFET and lateral nanosheet FET targeting for 3nm CMOS technology. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017; pp. 20.4.1–20.4.4. https://doi.org/10.1109/IEDM.2017.8268429.
16. Paydavosi, N.; Venugopalan, S.; Chauhan, Y.S.; Duarte, J.P.; Jandhyala, S.; Niknejad, A.M.; Hu, C.C. BSIM—SPICE Models Enable FinFET and UTB IC Designs. *IEEE Access* **2013**, *1*, 201–215. https://doi.org/10.1109/ACCESS.2013.2260816.
17. Volksen, W.; Miller, R.D.; Dubois, G. Low Dielectric Constant Materials. *Chem. Rev.* **2010**, *110*, 56–110. https://doi.org/10.1021/cr9002819.
18. Gu, M.; Wang, X.; Li, W.; Aquilino, M.; Peng, J.; Wang, H.; Jaeger, D.; Tabakman, K.; Carter, R.; Hu, O.; et al. Hybrid low-k spacer scheme for advanced FinFET technology parasitic capacitance reduction. *Electron. Lett.* **2020**, *56*, 514–516. https://doi.org/https://doi.org/10.1049/el.2019.3954.
19. Wang, Y.; Kumar, R. Stability of Carbon-Doped Silicon Oxide Low-k Thin Films. *J. Electrochem. Soc.* **2004**, *151*, F73. https://doi.org/10.1149/1.1648026.
20. Rabaey, J.; Chandrakasan, A.; Nikolic, B. *Digital Integrated Circuits: A Design Perspective. Electronics and VLSI Series*, 2nd ed.; Pearson Education: London, UK, 24 December 2002.
21. Ribas, R.P.; Reis, A.I.; Ivanov, A. Performance and functional test of flip-flops using ring oscillator structure. In Proceedings of the 2011 IEEE 6th International Design and Test Workshop (IDT), Beirut, Lebanon, 11–14 December 2011; pp. 42–47. https://doi.org/10.1109/IDT.2011.6123099.
22. Ortiz-Conde, A.; García Sánchez, F.; Liou, J.; Cerdeira, A.; Estrada, M.; Yue, Y. A review of recent MOSFET threshold voltage extraction methods. *Microelectron. Reliab.* **2002**, *42*, 583–596. https://doi.org/https://doi.org/10.1016/S0026-2714(02)00027-6.

23. Rudenko, T.; Kilchytska, V.; Md A, M.K.; Raskin, J.P.; Nazarov, A.; Flandre, D. On the MOSFET Threshold Voltage Extraction by Transconductance and Transconductance-to-Current Ratio Change Methods: Part II—Effect of Drain Voltage. *IEEE Trans. Electron Devices* **2012**, *58*, 4180–4188. https://doi.org/10.1109/TED.2011.2168227.
24. Na, M.; Nowak, E.; Haensch, W.; Cai, J. The effective drive current in CMOS inverters. In Proceedings of the Digest. International Electron Devices Meeting, San Francisco, CA, USA, 8–11 December 2002; pp. 121–124. https://doi.org/10.1109/IEDM.2002.1175793.
25. Hu, J.; Park, J.E.; Freeman, G.; Wachnik, R.; Wong, H.S.P. Effective Drive Current in CMOS Inverters for Sub-45nm Technologies. In Proceedings of the NSTI-Nanotech, Boston, MA, USA, 1–5 June 2008; Volume 3.

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.