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RESEARCH ARTICLE

Limit-Cycle Free, Digitally-Controlled Boost Converter Based on DDPWM

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ABSTRACT In this paper, a digitally controlled boost DC-DC power converter featuring a high-resolution Dyadic Digital Pulse Width Modulator (DDPWM) is proposed to achieve Limit-Cycle oscillations (LCOs)-free operation, high DC accuracy, low output voltage ripple at high switching frequency. The effectiveness of the DDPWM in suppressing the onset of LCOs, increasing DC accuracy, and reducing output ripple is verified by both Simulink/Modelsim co-simulations and experimental testing on a 7-10 V input, 13.8 V output boost converter operated at 1.17 MHz switching frequency. Thanks to the proposed modulator, improvement of more than 6X DC accuracy is achieved compared to a plain digital PWM. Moreover, approximately 3X less output ripple in comparison to a digital PWM with thermometric dithering is achieved.

INDEX TERMS Digital pulse width modulator (DPWM), dyadic digital pulse width modulation (DDPWM), digitally controlled boost converter, HDL verilog, limit-cycles oscillations (LCOs), simulink/modelsim co-simulation, switch-mode power converters.

I. INTRODUCTION

Digital controllers are more and more prevailing over their analog counterpart in present-day switching-mode power converters due to their intrinsic flexibility, reliability, good performance at low cost and reduced susceptibility to aging [1], [2], [3], [4]

Despite many unquestionable advantages, digitally controlled power converters suffer of specific issues, which includes the onset of low-frequency steady state limit-cycle oscillations (LCOs) due to the inherent quantization effect of the analog-to-digital converter (ADC) and of the digital-pulse-width-modulator (DPWM) [5], [6]. Since LCOs impair the output voltage regulation, increase power losses and output ripple, suppressing LCOs in digitally controlled power converters is of primary importance.

To remove LCOs, the DPWM resolution should be higher than the ADC resolution [7], [8], [9], [10] but this results in increased cost and complexity of the DPWM modulators, especially for converters operating at high switching frequency (MHz range) which takes advantage of emerging semiconductor technology (GaN, SiC power transistors [11]). The design of high switching frequency, limit-cycle-free, high-DC-accuracy converters, in particular, needs a very high DPWM counter clock frequency (usually in GHz range) which is impractical in most cases. Alternatively, the ADC resolution should be reduced to suppress LCOs, resulting in a limited DC accuracy.

Aiming to address this problem, high-resolution DPWM based on the Sigma-Delta (Σ-Δ) modulation [12], on delay-lines with sub-cycle unit delay [13], multiphase PWM [14], [15] and hybrid architectures [16] have been implemented in hardware. Most of the solutions proposed so far, however, have resulted in an increased cost and complexity [9], [17], [18].

On the other hand, dithering techniques have been proposed (e.g., the digital thermometric dithering (DTD) modulation [19]), which consist in periodically varying the DPWM duty cycle by 1 least-significant bit (LSB) over a pre-defined pattern, so that to vary the average duty-cycle with a sub-LSB resolution without increasing the DPWM clock frequency, [19]. Although digital dithering is easy to implement and highly controllable, it may introduce a large ripple in the output voltage [8], [9].

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In order to mitigate the disadvantages of dithered DPWM, the dyadic digital PWM (DDPWM) has been recently proposed [20], [21] aiming to increase the DPWM resolution at negligible cost and design effort and without any significant degradation of the output ripple. More recently, DDPWM has been experimentally validated by implementing it on field-programmable gate array (FPGA) and proven as an effective technique to increase the resolution of the DPWM for LCO-free operation in a DC-DC buck converter [8], [9].

While the buck converter exhibits a constant change in output voltage quantization steps with respect to duty-cycle [13], a boost converter exhibits a non-linear change in output voltage quantization steps with respect to the duty-cycle, i.e., it shows finer quantization steps at lower duty-cycle values and coarser steps as the duty-cycle increases [13]. For that reason, meeting the DPWM resolution requirement over a wide range of duty-cycles is particularly challenging.

In this paper, the DDPWM modulation is adopted in a voltage-mode, digitally controlled boost converter for the first time. The boost converter is designed to operate in continuous-conduction mode (CCM) at a switching frequency of 1.17 MHz. The input voltage ranges from 7 to 10 V while the output voltage is fixed at 13.8 V. The effectiveness of the DDPWM in suppressing the onset of LCOs, increasing DC accuracy, and reducing output ripple is verified by both Simulink/Modelsim co-simulations and experimental testing.

This paper is organized as follows. In Sect. II, a detailed analysis on the onset of LCOs in digitally controlled power converters is presented and the design conditions for LCO-free operation are revised. In addition, the difference in the DPWM resolution in terms of output voltage quantization with respect to the duty-cycle for the buck and boost converter are highlighted and the minimum required resolution of DPWM for LCO-free operation in boost converter is derived. The DTD and the DDPWM modulation are then explained in Sect. III and Sect. IV presents the complete system design, the Simulink/Modelsim co-simulation of the power stage, and the digital controller employed to validate the design, the hardware implementation, and the testing procedure. Simulation and experimental results are presented and discussed in Sect. V, where the effectiveness of DDPWM in mitigating the onset of LCOs, improvement by more than 6X the DC accuracy, and reducing output voltage ripple is verified under different operating conditions and various resolutions of the ADC and of the DPWM. In the same section, a boost converter featuring DDPWM is also compared in terms of performance with a similar converter featuring DPWM with DTD and a reduction of output voltage ripple by 3X is achieved. Finally, some concluding remarks are drawn in Section VI.

II. LIMIT-CYCLE OSCILLATION IN DIGITALLY CONTROLLED POWER CONVERTERS

In this section, the quantization-induced limit cycle oscillations in digitally controlled power converter are briefly revised and some sufficient conditions to achieve LCO-free operation are presented. In addition, the difference in the DPWM resolution in terms of output voltage quantization with respect to duty cycle for the buck and boost converter is addressed.

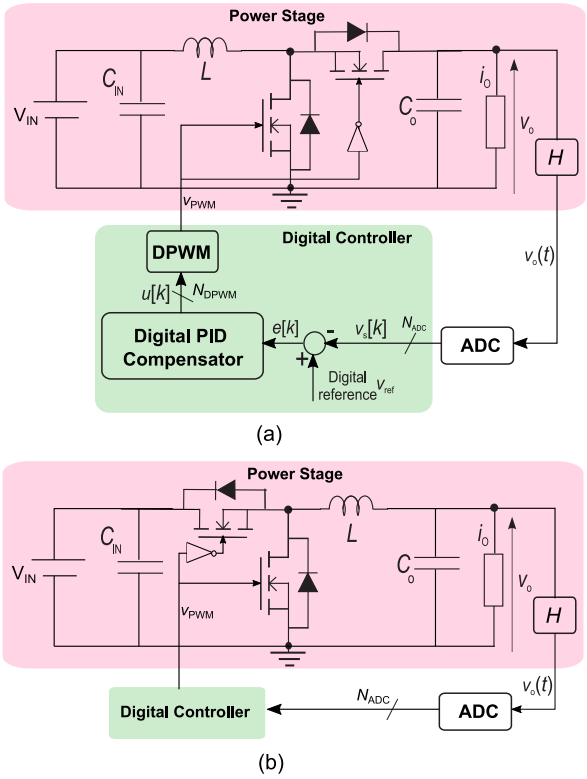

FIGURE 1. Block diagram of closed loop digitally controlled (a) boost converter (b) buck converter.

A. QUANTIZATION-INDUCED LIMIT CYCLES OSCILLATIONS

Synchronous boost (Fig. 1a) and buck (Fig. 1b) power converters with digital, voltage-mode control are considered in what follows. They both consist of a half-bridge driven by the PWM signal v_{PWM} generated by the digital controller block at the switching frequency of $f_{\mathrm{sw}} = 1/T_{\mathrm{sw}}$.

As shown in Fig. 1a, an ADC converts the output voltage $v_{\mathrm{o}}(t)$ into the digital code $v_{\mathrm{s}}[k]$ at a sampling frequency equal to the switching frequency f_{sw} of the power converter, i.e.,

$$v_{\mathrm{s}}[k] = H \cdot v_{\mathrm{o}}(kT_{\mathrm{sw}})$$

where H is the output voltage-divider gain for ADC input interfacing and $k = 0, 1, 2, \cdots$. In this context, the ADC quantization bin translates into a quantization step of the output voltage:

$$q_{\mathrm{v_o}}^{(\mathrm{ADC})} = \frac{V_{\mathrm{FS}}}{2^{N_{\mathrm{ADC}}} \cdot H} \tag{1}$$

where V_{FS} is the ADC input range and N_{ADC} is the number of bits of the ADC.

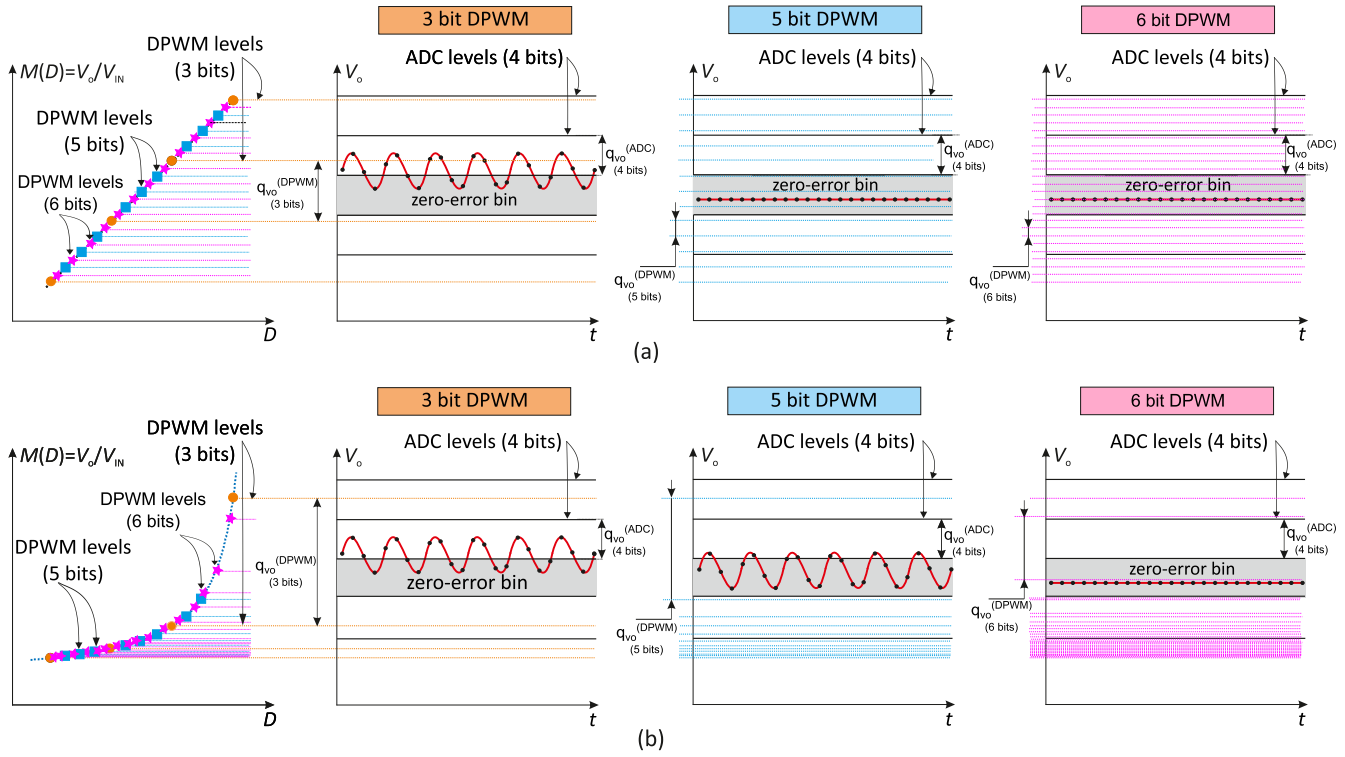

FIGURE 2. DPWM-induced output voltage quantization for $N_{\text{DPWM}} = 3$, $N_{\text{DPWM}} = 5$ and $N_{\text{DPWM}} = 6$ having $N_{\text{ADC}} = 4$ for: (a) buck converter (b) boost converter.

The digitized output $v_s[k]$ is then compared with a digital reference v_{ref} to get the digital error signal $e[k]$, i.e.,

$$e[k] = v_{\text{ref}} - v_s[k].$$

The error signal $e[k]$ is then processed by a digital proportional-integral-derivative (PID) controller which calculates the duty cycle to be applied in the next switching period. The DPWM modulator output is then used to generate a PWM signal with the required duty-cycle for driving the converter switches.

The quantization interval of the DPWM is:

$$q_{\text{D}}^{(\text{DPWM})} = \frac{1}{2^{N_{\text{DPWM}}}} \tag{2}$$

where N_{DPWM} is the number of bits of the DPWM. The DPWM modulator is operating at clock frequency $f_{\text{clk}} = 1/T_{\text{clk}}$ and since there are fixed quantization intervals of DPWM modulator, the on-time T_{on} of the switching period T_{sw} is restricted to be an integer multiple of T_{clk} resulting in a quantized duty-cycle $D = T_{\text{on}}/T_{\text{sw}}$, which eventually results in quantized output voltage levels. A duty cycle variation produces DPWM quantization of output voltage which is approximately equal to,

$$q_{v_{\text{o}}}^{(\text{DPWM})} \approx \left(\frac{\text{d}M}{\text{d}D}\right)_D \cdot q_{\text{D}}^{(\text{DPWM})} \cdot V_{\text{IN}} \tag{3}$$

where M is the converter conversion ratio, (i.e., $M = V_{\text{o}}/V_{\text{IN}}$) [13].

If no $q_{v_{\text{o}}}^{(\text{DPWM})}$ level lies inside the zero-error bin of the ADC, the zero-error condition cannot be attained and the output oscillates between two or more duty-cycle levels, which correspond to an average output voltage around the zero-error bin. As a result, low frequency LCOs can be observed in the output voltage.

The LCOs can be avoided if three conditions, which will be described in the following, are satisfied [6], [8], [9].

The first of these conditions is that the $q_{v_{\text{o}}}^{(\text{DPWM})}$ should be smaller than the $q_{v_{\text{o}}}^{(\text{ADC})}$, i.e.,

$$q_{v_{\text{o}}}^{(\text{DPWM})} < q_{v_{\text{o}}}^{(\text{ADC})}. \tag{4}$$

Meeting the above condition requires a trade-off among f_{clk}, f_{sw} and N_{ADC}. A lower N_{ADC} results in DC inaccuracy of output voltage. For example, for a $f_{\text{clk}} = 100$ MHz, $f_{\text{sw}} = 3$ MHz, the N_{DPWM} is found to be:

$$N_{\text{DPWM}} = \log_2\left(\frac{f_{\text{clk}}}{f_{\text{sw}}}\right) = 5.$$

Meeting (4) requires $N_{\text{ADC}} = 4$-bits or less, which is very low for most practical applications. Alternatively, for high DC accuracy i.e., $N_{\text{ADC}} = 8$-bits or even higher and switching frequency $f_{\text{sw}} = 3$ MHz requires at least $f_{\text{clk}} = 1.5$ GHz which is an impractical high clock frequency.

The second required condition is that there should be an integral gain K_{i} in the PID control law, i.e.,

$$0 < K_{\text{i}} \leq 1. \tag{5}$$

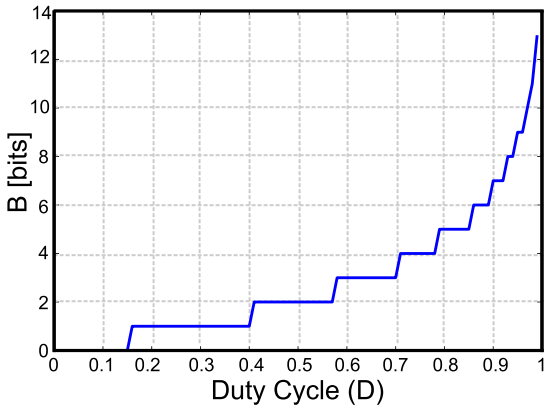

FIGURE 3. Minimum required increase in DPWM resolution than ADC resolution to satisfy LCO-free operation condition in boost converter.

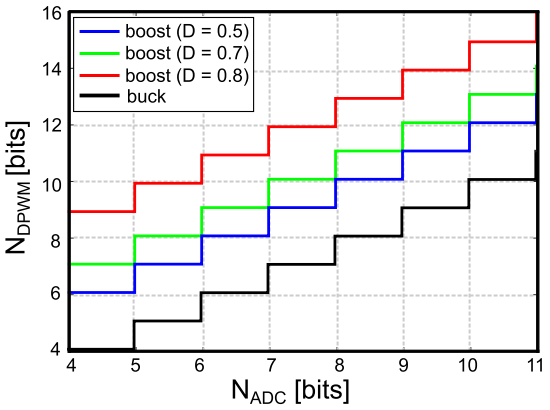

FIGURE 4. Minimum required DPWM resolution vs ADC resolution for different duty cycle values for buck and boost converter.

An integral term K_i in the controller leads the integrator output to gradually approach the zero-error bin and will remain there as long as the error signal is zero.

The third condition is about the Nyquist stability criterion that should be respected in large-signal conditions [6], i.e.,

$$1 + L(j\omega) \cdot N(A) \neq 0 \tag{6}$$

where $N(A)$ is the describing function for non-linear quantizers, A is the AC amplitude for the ADC, and $L(j\omega)$ is the loop gain.

While the conditions (5) and (6) are not difficult to be met by design with convenient PID coefficients, (4) is related to the resolution of the ADC and of the DPWM and is a more challenging requirement.

B. COMPARISON OF BUCK AND BOOST CONVERTER IN TERMS OF OUTPUT VOLTAGE QUANTIZATION

In what follows, the relationship between the resolution of the ADC and that of the DPWM to meet the condition (4) is investigated in case of both the buck and the boost converter.

Considering the buck converter in Fig. 1b, the output voltage quantization due to the DPWM resolution in (3) can be expressed as:

$$q_{v_o}^{(\mathrm{DPWM})} = q_{\mathrm{D}}^{(\mathrm{DPWM})} \cdot V_{\mathrm{IN}} \tag{7}$$

since the $M(D) = D$ [13].

As a consequence, for the buck converter, $q_{v_o}^{(\mathrm{DPWM})}$ is independent of D and the change in the output voltage is proportional to the change in the duty cycle. By replacing (1) and (2) in (7), the LCO-free operating condition (4) becomes:

$$2^{N_{\mathrm{DPWM}}} > \frac{2^{N_{\mathrm{ADC}}} \cdot V_{\mathrm{IN}} \cdot H}{V_{\mathrm{FS}}}$$

and by taking the logarithm in base 2, we get:

$$N_{\mathrm{DPWM}} > N_{\mathrm{ADC}} + A \tag{8}$$

where,

$$A = \left\lceil \log_2 \frac{V_{\mathrm{IN}} \cdot H}{V_{\mathrm{FS}}} \right\rceil$$

is a constant which depends on the design parameters and specifications. As an example, the second plot from the left in Fig. 2a shows, for a buck converter, a 3-bit DPWM-induced output voltage quantization (circle marks), as well as the output voltage bins due to 4-bit ADC quantization. In this situation, no DPWM output voltage quantization level falls within the ADC zero-error bin. As a result, a limit cycle arises. The third and fourth plots from the left in the same Fig. 2a, the DPWM resolution has been increased to 5-bits (square marks) and 6-bits (star marks), respectively, i.e., fulfilling the LCO-free operation criteria (4). It can be seen that at least one DPWM quantization level lies into ADC zero-error bin and the controller adjusts the output voltage at one stable point, supposing conditions (5) and (6) are satisfied, avoiding limit cycles.

By contrast, in the boost converter in Fig. 1a, $M(D) = 1/(1-D)$ [13], so (3) becomes:

$$q_{v_o}^{(\mathrm{DPWM})} = \frac{1}{(1-D)^2} \cdot q_{\mathrm{D}}^{(\mathrm{DPWM})} \cdot V_{\mathrm{IN}} \tag{9}$$

which suggests that $q_{v_o}^{(\mathrm{DPWM})}$ is depending on D with finer output voltage quantization steps for lower duty-cycle values while the step size increases as the duty cycle increases. The non-linear output voltage quantization makes the LCO-free operation condition (4) more critical to be achieved for the boost rather than the buck converter.

By carrying out calculations similar to those previously done for the buck converter, the minimum DPWM resolution found for the boost converter is:

$$N_{\mathrm{DPWM}} > N_{\mathrm{ADC}} + B \tag{10}$$

where,

$$B = \left\lceil \log_2 \frac{V_{\mathrm{IN}} \cdot H}{V_{\mathrm{FS}}} + \log_2 \frac{1}{(1-D)^2} \right\rceil$$

is depending on the duty cycle. The plot of B for the whole range of duty cycle values is shown in Fig. 3. As an example, the second plot from the left in Fig. 2b shows for a

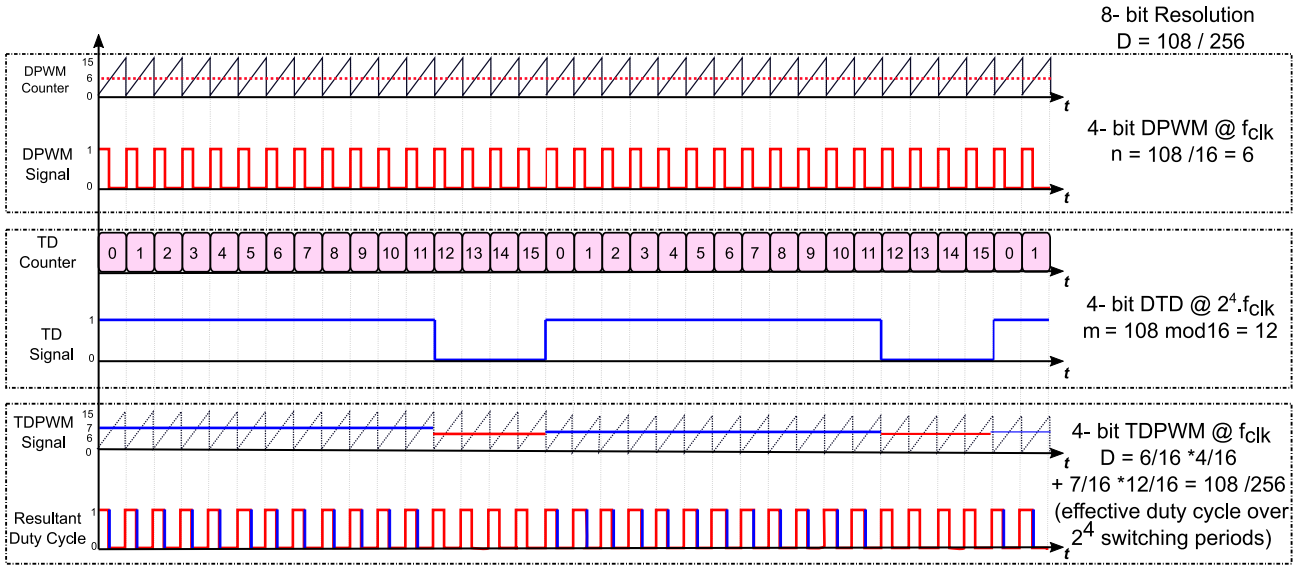

FIGURE 5. 8-bit Digital thermometric dithering pulse width modulation having 4-bit DPWM and 4-bit DTD.

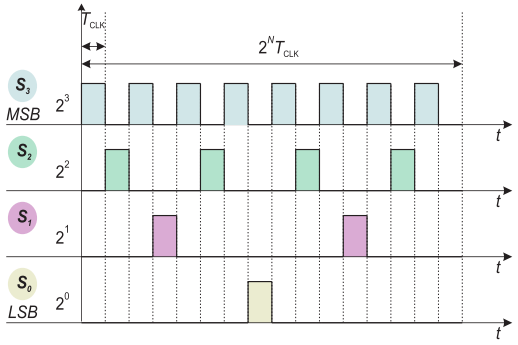

FIGURE 6. 4-bit dyadic basis signals.

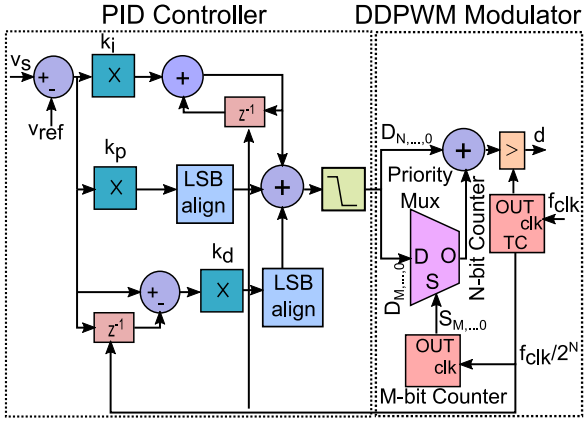

FIGURE 7. Block diagram of digital PID compensator and DDPWM.

boost converter, a 3-bit DPWM quantization interval (circle marks) and 4-bit ADC quantization bins in terms of the output voltage. As expected, there is no DPWM quantization level which lies in the ADC zero-error bin resulting in limit-cycles oscillations. The third plot from the left in the same Fig. 2b, the DPWM resolution has been increased to 5-bits (square marks), but again no DPWM quantization interval lies in the zero-error bin. It means that simply having the DPWM resolution higher than the ADC resolution is not straightforward in the case of the boost converter. The operating value or range of the duty cycle must be considered. The plot of the minimum DPWM resolution required as a function of the ADC resolution for different values of duty cycle to have LCO-free operation for both the buck and the boost converter is shown in Fig. 4. Following (10) in the fourth plot from the left in Fig. 2b, the DPWM resolution has now been increased to 6-bits (star marks), i.e., fulfilling the LCO-free operation criteria (4). The DPWM quantization level now lies into ADC zero-error bin, thus avoiding limit cycles.

III. DIGITAL PULSE WIDTH MODULATION TECHNIQUES

In order to avoid the onset of LCO at high ADC resolution, several techiques aiming at increasing the effective DPWM resolution have been proposed. The DTD and the recently proposed DDPWM techniques are briefly explained in what follows.

A. DIGITAL THERMOMETRIC DITHERING

In this technique, the average duty cycle is controlled by varying it with sub-LSB resolution over a pre-defined dithering pattern effectively increasing the DPWM resolution without increasing the clock frequency [19].

DTD is illustrated in Fig. 5 for a duty-cycle $D = 108/256$ taken as an example. The 8-bit duty-cycle obtained from PID compensator is splitted into $N = 4$ MSBs employed to represent the number $n = 6$ and $M = 4$ LSBs containing $m = 12$. The M-bit DTD modulator, whose counter is operated at $f_{clk}/2^N$ (i.e., $f_{clk}/16$), provides DTD

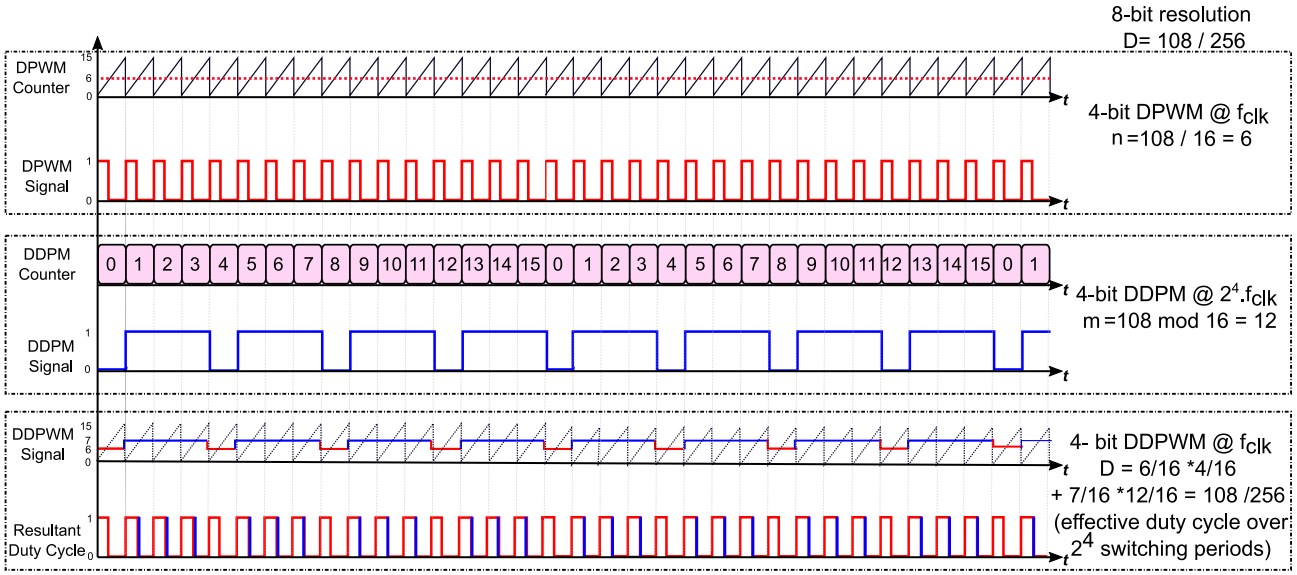

FIGURE 8. 8-bit Dyadic digital pulse width modulation having 4-bit DPWM and 4-bit DDPM.

signal based on input to DTD, i.e., $m = 12$. The DTD signal whose value is either 0 or 1 is added to $n = 6$ and the obtained resultant PWM signal is input to a plain N-bit DPWM modulator operated at f_{clk}. It eventually generates the duty cycle, which is $D_1 = (n+1)/2^N$ (i.e., $D_1 = 7/16$ shown in blue in Fig. 5) for the first $m = 12$ switching periods and $D_{\text{o}} = n/2^N$ (i.e., $D_{\text{o}} = 6/16$) for the remaining $(2^M - m) = 4$ switching periods. So that an average duty cycle $D = (n \cdot 2^M + m)/2^{(N+M)}$ (i.e., $D = 108/256$) is achieved over 2^M switching periods, hence effectively increases the resolution of DPWM.

Digital dithering is easy to implement and highly controllable, but it may introduce distortion due to noise at switching frequency sub-harmonics which cannot be filtered out properly, hence causing large ripple in the output voltage [8].

B. DYADIC DIGITAL PULSE WIDTH MODULATION

In order to address the limitations of the digital thermometric dithering discussed in the previous subsection, the DDPWM has been recently proposed and experimentally validated on a digitally controlled DC-DC buck converter [8], [9]. It is based on the dyadic digital pulse modulation (DDPM) pattern [20], [21], i.e.,

$$\Sigma_m(t) = \sum_{i=0}^{M-1} b_i \cdot S_i(t)\,(0 < t < T) \tag{11}$$

where $b_i \in 0, 1$ is the bit value corresponding to the i-th binary digit, $i = 0, 1, \cdots, M$, and $S_i(t)$ are the dyadic basis signals which contain 2^i "one" pulses and $2^{M-i} - 1$ "zero" pulses [20]. For all $i = 0, 1, \cdots, M$, the $S_i(t)$ are made orthogonal to each other, i.e., $(S_i(t) \cdot S_k(t) = 0, \forall i \neq k)$. The 4-bit dyadic basis signals are shown in Fig. 6.

Based on the analysis presented in [22], the spectrum of a DDPM stream can be expressed as:

$$X_m^{\text{DDPM}}(f) = \sum_{k=-\infty}^{+\infty} a_k \cdot c_{k,m}\delta(f - kf_0) \tag{12}$$

where,

$$f_0 = \frac{1}{T_0}$$

$$a_k = \frac{1}{2^M}\,\text{sinc}\left(\frac{k}{2^M}\right) e^{\frac{-jk\pi}{2^M}}$$

$$c_{k,m} = \sum_{i=0}^{M-1} b_{i,m} 2^i \sum_{p=0}^{2^{M-i}-1} (-1)^p \delta[k - 2^i p]$$

$\delta[\cdot]$ is the Kronecker function defined as

$$\delta[\cdot] = \begin{cases} 0 & n = 0 \\ 1 & n \neq 0 \end{cases}$$

The envelope of the spectra of DDPM waveforms found from (12) for different m is [23],

$$S(kf_0) = \max_m |X_m^{\text{DDPM}}(kf_0)|. \tag{13}$$

From the above equations, the qualitative analysis of the DDPM spectral components has been carried out in [8], [9], [22], and [23], revealing that most of the spectral energy of the spurious spectral components is pushed at high frequencies, where it can be easily filtered out by a first-order low-pass filter.

The FPGA-based hardware implementation and a software implementation of a DDPM modulator, suitable to a microcontroller implementation, have been presented in [20] and [24], respectively.

The PID compensator along with DDPWM can be implemented on hardware as shown in Fig. 7. The duty-cycle D calculated by the PID compensator which is sampled at $f_{\rm clk}/2^M$ is splitted in N MSBs which are input to a plain DPWM modulator operated at $f_{\rm clk}$, while the M LSBs are given as input to the priority multiplexer (mux) of the DDPM modulator. The following Boolean function is implemented by the priority mux,

$$O = \sum_{i=0}^{M-1} D_{M-i-1} \cdot S_i \cdot \prod_{k=0}^{i-1} (\bar{S}_k). \tag{14}$$

The selection inputs $S_{M,\ldots,0}$ of the priority mux are driven by an M-bit counter clocked at $f_{\rm clk}/2^N$. At each clock, a new counter value arrives at the selection input, which is checked for '1' starting at LSB, where k is the position of first '1'. The priority of the multiplexer is such that the mux output O takes the value D_{M-k} of the data input $D_{M,\ldots,0}$. The output O is hold at zero if all selection inputs are zero.

In a full 2^M counting period, at every other clock period (i.e. 2^{M-1} times), $S_0 = 1$ and the output O takes the value of D_{M-1}. In the other counting periods, i.e. when $S_0 = 0$, in one half of the cases (i.e. 2^{M-2} times), $S_1 = 1$ and the output O is driven to the logic value of D_{M-2}. By similar arguments, the output O is driven in a full counting period to the value of D_i exactly 2^i times according with the DDPM pattern in Fig. 6.

The DDPWM waveforms are illustrated in Fig. 8 for a duty cycle $D = 108/256$ taken as an example. The 8-bit duty cycle obtained from the PID compensator is splitted in $N = 4$ MSBs employed to represent the number $n = 6$ and $M = 4$ LSBs containing $m = 12$. The proposed M-bit DDPM modulator whose counter is operated at $f_{\rm clk}/2^N$ will generate DDPM signal which is based on input to DDPM, i.e., $m = 12$ ($D_{M,\ldots,0} = 1100b$). The obtained DDPM signal whose value is either 0 or 1 is added to $n = 6$ and the resultant DDPWM signal is given as input to plain N-bit DPWM modulator operated at $f_{\rm clk}$. It will eventually generate a duty cycle, which is varying among two adjacent quantization levels, i.e., $D_{\rm o} = \frac{n}{2^N}$ ($D_{\rm o} = \frac{6}{16}$) or $D_1 = \frac{(n+1)}{2^N}$ ($D_1 = \frac{7}{16}$ shown in blue in Fig. 8). Since a duty cycle D_o is applied $2^M - m$ times and a duty cycle D_1 is applied m times over a pattern of 2^M switching periods, the average duty-cycle over a period of 2^M is calculated as,

$$D = \frac{n}{2^N} \cdot \frac{2^M - m}{2^M} + \frac{n+1}{2^N} \cdot \frac{m}{2^M} = \frac{n \cdot 2^M + m}{2^{N+M}} = \frac{108}{256}.$$

The effective resolution of the N-bit DPWM modulator is increased to $(N + M)$-bits by employing DDPWM without trading off among DC accuracy and clock frequency to achieve LCOs free operation. Thanks to the spectral properties of the DDPWM modulation (previously discussed in [10]), this increased resolution is achieved at minimum output ripple degradation, since the DDPWM ripple components are pushed at higher frequencies and can be more effectively suppressed by the output filter.

TABLE 1. Design specifications of complete system.

Parameters	Values	Unit
Input Voltage '$V_{\rm IN}$'	7 - 10	V
Input Capacitor '$C_{\rm IN}$'	1	μF
Capacitor Equivalent Series Resistance '$r_{\rm C}$'	10	mΩ
Inductor 'L'	900	nH
Inductor series Resistance '$r_{\rm L}$'	8	mΩ
FET ON Resistance '$R_{\rm on}$'	24	mΩ
Output Capacitor '$C_{\rm o}$'	3	μF
Capacitor Equivalent Series Resistance '$r_{\rm C_o}$'	3.3	mΩ
Load Resistor '$R_{\rm L}$'	25	Ω
Voltage Divider Gain 'H'	1 / 9.2	-
ADC Input Range '$V_{\rm FS}$'	3	V
Clock Frequency '$f_{\rm clk}$'	18.75, 37.5, 75, 150	MHz
Switching Frequency '$f_{\rm sw}$'	1.17	MHz
Proportional Gain '$K_{\rm p}$'	20	-
Derivational Gain '$K_{\rm d}$'	79	-
Integral Gain '$K_{\rm i}$'	0.009	-
$N_{\rm ADC}$	4 - 11	bits
$N_{\rm DPWM}$	4 - 7	bits
$N_{\rm DDPM}$	4	bits
$N_{\rm DTD}$	4	bits

IV. SIMULATION AND HARDWARE IMPLEMENTATION APPROACH

The above-described approach is validated for the boost converter both through simulations and measurements. A digitally controlled boost power converter as depicted in Fig. 1a is considered for validation. It includes the power stage and the controller, containing the digital compensator, the DDPWM and the ADC. The converter is designed to operate in CCM over an input voltage ranging from 7 to 10 V and output voltage regulated at 13.8 V, with a switching frequency of 1.17 MHz while a voltage-mode digital control algorithm is considered. The compensator gains have been computed to obtain a crossover frequency $f_{\rm c} = 100$ kHz with a phase margin of $\phi = 45^o$. All the parameters, components value along with their parasitics are reported in Tab. 1.

The Simulink/Modelsim co-simulation and hardware implementation of the power stage and the digital controller employed to validate the effectiveness of the DDPWM in suppressing the onset of the LCOs, increasing DC accuracy, and reducing output voltage ripple are discussed in this section.

A. CO-SIMULATION TEST SETUP

The synchronous DC-DC boost converter has been simulated on Matlab/Simulink with the component values reported in Tab. 1. The digital PID compensator and the DDPWM, whose architecture is discussed in the previous section, have been implemented starting from their description in Verilog. The verification and simulation tool Modelsim is then used to simulate the hardware-description language (HDL) design of the complete digital controller.

In order to perform a complete system simulation, the co-simulation wizard tool of MATLAB is used to simulate the Modelsim block described in Verilog within the Simulink environment [25]. Since the block contains the HDL implementation of the digital controller (i.e., digital

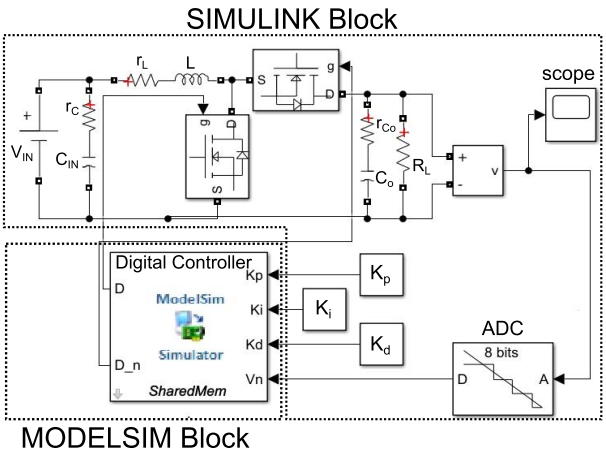

FIGURE 9. Simulation test setup of digitally controlled boost converter.

PID compensator and DDPWM), the Simulink-ADC block is used to convert the output voltage to a quantized digital value which is then provided as input to the Modelsim Simulator block for the digital controller processing. This block performs the error signal computation, PID calculations, and DDPWM evaluation. The square-wave PWM generated signal taken as the output of the Modelsim block is eventually used to control MOSFETs switching. The complete setup is shown in Fig. 9.

The behavior of output voltage is shown on the scope connected to the load resistor. The results are obtained for various ADC and DPWM resolutions and for multiple input voltages to the converter and will be commented on and compared to experimental results in the next section.

B. EXPERIMENTAL TEST SETUP

The experimental test setup schematic is shown in Fig. 10a. It includes the EPC9006C development board which contains half-bridge with onboard gate drivers, featuring the enhancement mode (eGaN) field effect transistors (FET) used for high-switching frequency applications [26]. The purpose of this development board is to operate at high frequencies and simplifies the evaluation process of the EPC2007C eGaN FETs by including all the critical components on a single board that can be easily wired to external components to build different topologies of switching converters. To this purpose, a printed circuit board (PCB) has been designed to allocate the inductor L and load resistor R_o to obtain, together with the EPC9600C board to which is connected through a 12-pin female header, the boost in Fig.1a. A c2000 microcontroller prototyping board operates as a digital controller (i.e., digital PID compensator and DDPWM) containing a 150 MHz TMS320F2833F processor with an onboard 8-channel 12-bit ADC module and an enhanced PWM (ePWM) module [27]. The ePWM output pin is wired to the EPC9006C PWM input pin while the connection between the boost and the ADC module is assured by a SMA cable. The testbench includes a DC power supply and a digital storage oscilloscope as shown

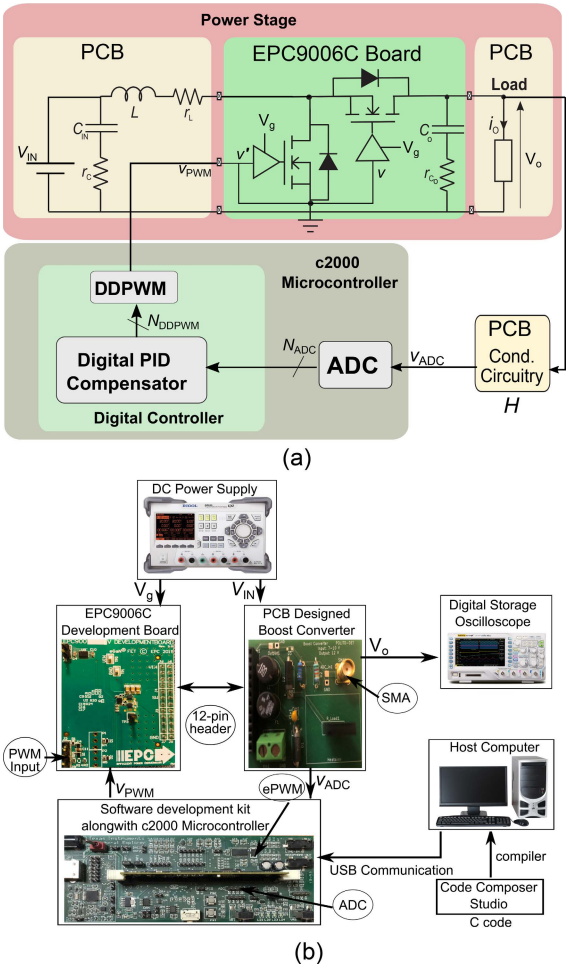

FIGURE 10. Experimental test setup of digitally controlled boost converter (a)Test setup schematic (b)Block diagram of the experimental testbench.

in Fig. 10b. The complete architecture of the digital control employed in this work is reported in Fig. 11. It entails a microcontroller interface of the digital control employed in this work to the ADC and the ePWM module. The ePWM module is initially configured for a target resolution depending on the DPWM resolution, i.e., N_{DPWM} and switching frequency, f_{sw}. The DPWM counter operates at clock frequency $f_{\text{clk}} = f_{\text{sw}} 2^{N_{\text{DPWM}}}$. Whenever the counter value reaches the maximum count, an ADC start of conversion (SOC) interrupt is called, which will trigger the ADC sampling according to defined sampling channels and sampling frequencies. The controller processing time should be considered in order to work properly at the desired frequency, i.e., the time needed by the controller for PID computations must be less than the sampling period. Since, the clock frequency is 150 MHz, the switching frequency is 1.17 MHz and the controller takes 172 clock cycles to complete a process, the sampling frequency is set to half of the switching frequency (i.e., $f_s = f_{\text{sw}}/2$). The error signal is then processed by the PID compensator to calculate a new duty-cycle value at each sampling instant. This duty cycle value is updated in the compare

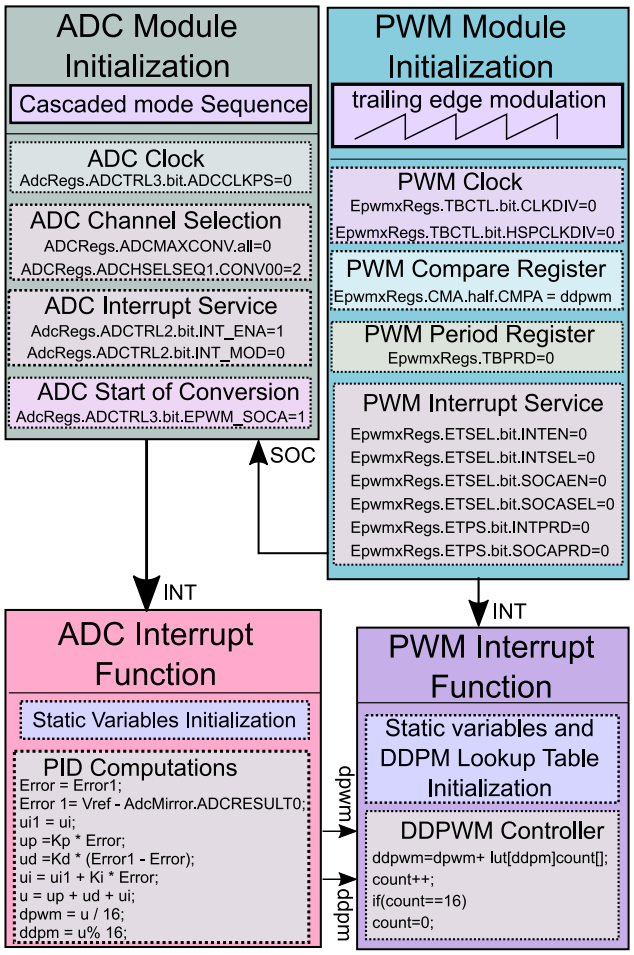

FIGURE 11. C code Architecture.

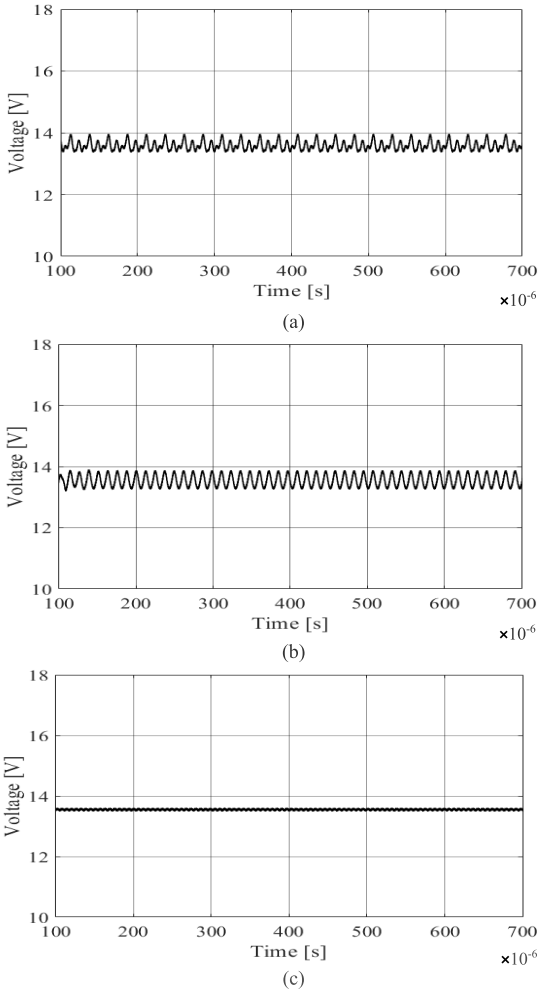

FIGURE 12. Simulated output voltage of the boost converter. (a) $N_{ADC} = 7$, $N_{DPWM} = 5$; (b)$N_{ADC} = 7$, $N_{DPWM} = 5$, $N_{DTD} = 4$; (c) $N_{ADC} = 7$, $N_{DPWM} = 5$, $N_{DDPM} = 4$.

register (dedicated input register) of the ePWM module at each switching period. It will eventually generate a square-wave PWM signal at the defined ePWM output pin of the prototype board.

A number of experiments are performed with different converter parameters, to acquire the corresponding data, process them, and display parametrically the results.

V. RESULTS AND DISCUSSIONS

The simulated and measured results obtained for both DDPWM-modulator and digital thermometric dithering modulator are compared and discussed. In particular, the LCOs suppression, the DC accuracy, and output ripple for various resolutions of ADC, DPWM, and DDPM are presented in this section.

A. LCO SUPPRESSION

The simulated output voltages of the boost converter are reported in Fig. 12 for different parameters of the controllers.

Regarding the LCOs, Fig. 12a shows the results for $N_{ADC} = 7$-bits and $N_{DPWM} = 5$-bits. The DPWM modulator is clocked at $f_{clk} = 37.5$ MHz. Under these operating conditions and resolutions, the conditions discussed in Sect.II for LCO-free operation are not met, i.e., $N_{DPWM} \not> N_{ADC}$. This causes low-frequency LCOs that can be clearly seen at the output voltage.

Similarly in Fig. 12b, $N_{DTD} = 4$-bits DTD is introduced together with $N_{DPWM} = 5$-bit DPWM modulator. The effective resolution of overall DTDPWM modulator is now increased to $N_{DPWM} + N_{DTD} = 9$-bits. It can be observed that LCOs are suppressed, but a significant ripple voltage at the frequency of the thermometric dithering pattern has appeared. This is due to the fact that the DTD pattern introduces distortion and noise at low frequencies, i.e., within the controller bandwidth, which can not be filtered out by a low-pass LC filter. Although it effectively increases the resolution of DPWM, which is helpful in mitigating the LCOs, this is achieved at the expense of DTD-induced ripple, which degrades the performance of DTD. The frequency of the DTD-induced ripple is $f_{sw}/2^{N_{DTD}}$ (i.e., 73.125 kHz).

By contrast, in Fig. 12c, $N_{DDPM} = 4$-bits DDPM modulation is presented in addition to $N_{DPWM} = 5$-bit DPWM

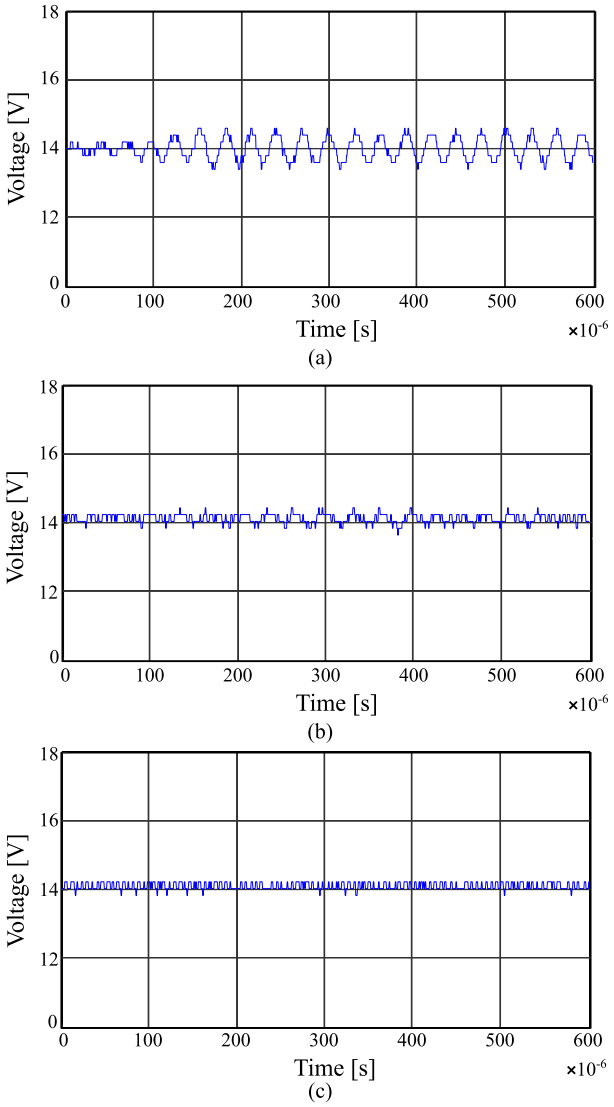

FIGURE 13. Measured output voltage of the boost converter. (a) $N_{ADC} = 7$, $N_{DPWM} = 5$; (b)$N_{ADC} = 7$, $N_{DPWM} = 5$, $N_{DTD} = 4$; (c) $N_{ADC} = 7$, $N_{DPWM} = 5$, $N_{DDPM} = 4$.

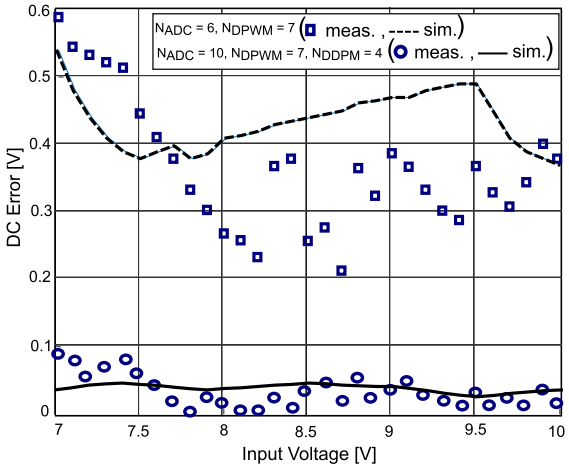

FIGURE 14. Simulated and measured DC error w/ and w/o 4-bit DDPM.

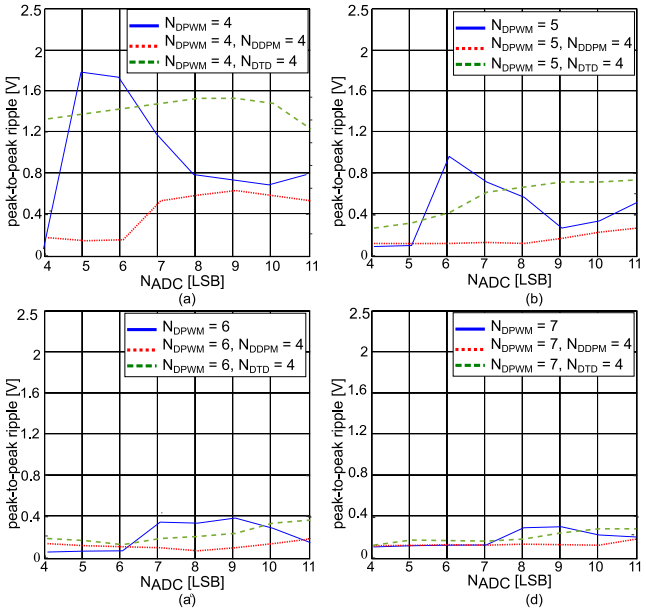

FIGURE 15. Simulated ripple of the output voltage (a) $N_{DPWM} = 4$ (b) $N_{DPWM} = 5$ (c) $N_{DPWM} = 6$ (d) $N_{DPWM} = 7$.

modulator. The effective resolution of the overall DDPWM modulator is now increased to $N_{\mathrm{DPWM}}+N_{\mathrm{DDPM}} = 9$-bits. It is observed that there are no LCOs and no additional ripple is present at the output voltage. The output is highly regulated. Since the controller is now able to drive output to the zero-error bin, the duty cycle generated by the PID compensator is constant and the error signal to the controller is zero. Thanks to the dyadic pattern, the distortion and noise are at high frequencies which can easily be filtered out by a low-pass LC filter.

The measured results displayed at the oscilloscope for a similar experiment are shown in Fig. 13. It is observed that the voltage regulation, LCOs behavior, and ripple amplitude of measurement results are in close agreement with the simulation results. The offset in the output voltage which is observed in measured results is consistent with the DC accuracy results for $N_{\mathrm{DPWM}} = 7$ bits, that are better explained in the later subsection.

B. DC ACCURACY

The output voltage DC error, which mainly depends on the ADC resolution, is simulated for the whole range of input voltage. The ADC resolution is set to $N_{\mathrm{ADC}} = 6$-bits and a DPWM resolution $N_{\mathrm{DPWM}} = 7$-bits is considered in order to meet LCOs free operation criteria. The DC error is computed and represented in Fig. 14 (dotted line). It can be observed that a maximum DC error of 540 mV is obtained.

A similar test has been performed for the same DPWM resolution but $N_{\mathrm{DDPM}} = 4$-bits DDPM modulation is introduced too in addition to $N_{\mathrm{DPWM}} = 7$-bit DPWM modulator. Now,

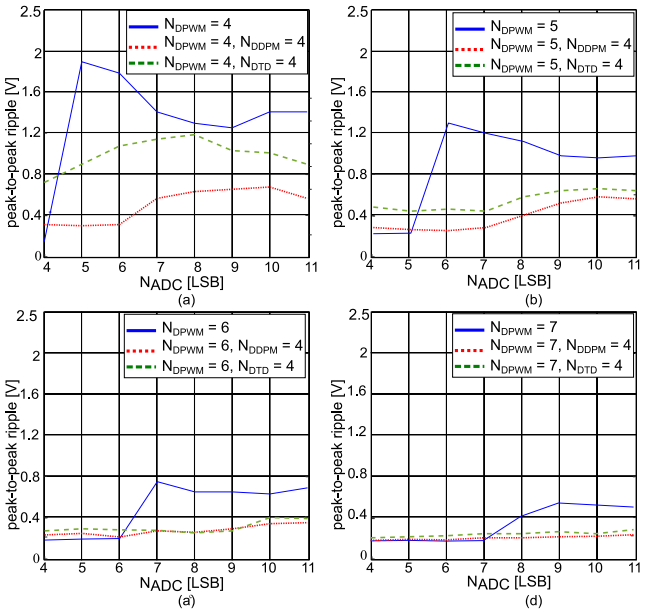

FIGURE 16. Measured ripple of the output voltage (a) $N_{DPWM} = 4$ (b) $N_{DPWM} = 5$ (c) $N_{DPWM} = 6$ (d) $N_{DPWM} = 7$.

the effective resolution of the overall DDPWM modulator is increased to $N_{\text{DPWM}} + N_{\text{DDPM}} = 11$-bits. In view of that, an ADC resolution of $N_{\text{ADC}} = 10$-bits can be adopted here in order to meet LCOs free operation criteria. The DC error is computed and represented in Fig. 14 (solid line). It can be observed that the maximum DC error of 60 mV is obtained which is approximately 9X less compared to other case. It means that the DDPWM is effective in significantly improving the DC accuracy of output voltage.

The measurement results are also reported in the same Fig. 14, in which around 6.5X less DC error is obtained.

C. OUTPUT RIPPLE

Starting with the $N_{\text{DPWM}} = 4$-bit plain-DPWM modulation, the amplitude of output ripple has been computed and plotted versus various ADC resolutions ($N_{\text{ADC}} = 4, 5, \cdots, 11$). Similarly, the test has been repeated for 4-bit DDPM and 4-bit DTD modulators along with DPWM modulation and plotted in the same figure. The similar tests has been performed for $N_{\text{DPWM}} = 5, 6$ and 7 bits. The corresponding simulation results are presented in Fig. 15.

It can be observed that in case of plain-DPWM modulator (solid line), there is a large output ripple due to the limit-cycle oscillations except for the case when $q_{v_o}^{(\text{DPWM})} \leq q_{v_o}^{(\text{ADC})}$, i.e., meeting the LCO-free operation criteria. The maximum amplitude of ripple is 1.8 V peak-to-peak. By introducing 4-bit DTD modulation (dashed line), the LCOs are highly suppressed but the amplitude of ripple is very large, i.e., up to 1.5 V peak-to-peak. The large ripple amplitude is due to the DTD pattern as discussed before. On the other hand, in the case of 4-bit DDPM modulation (dotted line), the LCOs are completely suppressed, and the amplitude of ripple is also reduced, i.e., up to 0.5 V peak-to-peak, which is 3X less.

The results of the experimental tests are reported in Fig. 16. The amplitude of ripple and LCOs obtained for both measurements and simulations are in fair agreement, thus confirming the effectiveness of the proposed approach.

VI. CONCLUSION

In this paper, the recently proposed DDPWM technique is adopted in a DC-DC boost converter in order to increase the resolution of the DPWM for LCO-free operation. Its performance is tested by both Simulink/Modelsim co-simulation and experimental characterization of a hardware prototype. The boost converter is designed to operate in CCM over a range of input voltages and fixed output voltage, with a switching frequency in the MHz range while a voltage-mode digital control algorithm is considered. The simulated and measured results obtained for both the DDPWM-modulator and the previously existing thermometric dithering are compared. The effectiveness of the DDPWM in mitigating the onset of the LCOs, increasing the DC accuracy, and reducing the ripple is verified under different operating conditions and for various resolutions of ADC and DPWM. Simulated and measured results are in substantial agreement with each other, which confirms the effectiveness of technique.

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