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Exploring Stability and Accuracy Limits of Distributed Real-Time Power System Simulations via System-of-Systems Co-simulation

Luca Barbierato, Enrico Pons, Ettore Francesco Bompard, Vetrivel S. Rajkumar, Peter Palensky, Lorenzo Bottaccioli, and Edoardo Patti

Abstract—Electro-Magnetic Transients (EMT) is the most accurate, but computationally expensive method of analyzing power system phenomena. Thereby, interconnecting several real-time simulators can unlock scalability and system coverage, but leads to a number of new challenges, mainly in time synchronization, numerical stability, and accuracy quantification. This study presents such a co-simulation, based on Digital Real-Time Simulator (DRTS), connected via Aurora 8B/10B protocol. Such a setup allows to analyze complex and hybrid System-of-Systems (SoS) whose resulting numerical phenomena and artifacts have been poorly investigated and understood so far. We experimentally investigate the impact of IEEE 1588 Precision Time Protocol (PTP) synchronization assessing both time and frequency domains. The analysis of the experimental results is encouraging and show that numerical stability can be maintained even with complex system setups. Growing shares of inverter-based renewable power generation require larger and interconnected EMT system studies. This work helps to understand the phenomena connected to such DRTS advanced co-simulation setups.

Index Terms—Co-simulation, Digital Real-time Simulators, Numerical Stability, Power System Assessments, System-of-Systems

ACRONYMS

CPU	Central Processing Unit
DRTS	Digital Real-Time Simulator
DUT	Device Under Test
E2E	End-to-End
EMT	Electro-Magnetic Transients
FPGA	Field Programmable Gate Array
GPS	Global Positioning System
I/O	Input/Output
ICT	Information and Communication Technologies
ITM	Ideal Transformer Method
IA	Interface Algorithm
LAN	Local Area Network
P2P	Peer-to-Peer
PTP	Precision Time Protocol
PSUT	Power System Under Test
PHIL	Power Hardware-In-the-Loop
ROS	Rest Of the System
SFP	Small-form Factor Pluggable
SoS	System-of-Systems

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TC Transparent Clock

I. INTRODUCTION

Significant scientific effort has recently been conducted on computer-aided power system analysis for the design, development, and test of future power system designs. This has resulted in multiple domain-specific simulation tools that can capture functionalities and behaviour of different power system components with a high-precision accuracy [1]. In particular, numerical real-time simulation has arisen as a critical tool for modern-day power system planning, design, and operation [2]. Real-time simulation refers to a digital twin of a real world power system which is simulated in *wall clock* time, to mimic the behaviour of its real-world physical counterpart. These real-time simulations are conducted using small, discrete, and constant time steps, usually in the order of a few μ s. The real-time constraints are susceptible to the targeted analysis. For instance, transient stability analysis is carried out with phasor simulations of around 10 ms of time step duration. Electro-Magnetic Transients (EMT) analysis instead requires a smaller time step duration (i.e. tens of microseconds) to detail the dynamics of large power systems [3]. In particular for EMT, innovative multiprocessor architecture (e.g. IBM® Power8) and Field Programmable Gate Array (FPGA) have been used to deploy Digital Real-Time Simulator (DRTS). DRTSs are solution to hardware accelerate EMT analysis [4] respecting real-time restrictions. These simulators allow fast Analogue and Digital Input/Output (I/O) to connect in a closed-loop a real-world equipment, allowing Power Hardware-In-the-Loop (PHIL) to test its functionalities in a safe experimental testbed. The major limitation of commercial DRTS is the significant amount of computational power required to run detailed EMT power system analysis, generating limitations on the dimension of simulated models [4], [5].

This limitation has prompted power systems and Information and Communication Technologies (ICT) experts to collaborate with each other to connect two or more DRTS by leveraging on novel co-simulation techniques [6], communication protocols, and standards [7]. These techniques permits breaking up a larger Power System Under Test (PSUT) into smaller sub-models, with each being executed on a dedicated DRTS. Such an approach involves the usage of Interface Algorithm (IA), such as the Ideal Transformer Method (ITM) [8], [9]. This IA is inspired by PHIL applications

and involves representing the Device Under Test (DUT) as a current source, with the network simulation as a voltage source [10], [11]. Thereby, a larger system is decomposed into a set of smaller-subsystems, thereby resulting in a SoS approach. This approach is demonstrated in recent work such as [12], wherein two university labs representing local energy communities have been interconnected. Similarly, in [13], [14], the ITM is used to interface geographically separated DRTS and PHIL equipment. Furthermore, such setups have also been extensively used for cybersecurity studies and resilience analysis, as noted in [15], [16].

Typically, such distributed real-time simulations are achieved through high-bandwidth communication protocols (e.g. IEEE802.3) to exchange interface signals (i.e. voltages and currents) between the sub-models/sub-systems. For instance, multiple joint research experiments, spanning continents, have been carried out to overcome the limitations of individual capabilities of real-time laboratories, such as the infrastructures proposed in [17], [18]. The objective of these experiments is to virtually interconnect DRTSs and PHIL setups in geographically distributed laboratories via the Internet, allowing simulation and testing of future power systems. Thus, a virtual research infrastructure can be formed.

In [19], the authors present a detailed overview and analysis of case studies related to co-simulation application, called *Real-Time Coupling of Geographically Distributed Research Infrastructures*, subsequently leading to the paradigm of geographically distributed simulations. However, these interconnections provoke numerical instabilities and accuracy issues due to inherent communication latencies between interconnected DRTSs, as noted in [20], [21]. The proposed solutions have been applying time delay compensation methods, such as the one in [22], [23]. However, these solutions severely limitate the scope of EMT studies. In fact, such compensation methods are still geared towards power PHIL setups but with significant slower dynamics than EMT simulations. Another associated drawback of distributed real-time co-simulations is time synchronisation between DRTSs. This leads to misalignment and inaccurate logging of results due to the probabilistic nature of the communication medium [24], [25]. Therefore, there is a need for a scalable and accurate solution to interconnect DRTSs for distributed real-time EMT simulations while adhering to real-time constraints.

This paper presents a novel application of a Locally Distributed Hybrid Digital Real-Time Co-simulation Infrastructure that allows a point-to-point connection of two DRTSs via the high-bandwidth communication protocol Aurora 8B/10B. Aurora reduces the consequence of uncertainty brought about by communication latency adhering to real-time constraints in a co-simulated environment. The proposed solution synchronises DRTSs' interconnections through the IEEE 1588 Precision Time Protocol (PTP) [26] to adjust co-simulation execution and logging of synchronized simulation results. Through this setup, we seek to explore the accuracy and stability limits of a distributed real-time co-simulation.

With respect to our previous works [27], [28], the key contributions and novelties proposed in this manuscript are summarised in the following.

- 1) This solution presents a more general time synchronization strategy that allows to concurrently implement different IEEE 1588 PTP stack configurations following the same GPS clock reference, required because different DRTS could implement different PTP profiles and delay mechanisms.
- 2) Different DRTS in our infrastructure can be interconnected for co-simulating a power system scenario, not only RTDS. In our laboratory setup, we propose RTDS and OPAL-RT, which are the main DRTS commercial solutions for power system analysis. Moreover, the infrastructure is flexible to integrate other DRTS solutions (e.g., Speed Goat, NI PXI) that implement the Aurora and IEEE 1588 PTP.
- 3) A comprehensive description of the intra-time step operations of RTDS and OPAL-RT is given, explaining how the different DRTS solutions manage the model calculation, the CPUs, the CPUs/FPGA communications, and the management of the Aurora link to better understand where the communication latency of the co-simulation impact is generated.
- 4) The laboratory setup has been tested on four different configurations involving either RTDS, OPAL-RT or both, where the two power subsystems have been run separately, namely *i)* RTDS-RTDS, *ii)* OPAL-OPAL, *iii)* RTDS-OPAL, and *iv)* OPAL-RTDS.
- 5) The sequence operations of each of the four configurations are described to explain the communication latency generated by the application of our co-simulation infrastructure. This allows a precise understanding of the contribution of the experienced latencies, instead of measuring the latency by running a simulation as in our previous works.
- 6) Time-domain and frequency-domain results present different latencies effects between the different infrastructure configurations.

The structure of the manuscript is described as follows. The computing capabilities and system size simulation limits of DRTS are discussed in Section II. The Locally Distributed Hybrid Digital Real-Time Co-simulation Infrastructure is described in Section III, along with the laboratory setup implemented for the experiments. The experimental results are shown in Section IV that includes *i)* the analytical description of the communication latency in the four proposed configurations, *ii)* the time-domain accuracy for steady state and transient scenarios, and *iii)* the frequency-domain accuracy for the steady state scenario. Concluding remarks and future work are provided in Section V.

II. SYSTEM SCALABILITY AND MOTIVATION

As briefly introduced in the previous Section I, the main limitation of commercial DRTS (e.g. OPAL-RT and RTDS Technologies) is the significant amount of computational power required to run detailed EMT models, thereby limiting the overall size of power systems that can be accurately simulated. The maximum size of the power system that can be simulated in one real-time simulator cannot be easily and precisely assessed, as it depends mainly on:

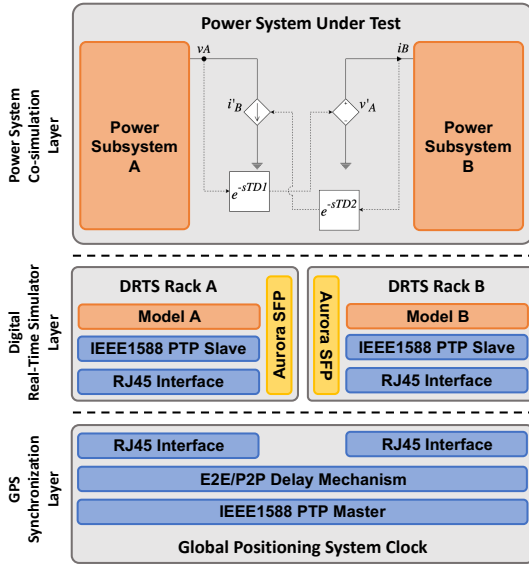


Fig. 1. The hybrid Locally Distributed Digital Real-Time Co-simulation infrastructure and its three main architectural layers.

- the size of the time-step used in the simulation;
- the model of the real-time simulator, software platform and solution algorithms;
- the complexity of the control systems in the model;
- the number of I/O channels needed.

A very rough figure is that on a single RTDS NovaCor chassis with one activated core, the simulated system can have a maximum of 90 single-phase buses. With more activated cores, the maximum network size per chassis is 600 single-phase buses. The actual size then depends on the complexity of the models used for the power system and control system components. A very rough figure for OPAL-RT is that with the eMEGASIM software, it is possible to simulate networks with a maximum of 60 to 70 single-phase nodes per activated core with a time-step of 50 μ s.

By coupling several DRTS in a co-simulation infrastructure it is possible to sum up the computational power of the different simulators and therefore simulate larger networks. Unfortunately, it is not possible to compare the simulation results for large networks in a monolithic simulation with the co-simulation, as the monolithic system would not run on a single DRTS due to a lack of computational resources. A detailed discussion on the scalability of such setups is beyond the scope of this work.

III. METHODOLOGY

The proposed Locally Distributed Digital Real-Time Co-simulation Infrastructure is a hybrid architecture that makes use of Aurora 8B/10B, a serial fiber optic link protocol, and IEEE1588 PTP, which is commonly used to synchronise internal reference clocks throughout a computer network, to enable the serial interconnection of various commercial DRTS (e.g. OPAL-RT and RTDS technologies). The architectural description of the proposed infrastructure is presented in Figure 1 and consists of three main layers: *i*) the *Global Positioning System (GPS) Synchronization Layer*, *ii*) the *Digital Real-Time*

Simulator (DRTS), and *iii*) the *Power System Co-simulation Layer*. The rest of this section presents every single layer and its main components and the laboratory setups that are used to test the infrastructure functionalities.

A. GPS Synchronization Layer

This layer guarantees the complete infrastructure time synchronization by exploiting a GPS clock. The GPS is a global navigation satellite system that allows worldwide time synchronization by broadcasting a time reference clock synchronised to the GPS atomic clock technology, in addition to providing geolocation. The GPS clock is an hardware component that receives the GPS signal and synchronises its internal reference clock to the atomic time received by the GPS satellites without needing a nearby atomic clock, ensuring synchronisation among devices all over the world. Once synchronized with the GPS, this equipment offers different local synchronization protocols, such as IRIG-B, 1PPS, and the IEEE 1588 Precision Time Protocol (PTP).

Our infrastructure uses the IEEE1588 PTP to synchronize both internal reference clocks of the interconnected DRTS. By exploiting the PTP stack functionalities, the GPS clock sets its operation in master mode to control other slaves by broadcasting PTP packets on a Local Area Network (LAN). The end-user can choose among a set of standard PTP profiles (e.g. default profile) that serve different final uses. Moreover, the PTP stack offers two different delay mechanisms, namely, *i*) the End-to-End (E2E) and *ii*) the Peer-to-Peer (P2P), that provides PTP functionalities to the two homonymous types of transparent clocks. The E2E mechanism allows the calculation of the overall latency among the master and slave nodes ensuring the fastest synchronization with a low precision. Moreover, this delay mechanism ensures the most interoperable version of the PTP standard, reducing the limitations on hardware that can be used in the PTP network. The P2P delay mechanism instead allows a fine-grained and precise latency calculation of each hop of the network path between the master and the slave node. However, it reduces the interoperability of different hardware since they must implement the overall PTP standard protocol stack.

Furthermore, PTP offers two different protocols to allow communication among master and slave nodes: *i*) Layer 2 (i.e. IEEE802.3 or Ethernet) that ensures a fast synchronization in the same network segment, and *iii*) Layer 3 (i.e. IP) that allows the time synchronization of wider networks. Depending on the LAN configuration of the laboratory, the end-user could choose among the two layers. Apart from this configuration, the GPS clock is interconnected to the LAN using two RJ45 Ethernet interfaces, one serving the E2E, and the other the P2P delay mechanism.

B. DRTS Layer

This is the central layer of the proposed architecture. It enables the connection of two DRTS by exploiting a physical point-to-point bidirectional serial communication. This layer takes advantage of Aurora 8B/10B, a point-to-point full-duplex multi-mode optical fibre serial link with a high bandwidth of 2

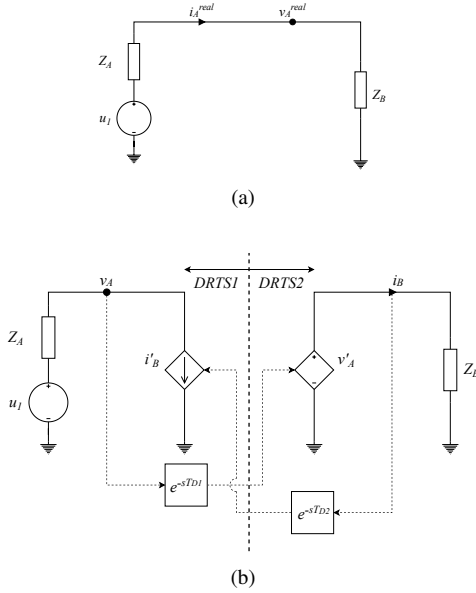


Fig. 2. A standalone electric system (a) consisting of an alternate current voltage source u_1 and two impedances Z_A and Z_B splitted via a SoS approach by exploiting ITM IA (b)

Gbps to 5 Gbps. As a matter of fact, Aurora is the fastest on-board protocol available on commercial DRTS, guaranteeing the lowest latency. To enable Aurora protocol, each DRTS must occupy one of the available Aurora Small-form Factor Pluggable (SFP) ports for the data exchange.

Each DRTS is also equipped with an IEEE1588 PTP synchronization boards since the time synchronization among the DRTSs involved in the proposed infrastructure is ensured by the IEEE1588 PTP. PTP boards are set as slave-only PTP nodes. Moreover, they are interconnected with the GPS synchronization layer with an RJ45 Ethernet cable to receive PTP packets coming from the PTP master node (i.e. GPS clock) and align the DRTS internal reference clock to the reference master clock. Finally, each interconnected DRTS implements its own logic to fulfil the real-time simulation of the assigned power subsystem by including simulation blocks that enables *i)* the Aurora link and *ii)* the PTP synchronization in the compiled models.

C. Power System Co-simulation Layer

The application of the logical SoS split of a PSUT is implemented in this layer via the ITM IA [27]. ITM is commonly adopted as interface to interconnect a physical Device Under Test (DUT) to a simulated Rest Of the System (ROS) in PHIL applications. It is the simplest choice to set up a PHIL system and it has been chosen to simply and efficiently split a PSUT into a source and load power subsystems modelled for each DRTS, where each resulting subsystem runs. The ITM IA illustrated in Figure 2b makes use of a controlled voltage source in the load circuit of the power subsystem to replicate the voltage v_A measured in the source circuit (i.e. v'_A) and a controlled current source in the source circuit of the power subsystem to replicate the current i_B measured in the load circuit (i.e. i'_B).

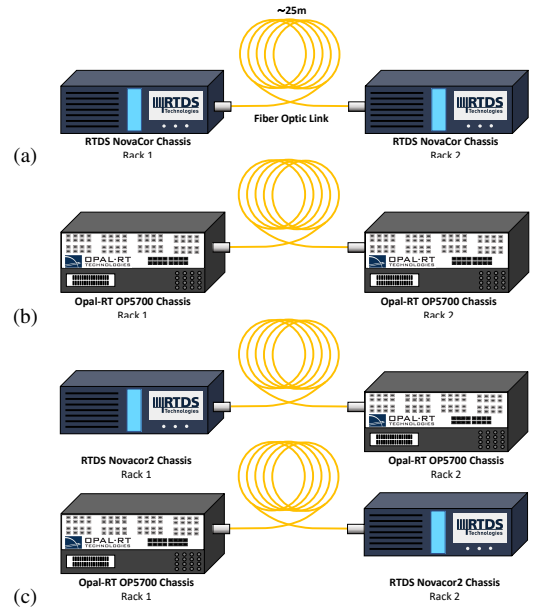


Fig. 3. Different configuration of the DRTS Layer: (a) RTDS-RTDS, (b) OPAL-OPAL, and (c) RTDS-OPAL in both directions.

Additionally, it applies a latency that is correlated to the delay experienced by the voltage and current value interchanged between DRTS racks 1 and rack 2 to affect the load power subsystem from the source power subsystem (i.e. T_{D1}) and vice versa (i.e. T_{D2}). The open-loop transfer function of the ITM IA described in Equation 1 is obtained by exploiting the ITM equivalent block diagram [28]:

$$G_{ol} = \frac{Z_A}{Z_B} e^{-s(T_{D1} + T_{D2})} \quad (1)$$

where Z_A is the source impedance; Z_B is the load impedance; T_{D1} is the latency affecting the voltage signal exchanged between the source and the load circuits; and T_{D2} is the latency affecting the current signal exchanged between the load and the source circuits. This equation describes the frequency stability of the ITM IA solution state space. By applying the Nyquist criterion, the stability of the PSUT is ensured when the ratio Z_A/Z_B is lower than 1. Furthermore, a large latency $T_{D1} + T_{D2}$ could provoke non-linearities (i.e. phase shifts) impacting the accuracy of the overall system in time and frequency domains, also in a stable region ensured by the Nyquist criteria.

D. Laboratory Setups

The proposed laboratory setups reduces significantly the latency between two DRTS chosen among the available commercial solutions for electric grid analysis, i.e. OPAL-RT OP5700 (OPAL) and RTDS Technologies NovaCor (RTDS). Following the architectural description in Figure 1, the GPS Synchronization Layer is managed by the Meinberg microSync HR102HQ GPS clock with an IEEE 1588-2008 v2 Default Layer 2 profile. This GPS clock offers four configurable Ethernet interfaces. Since RTDS and OPAL synchronization boards implement two different Transparent Clock (TC), port 2 have been configured to manage End-to-End (E2E) TC and

port 3 instead to manage Peer-to-Peer (P2P) TC. The GPS clock is the master of the IEEE1588 PTP network, and the two DRTS synchronization boards are slave to ensure a proper set up of the synchronization with the reference master clock.

RTDS racks must include the GTSYNC card to deal with the IEEE1588 PTP network. GTSYNC is a peripheral board interconnected with the core rack that enables different synchronisation techniques (e.g. IEEE 1588 PTP, 1PPS, IRIG-B). Moreover, the GTSYNC only accept P2P TC configuration of the IEEE1588 PTP stack. So, both RTDS racks' GTSYNC cards are connected with a RJ45 Ethernet cable to port 3 of the Meinberg GPS clock exploiting an Ethernet switch. During the design of the RSCAD draft, the GTSYNC block is a prerequisite to enable the synchronization of the GTSYNC card. OPAL instead provides the Oregano card that communicate with the core rack through PCIe bus. Like the GTSYNC, the Oregano card allows the same set of synchronization protocols. However, the TC configuration of the IEEE1588 PTP stack must be E2E. So, both OPAL racks' Oregano card are connected with a RJ45 Ethernet cable to port 2 of the GPS clock using the Oregano Syn1588 Ethernet switch to reduce latency of the PTP E2E packets. The time regulation schema is insignificant because both DRTSs evolve their simulations with a distinct time-regulating schema that maintains the correct event ordering while adhering to the appropriate real-time restriction. Because the proposed circuit for testing the connections is a basic source-load circuit, the source power circuit will cause the load power circuit simulation to begin. Because the IEEE 1588 PTP stack maintains the correct time synchronisation schema, results from DRTS racks are actually aligned using the internal clock time as a reference.

Since each commercial DRTS solution implements its own numerical solver and implementation of the Aurora 8B/10B, different configurations of the DRTS layer are proposed in Figure 3 to take into account each possible DRTS combination. Figure 3a presents two RTDS NovaCor that have been interconnected with an optical fiber cable of 25 m by leveraging on Aurora protocol. Figure 3b instead present two OPAL racks interconnected by an identical optical fiber cable of 25 m by leveraging on Aurora protocol. Finally, an RTDS rack and an OPAL rack have been coupled together as depicted in Figure 3c. This interconnection has been analysed in both directions, considering the rack 1 as the generation source and the rack 2 as the load of the proposed power system co-simulation scenario.

Figure 4 presents the sequence operation diagrams of a time step for both RTDS and OPAL are presented to highlight the management of the Aurora Read (RD) and Write (WR) operations. In Figure 4a, RTDS executes after each time step starting time an instantaneous WR operation followed by a RD. At the end of the RD, received variables are exchanged with the Control Signal Core that runs its operations in parallel with the Power System Component Cores. At the end of the time step, Control Signal Core and Power System Component Cores exchange both the control signal variable and the network signals representing voltages and currents. The OPAL sequence operation diagram instead is presented in Figure 4b. At the very beginning of each time step, the

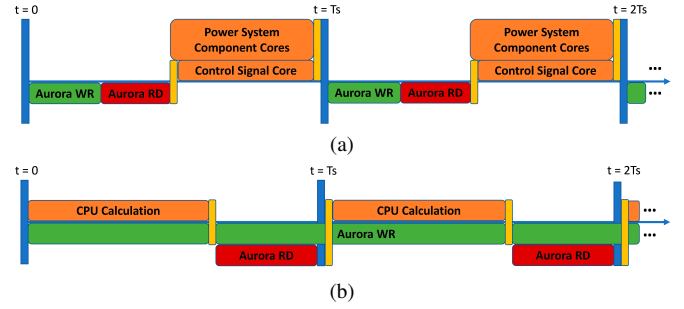


Fig. 4. Sequence operation diagrams of the FPGA Aurora Read (red blocks) and Write (green blocks) implementations in RTDS NovaCor (a), and OPAL-RT OP5700 (b), highlighting the data exchange between the FPGA and CPU operations (orange blocks).

FPGA exchanges data received by the Aurora RD operation in the previous step with the Central Processing Unit (CPU). Then, the CPU Calculation of the model is executed. After this operation, data are moved from the CPU to the FPGA. For each time step, WR operation is continuously transmitting data each $2.5\mu s$ and update the values exchanged once the CPU ends the operation of moving data to the FPGA. During the idle time at the end of this exchange, the FPGA also executes an Aurora RD operation that instead terminates at the end of the time step. The Aurora WR operation continues along the next time step by sending the same data received in the previous time step, until new data comes at the end of each CPU calculation operation. This workaround implemented in the FPGA bitstream of the OPAL enables a faster data transmission in hybrid configuration (see Figure 3c).

Aurora is enabled in RTDS chassis through RSCAD adding the *Aurora block*. It permits to select the specific SFP port, the assigned processor, the computation priority, the frame structure (i.e. exchanged control signals with maximum width of 128), and the sequence number blocking property. In OPAL systems instead, Aurora protocol is enabled through RT-LAB by selecting the proper SFP communication block that defines the FPGA DataIn and DataOut port numbers and enables a variable width of the exchanged signals with a maximum of 255 doubles exchanged. The Aurora link configuration (e.g. SFP transceiver port) instead is defined in the FPGA bitstream, that is uploaded during the scenario loading operations.

Finally, the Power System Co-simulation Layers implements the simple ITM circuit presented in Figure 2b by splitting the monolithic circuit (Figure 2a) into a source circuit A and a load circuit B. This simple scenario permits to precisely calculate the latency among the different configurations of the DRTS layer, and the accuracies in time and frequency domains of the co-simulated results by comparing them with the standalone monolithic results.

IV. EXPERIMENTAL RESULTS

This section presents the experimental results of the simple electric circuit applied to the proposed Digital Real-Time Co-simulation Infrastructure. The circuit in Figure 2b has been implemented in both DRTSs (i.e. RTDS NovaCor and OPAL-RT OP5700) by exploiting RSCAD and RT-LAB software. In source part A of Figure 2b, u_1 is a single phase voltage source

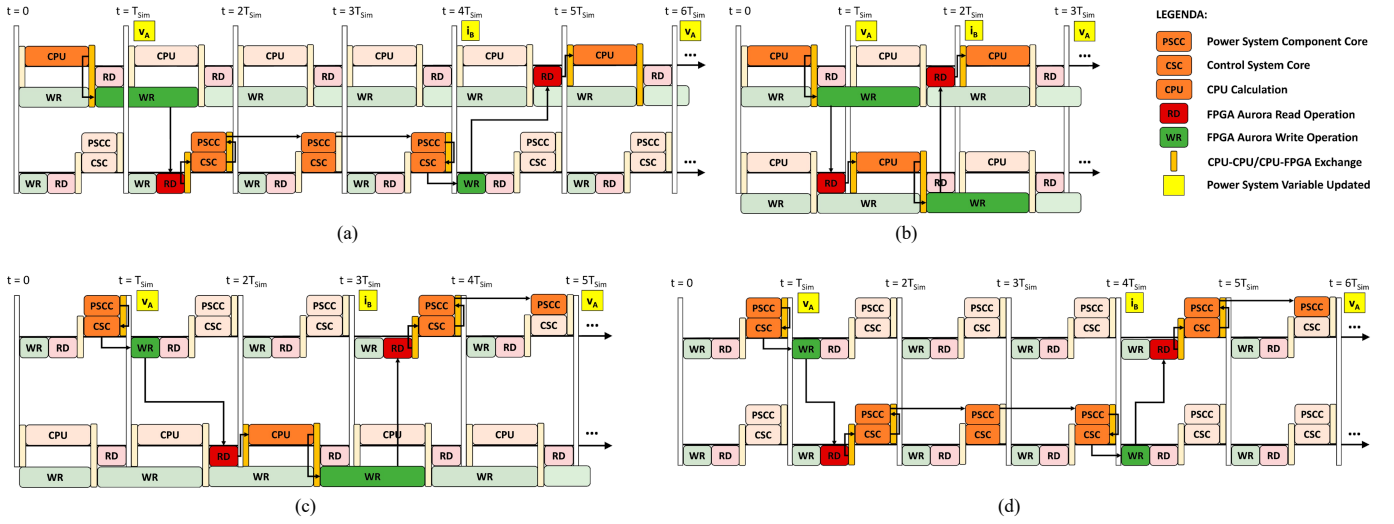


Fig. 5. Sequence Operation Diagrams for the different DRTS configurations: RTDS-RTDS (a), OPAL-OPAL (b), RTDS-OPAL (c), and OPAL-RTDS (d).

with an amplitude of 100 kV and a nominal frequency of 50 Hz. Impedance Z_A is set to 50Ω . v_A is retrieved employing a metering point to send its values each time step to load part B through the Aurora link. The load part B of Figure 2b receives the voltage signal v_A via the Aurora link that causes the controlled voltage generator v'_A to induce a delayed v_A signal. Two different Z_B values, namely 50.5Ω and 500Ω , are adopted to test the ITM regions *i*) $Z_A/Z_B \approx 1$, and *ii*) $Z_A/Z_B \ll 1$, respectively. To return feedback to the source part A , a metering point retrieves i_B current to then send it back through the Aurora link. This value is received by source part A and imposed through the controlled current source i'_B . The ITM IA circuit has been tested for all the possible combinations, namely, *i*) RTDS-RTDS, *ii*) OPAL-OPAL, *iii*) RTDS-OPAL, and *iv*) OPAL-RTDS (see Figure 3). All the configurations exploit a 25-meter long standard full-duplex multi-mode optical fibre cable as physical media to interconnect both racks.

In the following subsections, we discuss the experimental results on: *i*) the *ITM IA Latency Calculation* that describes the time step contributions to the overall latency experimented by the ITM IA circuit for each of the Digital Real-Time Simulation layer configurations, *ii*) the *ITM IA Time-domain Accuracy Analysis* that compares the standalone voltages signals with the co-simulated ITM IA case in the stable region ($Z_B = 500 \Omega$) and near the instability region ($Z_B = 50.5 \Omega$) for each configuration of the infrastructure, and *iii*) the *ITM IA Frequency-domain Accuracy Analysis* that, similarly to the time-domain case, compares the standalone frequential contents with the co-simulated solution ones for both regions and all infrastructure configurations. For each section, the time step duration T_{sim} has been changed from $20 \mu s$ to $500 \mu s$ to highlight possible dependencies from the time step duration that could influence the overall latency.

A. ITM IA Latency Calculation

For each infrastructure configuration, the overall observed latency the ITM IA circuit solution is described using its

sequence operation diagrams in Figure 5. More in-depth, these sequence diagrams describe the contribution of each single time-step, highlighting internal operations executed by each DRTS and the data exchange among the interconnected racks. Depending on the infrastructure configuration, these operations may or may not contribute to the overall latency represented by $T_{D1} + T_{D2}$ in Equation 1. The generated phase shifts impact both time and frequency-domain accuracy of the ITM IA circuit solution.

1) *RTDS-RTDS*: By exploiting RSCAD software libraries, Aurora blocks are set with the sequence number blocking configuration activated on port 24 for both RTDS racks. The overall calculated latency by the ITM IA application is $5T_{sim}$ for all T_{sim} values. The contributions are depicted in the sequence operation diagram in Figure 5a. From $t = 0$ to $t = T_{sim}$, the Power System Component Core (PSCC) of RTDS rack 1 calculates v_A and passes its value to the Control System Core (CSC). From $t = T_{sim}$ to $t = 2T_{sim}$, rack 1 retrieves v_A value from the CSC and send it through the Aurora link by executing a write operation (WR). In the same time interval, RTDS rack 2 receives v_A value from the Aurora link with a read operation (RD) and gives it to the Control System Core that is in charge to send its value to the PSCC at the end of the time interval. From $t = 2T_{sim}$ to $t = 4T_{sim}$, rack 2 calculates the current i_B by applying v_A voltage to the controlled voltage source v'_A and, finally, moves i_B from the PSCC to the CSC. These operations take $2T_{sim}$ in total. From $t = 4T_{sim}$ to $t = 5T_{sim}$, rack 2 retrieves the i_B value from the CSC and executes an Aurora WR operation. In the same time interval, rack 1 receives its value by executing an Aurora RD operation and passes its value to the CSC. To conclude, the effect of i_B on v_A calculation requires another T_{sim} to take effect on source part A of the circuit in Figure 2b. The ITM IA latency is calculated from the first v_A calculation in rack 1 at $t = T_{sim}$ to the effect of i_B to v_A calculation at $t = 6T_{sim}$, resulting in a total of $5T_{sim}$.

2) *OPAL-OPAL*: By exploiting RT-LAB software libraries, the SFP block is integrated into both models of the ITM

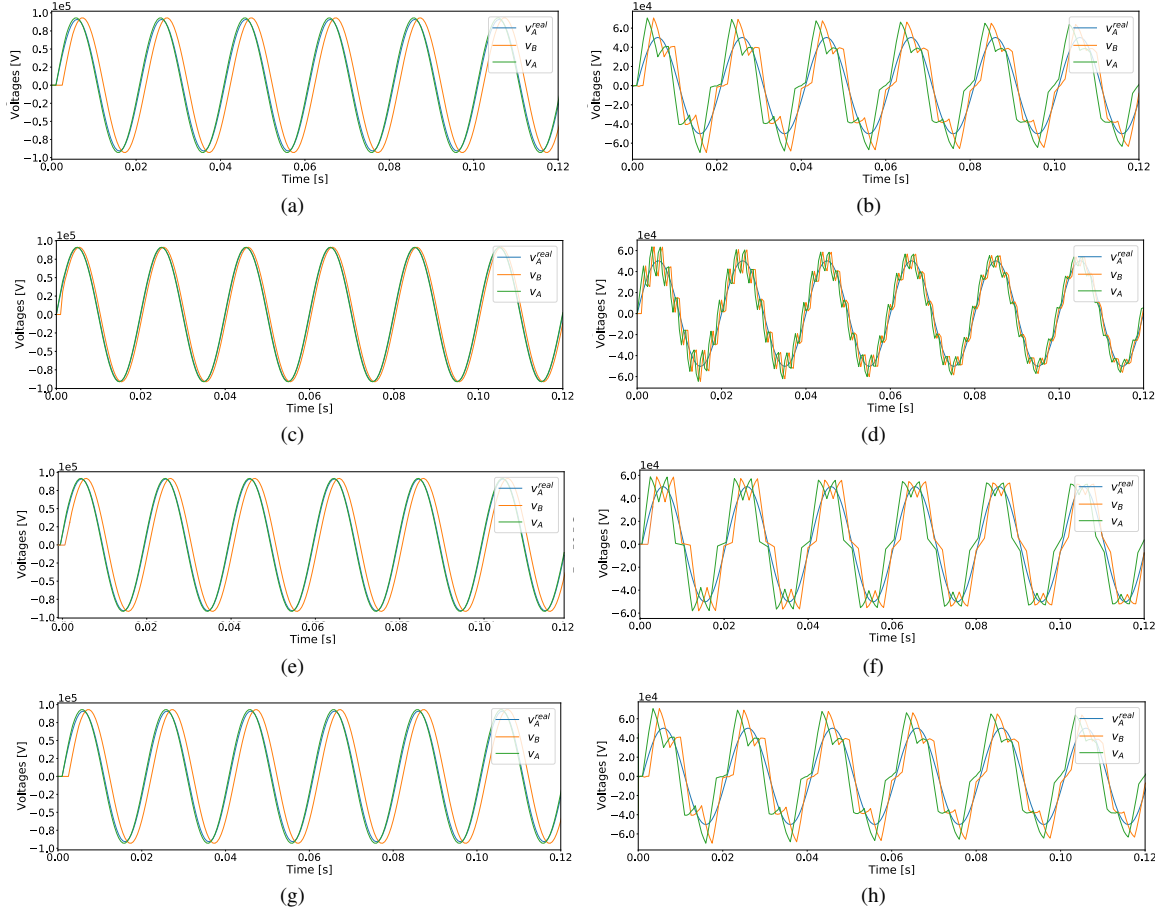


Fig. 6. Comparison of voltage signals in time-domain for the standalone electric system (blue line) vs ITM IA (green and orange lines) for $T_s = 500 \mu s$ in the region $Z_A/Z_B \ll 1$ (a, c, e, g) and near the region $Z_A/Z_B \approx 1$ (b, d, f, h) for the different DRTS configurations: RTDS-RTDS (a, b), OPAL-OPAL (c, d), RTDS-OPAL (e, f), and OPAL-RTDS (g, h).

circuit. SFP blocks are set on port SFP00 for both OPAL racks. The calculated latency is $2T_{Sim}$ for all T_{Sim} values and its contributions are depicted in Figure 5b. From $t = 0$ to $t = T_{Sim}$, the Control Processing Unit (CPU) of the OPAL rack 1 calculates v_A and provides its value to the FPGA that executes the Aurora WR operation. In the same time interval, the FPGA of the OPAL rack 2 receives v_A value by executing the Aurora RD operation. Right at the beginning of the time interval between $t = T_{Sim}$ and $t = 2T_{Sim}$, rack 2 moves v_A value from the FPGA to the CPU. Subsequently, the CPU of rack 2 executes the calculation to retrieve the current i_B , moves its value to the FPGA, and sends it through the Aurora link with an Aurora WR operation. To conclude, in this time interval, rack 1 receives i_B value and stores it in the FPGA by executing an Aurora RD operation. In the last time intervals from $t = 2T_{Sim}$ to $t = 3T_{Sim}$, i_B moves from the FPGA to the CPU to allow the calculation of the effect on v_A on the source circuit. v_A value is updated at the end of this time interval as a result of the circuit numerical solution. So, the ITM IA latency is calculated from the first v_A calculation in rack 1 at $t = T_{Sim}$ to the effect of i_B to v_A calculation at $t = 3T_{Sim}$, resulting in a latency of $2T_{Sim}$.

3) *RTDS-OPAL*: The source circuit of Figure 2b in the RSCAD draft and load counterpart in the RT-LAB model of the two previous cases are used in this first hybrid configuration. The physical interconnection of the optical fiber link has been changed from port 23 of the RTDS rack 1 to port SFP01 of the OPAL rack 2. The overall latency is $4T_{Sim}$ for all T_{Sim} values. The contributions are presented in Figure 5c. From $t = 0$ to $t = 2T_{Sim}$, RTDS rack 1 executes same operations described in the previous Paragraph IV-A1, presenting as a result v_A at $t = T_{Sim}$. OPAL rack 2 receive v_A value by executing an Aurora RD operation at the end of the time interval from $t = T_{Sim}$ to $t = 2T_{Sim}$. At the very beginning of the time interval from $t = 2T_{Sim}$ to $t = 3T_{Sim}$, OPAL rack 2 moves v_A value from the FPGA to the CPU and, then, executes i_B calculation. In the same time interval, the current i_B is moved from the CPU to the FPGA to finally execute the Aurora WR operation. Aurora WR lasts till the next time interval from $t = 3T_{Sim}$ to $t = 4T_{Sim}$, where RTDS rack 1 reads i_B current and passes to the CSC its value, concluding the interval by pass through i_B to the PSCC. Finally, RTDS rack 1 calculates v_A in the last time interval from $t = 4T_{Sim}$ to $t = 5T_{Sim}$. The ITM IA results in a latency of $4T_{Sim}$ by considering from the first v_A calculation in RTDS rack 1 at

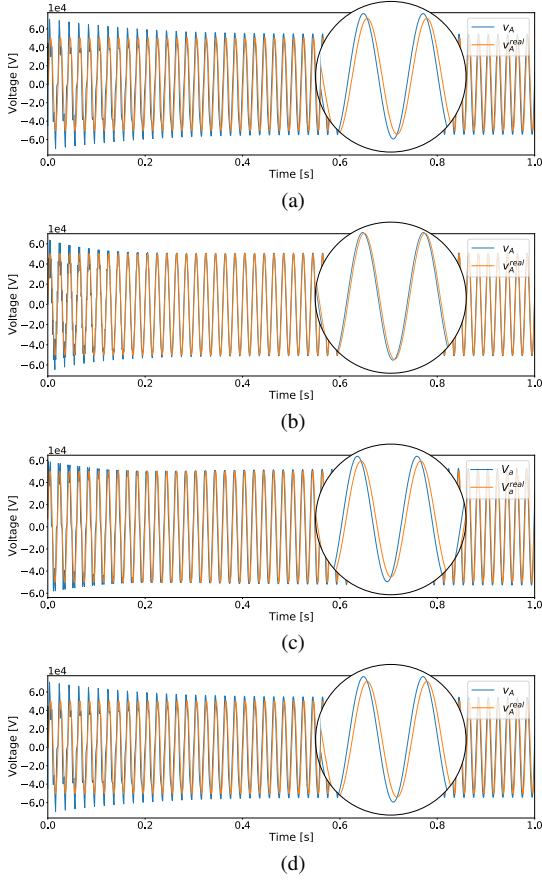


Fig. 7. Comparison of voltage signals in time-domain for the standalone electric system (orange line) vs ITM IA transients (blue line) for $T_s = 500 \mu s$ near the region $Z_A/Z_B \approx 1$ for the different DRTS configurations: RTDS-RTDS (a), OPAL-OPAL (b), RTDS-OPAL (c), and OPAL-RTDS (d).

$t = T_{Sim}$ to the effect of i_B to v_A calculation at $t = 5T_{Sim}$.

4) **OPAL-RTDS:** The source circuit in the RT-LAB draft and load circuit in the RSCAD model of the first two cases are used in this second hybrid configuration. The physical interconnection of the optical fiber link has been changed from port SFP00 of the OPAL rack 1 to port 24 of the RTDS rack 2. The ITM IA latency results $5T_{Sim}$ for all T_{Sim} values. As in previous cases, contributions are described by presenting the configuration's sequence operation diagram in Figure 5d. From $t = 0$ to $t = T_{Sim}$, OPAL rack 1 executes the same operations described in the previous Paragraph IV-A2. However, RTDS rack 2 reads v_A value from the Aurora link in the next time interval from $t = T_{Sim}$ to $t = 2T_{Sim}$. From $t = T_{Sim}$ to $t = 5T_{Sim}$, RTDS rack 2 executes the same operations of the previous Paragraph IV-A1. So, OPAL rack 1 retrieves the i_B value at the end of the time interval from $t = 4T_{Sim}$ to $t = 5T_{Sim}$. In the last interval, the CPU in OPAL rack 1 receives from the FPGA i_B value, calculates the v_A effect, and, finally, presents its value as a result. The overall calculated latency is $5T_{Sim}$, considering from the first v_A calculation in OPAL rack 1 to the effect of i_B to v_A calculation at $t = 6T_{Sim}$.

B. ITM IA Time-domain Accuracy Analysis

The time-domain analysis demonstrates that our infrastructure obtain good accuracy of the co-simulated solution. We compared the results of our distributed co-simulation system with a monolithic solution that runs the standalone circuit in Figure 2a. The results in this subsection are achieved only for a time step duration $T_{Sim} = 500 \mu s$ (i.e. worst-case scenario). This scenario is considered as a limit case since normal EMT analysis for electric grid scenario exploits a time step duration of around $50 \mu s$. The standalone electric system in Figure 2a runs simultaneously to the ITM scenario to fetch the standalone voltage and current, namely v_A^{real} and i_A^{real} . Results in Figure 6 are presented only for voltages v_A^{real} (blue line), v_A (green line), and v_B (orange line) since currents are in phase, as the power factor of a purely resistive circuit is 1. Voltages v_A^{real} , v_A , and v_B have been analysed for the two Z_B values that represent the stable ITM case (i.e. $Z_B = 500 \Omega$) and near the instability region of the ITM circuit (i.e. $Z_B = 50.5 \Omega$). Finally, the instability transient generated by case $Z_B = 50.5 \Omega$ is presented in Figure 7. The results demonstrate that applying a T_{Sim} lower than $500 \mu s$ ensures good time accuracy for both regions, reproducing with high fidelity the monolithic solution.

1) **RTDS-RTDS:** The case $Z_B = 500 \Omega$ is presented in Figure 6a. v_A overlies v_A^{real} confirming that the ITM application is capable of reproducing correctly the standalone simulation with a slight rise of 2.28% of v_A voltage peak caused by the round trip latency of the ITM circuit. v_B follows v_A , delayed of $1500 \mu s$ that is equal to $3T_{Sim}$. This is T_{D1} latency of the ITM open-loop function G_{ol} in Equation 1. This latency is described in the previous subsection IV-A1 and is composed of the first three time step contributions.

The case $Z_B = 50.5 \Omega$ instead is presented in Figure 6b and presents major instabilities due to the phase shift generated by the ITM application. In particular, the distortions are generated by the round trip latency $5T_{Sim}$ equal to $2500 \mu s$ and the Z_A/Z_B ratio equal to 0.9900 , near the instability region of the ITM open-loop function G_{ol} in Equation 1. v_A initial peak exceed 40.72% compared to v_A^{real} . v_B follows the v_A trend with a latency of $1500 \mu s$. Similarly to the stable ITM case, it results in $3T_{Sim}$. In Figure 7a, the distortion transient lasts 0.4 s eventually stabilising with a 7.92% rise compared to the voltage rise of the case $Z_B = 500 \Omega$. Finally, v_A presents a non-linear distortion of the sine due to the ITM application near the instability region.

2) **OPAL-OPAL:** The case $Z_B = 500 \Omega$ is presented in Figure 6c. v_A overlies v_A^{real} with an insignificant rise of 0.37% compared to the v_A voltage peak caused by the smallest round trip latency between the different infrastructure configurations equal to $2T_{Sim}$. v_B follows v_A , delayed of $500 \mu s$ that is equal to $1T_{Sim}$. This latency is described in Section IV-A2 and is composed of the first time step contribution. The case $Z_B = 50.5 \Omega$ instead is presented in Figure 6d and still presents major instabilities. In this case, the distortions are denser than in the previous case in Section IV-B1 due to the higher frequency of the phase shift generated by the round trip latency $2T_{Sim}$ and the Z_A/Z_B ratio. v_A initial peak exceeds

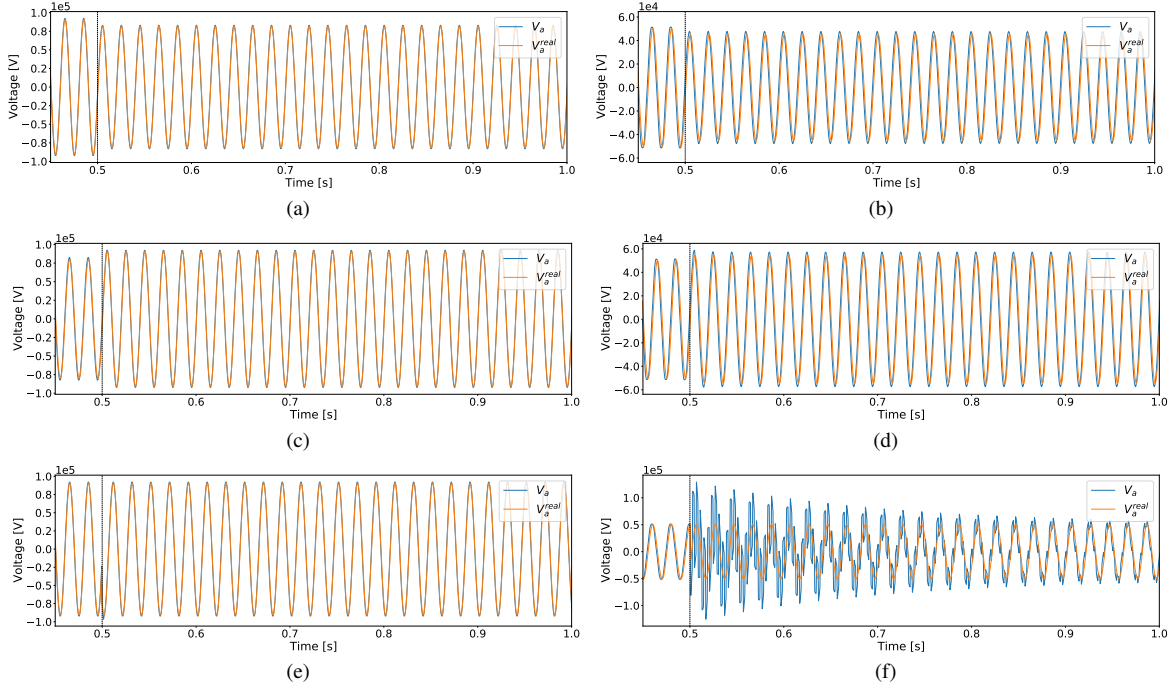


Fig. 8. Comparison of voltage signals in time-domain for the standalone electric system (*orange* line) vs ITM IA transients (*blue* line) for $T_s = 500 \mu s$ in RTDS-OPAL configuration in the region $Z_A/Z_B \ll 1$ (a, c, e) and near the region $Z_A/Z_B \approx 1$ (b, d, f), with different imposed conditions, namely the voltage source amplitude transient (a, b), the load impedance transient (c, d), and the voltage source phase shift transient (e, f)

26.56% compared to v_A^{real} . v_B follows the v_A trend with a latency of $500 \mu s$. Similarly to the stable ITM case, it results correctly in $1T_{Sim}$. In Figure 7b, the distortion transient lasts $0.16 s$ stabilising the result with an 1.25% rise compared to v_A^{real} . To conclude, v_A does not present particular non-linear distortion.

3) *RTDS-OPAL*: The case $Z_B = 500 \Omega$ is presented in Figure 6e. v_A follows v_A^{real} with a 0.83% rise of the v_A voltage peak. v_B follows v_A , delayed of $1000 \mu s$ that is equal to $2T_{Sim}$ confirming the description of the sequence operation diagram in Section IV-A3. The case $Z_B = 50.5 \Omega$ instead is presented in Figure 6f and presents similar instabilities to the previous cases. The distortions generated by the round trip latency $4T_{Sim}$ and the Z_A/Z_B ratio produce a v_A initial peak with a rise of 16.97% compared to v_A^{real} . v_B follows the v_A trend with a latency of $1000 \mu s$, which results correctly $2T_{Sim}$. In Figure 7c, the distortion transient lasts $0.32 s$ stabilising the result with a 5.14% rise compared to v_A^{real} . Lastly, v_A presents non-linear distortion smaller than case presented in Section IV-B1 due to the lower latency experimented by the ITM IA circuit.

4) *OPAL-RTDS*: The case $Z_B = 500 \Omega$ is presented in Figure 6g. This case presents results similar to case in Section IV-B1. However, v_A overlies v_A^{real} with a smaller rise equal to 1.47% . v_B follows v_A , delayed of $1500 \mu s$ that is equal to $3T_{Sim}$. The case $Z_B = 50.5 \Omega$ instead is presented in Figure 6h and presents the same instabilities as the case presented in Section IV-B1. In particular, v_A initial peak exceeds 40.72% compared to v_A^{real} . v_B follows v_A with the latency of $1500 \mu s$, confirming the $3T_{Sim}$ latency expectation.

In Figure 7d, the distortion transient lasts $0.4 s$ stabilising the result with a 7.92% rise compared to v_A^{real} . Finally, v_A presents the same non-linear distortion as the case presented in Section IV-B1.

C. ITM IA Time-domain Transient Accuracy Analysis

A transient condition could present accuracy issues in both the time domain and frequency domain. Three different transient conditions are proposed in the worst-case scenario $T_s = 500 \mu s$ to determine the accuracy in the stability region (i.e. $Z_B = 500 \Omega$) and near the instability region (i.e. $Z_B = 50.5 \Omega$) of the proposed infrastructure. For the sake of simplicity, only the case RTDS-OPAL is presented which presents an intermediate latency of $4T_{Sim}$. Results are presented in Figure 8 for time-domain accuracy in the three transient conditions, namely: *i*) the Voltage Source Amplitude Transient, *ii*) the Load Impedance Transient, and *iii*) the Voltage Source Phase Shift Transient.

1) *Voltage Source Amplitude Transient*: The voltage source v_S is modified after $0.5 s$ from the nominal value $100 kV$ to $90 kV$. In the stability region in Figure 8a, v_A follows v_A^{real} with an 1.47% rise of the v_A voltage peak. Near the instability region in Figure 8b, v_A instead presents similar instabilities to the initial transient. In the transient condition, the distortions generated by the round trip latency $4T_{Sim}$ and the Z_A/Z_B ratio produce a v_A initial peak with a rise of 5.73% compared to v_A^{real} . The distortion transient is negligible and stabilizes instantly the result with an 5.15% rise compared to v_A^{real} .

2) *Load Impedance Transient*: The load impedance Z_B is modified after $0.5 s$ i) from 200Ω to 500Ω in the stability

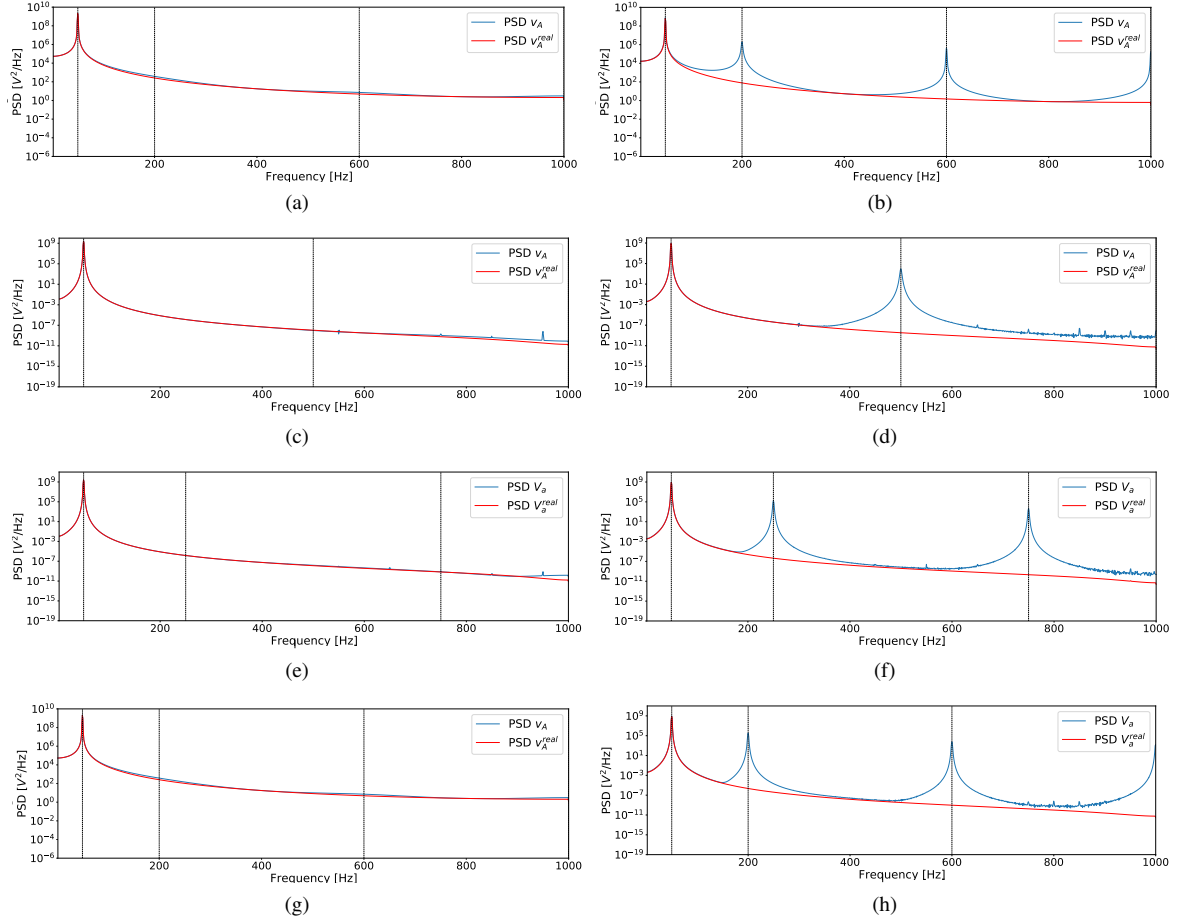


Fig. 9. Comparison of voltage PSD in frequency-domain for the standalone electrixt system (*red* line) vs ITM IA (*blue* line) for $T_s = 500 \mu s$ in the region $Z_A/Z_B \ll 1$ (a, c, e, g) and near the region $Z_A/Z_B \approx 1$ (b, d, f, h) for the different DRTS configurations: RTDS-RTDS (a, b), OPAL-OPAL (c, d), RTDS-OPAL (e, f), and OPAL-RTDS (g, h).

region, and ii) from 50.5Ω to 60Ω near the instability region. In the stability region in Figure 8c, v_A follows v_A^{real} with an 1.47% rise of the v_A voltage peak. Near the instability region in Figure 8d, v_A instead presents similar instabilities to the initial transient but is reduced by the fact that we are moving far away from the instability region. In the transient condition, the distortions generated by the round trip latency $4T_{Sim}$ and the Z_A/Z_B ratio produce a v_A initial peak with a rise of 7.86% compared to v_A^{real} . The distortion transient lasts 1 cycle stabilizing the result with an 5.05% rise compared to v_A^{real} .

3) *Voltage Source Phase Shift Transient*: In this case, a 90° phase shift is introduced in the voltage source v_S at $0.5s$ from the nominal value. In the stability region in Figure 8e, v_A follows v_A^{real} with an instantaneous transient peak that increases 6.15% with respect to the nominal value. After the transient in the steady state condition, v_A follows v_A^{real} with an 1.43% rise of the v_A voltage peak. Near the instability region in Figure 8f, v_A instead presents similar instabilities to the initial transient. During the transient condition, the distortions are generated by the round trip latency $4T_{Sim}$ and the impedance ratio of the system, i.e., the stiffness. Mathematically, this is Z_B/Z_A and in this case is approx 1.0,

i.e., not stiff. Hence, changes to the load or source magnitude or angle have a significant impact on resulting voltage. As a result, v_A shows an initial peak with a rise of 157.18% compared to v_A^{real} . The distortion transient lasts almost 27 cycles, before stabilising to a new result with an 5.14% rise compared to v_A^{real} .

D. ITM IA Frequency-domain Accuracy Analysis

The frequency-domain analysis allows a complete understanding of the effects of the latency experimented by applying the ITM IA circuit to the proposed co-simulation infrastructure. This analysis is obtained by applying Welch's method for the Power Spectral Density (PSD) estimation applied to voltage signals v_A^{real} and v_A for both Z_B values to compare the monolithic implementation w.r.t. the co-simulated one. As depicted in Section IV-B, the latency experimented from the different configurations of the proposed infrastructure gives rise to non-linearity in the time-domain results generated by the phase shift caused by the ITM IA application. The highest effect is resulting near the instability region (i.e. $Z_B = 50.5 \Omega$) for all configurations.

In fact, the phase shift time-domain effect near the instability region is similar to a triangle wave trend summed to

the original voltage signal. Applying additive synthesis, the triangle is approximated in time domain summing odd harmonics of the fundamental sine wave of frequency f_Δ while multiplying every other odd harmonic by -1 and multiplying the amplitude of the harmonics by 1 over the square of their mode number n as described in Equation 2:

$$x_{triangle}(t) = \frac{8}{\pi^2} \sum_{i=0}^{N-1} (-1)^i n^{-2} \sin(2\pi f_\Delta n t) \quad (2)$$

Because the phase shift effect changes sign for each round trip latency of the open-loop function G_{ol} , we may consider the fundamental sine wave period of the resulting triangular wave T_Δ in Equation 1 twice the round trip delay. Then, the fundamental frequency f_Δ is equal to the inverse of the period T_Δ . So, a spike in f_Δ will be always present for the case $Z_B = 50.5 \Omega$. Following the approximation in the time-domain with additive synthesis, the other frequency components of the triangle wave will be the odd harmonics $3f_\Delta$, $5f_\Delta$, and so on. Since the resolution of Welch's method for the PSD estimation is limited by the sampling period T_{Sim} to 1 kHz, some cases will present also the odd harmonics depending on the round trip latency. As matter of fact, the higher is the round trip latency, the lower is f_Δ and consequently its odd harmonics.

1) *RTDS-RTDS*: v_A PSD accurately overly v_A^{real} peak at $f = 50$ Hz (i.e. the power supply frequency) for $Z_B = 500 \Omega$ without any other frequency disturbances, as depicted in Figure 9a. So, the standalone frequency content result is correctly replicated. The case $Z_B = 50.5 \Omega$ in Figure 9b instead presents v_A PSD with the former peak at $f = 50$ Hz and three frequency peaks at $f = 200$, 600 and 1000 Hz. Since the round trip latency calculated in the previous Section IV-A1 is $5T_{Sim}$ and following the previous assumption, T_Δ results $10T_{Sim}$ and f_Δ is exactly 200 Hz that is the fundamental sine wave component of the triangle wave. Consequently, the frequencies of the odd harmonics are 600 Hz, 1000 Hz, and so on. These three frequency components are appreciated in Figure 9b. Moreover, they can be noticed also in Figure 9a (i.e. $Z_B = 500 \Omega$) but their effect is mitigated by the magnitude of Z_A/Z_B equal to 0.1 .

2) *OPAL-OPAL*: v_A PSD accurately overly v_A^{real} peak at $f = 50$ Hz (i.e. the power supply frequency) for $Z_B = 500 \Omega$ in Figure 9c. For $Z_B = 50.5 \Omega$, two main components result from the PSD estimation as depicted in Figure 9d: i) $f = 50$ Hz which is the former power supply frequency, and ii) $f_\Delta = 500$ Hz that is the fundamental sine wave of the triangle wave spectrum. The round trip latency of the ITM application for the OPAL-OPAL interconnection is $2T_{Sim}$, resulting in a $T_\Delta = 4T_{Sim}$ that confirms the PSD component of $f_\Delta = 500$ Hz. Since the PSD is limited to 1 kHz, the odd harmonics $3f_\Delta$, $5f_\Delta$, and so on, of the triangle wave approximation cannot be appreciated.

3) *RTDS-OPAL*: The stable ITM application for $Z_B = 500 \Omega$ correctly reproduce v_A^{real} peak at $f = 50$ Hz in the v_A PSD represented in Figure 9e. For $Z_B = 50.5 \Omega$ instead two harmonics of $f = 250$ Hz and $f = 750$ Hz can be appreciated as well as the former power supply frequency $f = 50$ Hz,

as depicted in Figure 9f. Following the additive synthesis hypothesis and considering the round trip latency of the RTDS-OPAL interconnection equal to $4T_{Sim}$, T_Δ results $8T_{Sim}$ and so the calculated fundamental sine frequency of the triangle wave confirms the former peak at $f = 250$ Hz and its first odd harmonic at $f = 750$ Hz.

4) *OPAL-RTDS*: Since for this case, the round trip latency is equal to case in Section IV-D1 (i.e. $5T_{Sim}$), we can assume similar observations on the frequency-domain accuracy. For $Z_B = 500 \Omega$ in Figure 9g, v_A PSD closely reproduces v_A^{real} peak at $f = 50$ Hz without disturbances. For $Z_B = 50.5 \Omega$, the former power supply peak is reproduced with three harmonic components at $f = 200$, 600 and 1000 Hz as depicted in Figure 9h. With the same assumptions of case in Section IV-D1, the fundamental sine frequency of the triangle wave is exactly 200 Hz and its visible odd harmonics are the former peaks at $f = 600$ and 1000 Hz.

V. CONCLUSION

In this work, we proposed a Locally Distributed Digital Real-Time Co-simulation Infrastructure to connect two DRTS by means of Aurora 8B/10B protocol. The infrastructure is capable of reducing the communication latency experienced by the data exchange among DRTS, allowing to run EMT analysis of a SoS co-simulated power system scenario. Moreover, the infrastructure offers IEEE1588 PTP standard as a synchronization method to avoid misalignment of the real-time executions, permitting to compare results coming from each single DRTS for logging and post-processing purpose.

The infrastructure proposes the PHIL ITM IA as the most simple method to split the PSUT into sub-models each one runs by a different interconnected DRTS, following a SoS approach. Similar to a PHIL set-up, ITM IA determines a stable and accurate numerical solution of a power system within the following limitation: $Z_A/Z_B \ll 1$. Furthermore, using the Aurora protocol helps in bringing down the effect of latency on the ITM IA and consequently enhancing its stability and accuracy. The communication latency is calculated exploiting the ICT infrastructure of DRTSs under analysis, highlighting the internal data exchange among CPU and FPGA to correctly manage Aurora 8B/10B communication protocol. The simple PSUT has been run in a scenario with a time step duration of $500 \mu s$ (i.e. worst-case) to evaluate the accuracy in time domain of the solution in both regions $Z_A/Z_B \ll 1$ and $Z_A/Z_B \approx 1$ of the ITM IA. The proposed infrastructure results are in both regions acceptable in accuracy and reproduce the performance of the standalone electric system. For instance, the amplitude accuracy of the stable cases is around 1.4% with a negligible transient usually shorter than one cycle. In the unstable region, the amplitude accuracy instead suffers from transients that can last up to 27 cycles, depending on the specific case, with a steady state over peak error of almost 5% . Since EMT analysis normally runs with smaller time steps, around $50 \mu s$, we conclude that our infrastructure allows the EMT analysis of larger scenario, enhancing the scalability of PSUT. It is worth noting that a smaller time step would relax the constraint $Z_A/Z_B \ll 1$, allowing to operate in $Z_A/Z_B \approx 1$ region.

Future works will involve the application of a real Smart Grid scenario to the proposed infrastructure and comparing its accuracy on the system dynamics with a standalone simulation.

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