Fast LDO Simulations via Parameter-Varying Linearized Macromodels

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Tommaso Bradde, Stefano Grivet-Talocia
Dept. Electronics and Telecommunications, Politecnico di Torino, Italy
tommaso.bradde@polito.it, stefano.grivet@polito.it

***Abstract*—An approach for generating time-varying linearized macromodels of analog circuit blocks is presented. These models can be used to perform fast small-signal analyses characterized by nonstationary operating conditions, thanks to their certified stability. We validate the proposed approach by performing post-layout simulations of a Low DropOut (LDO) voltage regulator, in view of power integrity assessment applications.**

I. Introduction

Analog Circuit Blocks (CBs) are fundamental components in virtually all electronic systems. When considered in advanced design stages, the behavior of these components is properly described in terms of large equivalent netlists that must take into account both the semiconductor models and the electrical characterization of the parasitics due to the circuit layout and packaging. As the number of CBs involved in modern Systems-on-Chip (SoC) and Systems-in-Package (SiP) is usually large, straight exploitation of such accurate yet complex descriptions within system-level simulations is often unfeasible due to an excessive computational cost. Thus, the availability of behavioral models for this kind of components is highly desirable [1], [2].

This contribution focuses on the generation of macromodels for CBs operating under small-signal conditions, characterized by a nonstationary working point. The latter can be determined, e.g., by changes of the system operation mode performed for the sake of energy management. The approach relies on the generation of a Linear-Parameter-Varying (LPV) reduced order model that approximates the local dynamics of the original system around its dynamic working point, as it evolves within prescribed limits [3]. The model is generated starting from samples of the circuit small-signal transfer function, retrieved in correspondence of a finite number of admissible bias configurations. Model parameterization is performed at runtime, by extracting the low frequency components of the electrical quantities at the circuit interface ports, which determine the instantaneous bias condition. Suitable numerical constraints are embedded in the model generation to guarantee the stability of the resulting LPV system for arbitrary working point trajectories.

The method is applied to perform a fast post-layout simulation of a LDO circuit design, in view of possible applications for advanced power integrity optimization and assessment. Experimental evidence show that the proposed models are accurate and guarantee up to $50\times$ speedup in transient simulations.

II. Problem Setting

We consider a mildly nonlinear analog circuit block accessible from P electrical interface ports, whose behavior is described by the nonlinear differential equations

$$\begin{aligned} \dot{\xi}(t) &= F(\xi(t), u(t)), \\ \eta(t) &= G(\xi(t), u(t)), \end{aligned} \tag{1}$$

being $u(t), \eta(t) \in \mathbb{R}^P$ the system input and output signals, and $\xi(t) \in \mathbb{R}^N$ is the system state vector, with N large. F, G are nonlinear differentiable maps not known in closed form, but encrypted in an available SPICE netlist.

We want to obtain a reduced order behavioral model of (1) for small-signal analyses characterized by nonstationary working conditions, compatible with the input decomposition

$$u(t) = U_0(t) + \tilde{u}(t), \tag{2}$$

satisfying the following assumptions

1) $\tilde{u}(t)$ is a small-signal component with $\tilde{u}(0) = 0$.
2) $U_0(t)$, henceforth denoted as *bias component*, attains values within a (not necessarily small) hyper-rectangle

$$U_0(t) \in \mathcal{U}_0 = [a_1, b_1] \times \cdots \times [a_P, b_P], \ \forall t \geq 0. \tag{3}$$

Additionally, at each $t^* \geq 0$, there exists a small constant $\delta_\xi \geq 0$ such that

$$||\xi(t^*) - \Xi_0(t^*)||_2 \leq \delta_\xi, \tag{4}$$

being $\Xi_0(t^*)$ the unique aymptotically stable equilibrium point satisfying

$$\begin{aligned} 0 &= F(\Xi_0(t^*), U_0(t^*)), \\ Y_0(t^*) &= G(\Xi_0(t^*), U_0(t^*)). \end{aligned} \tag{5}$$

Under the above assumptions, since (5) admits an unique solution, at each time instant system (1) operates in the neighborhood of the operating point determined solely by the instantaneous value of $U_0(t)$. This condition is practically verified when the bias component varies slowly with respect to the dynamics of the circuit of interest. Also, when (4) and (5) hold, the output of (1) can be decomposed as

$$\eta(t) = Y_0(t) + \tilde{\eta}(t) \tag{6}$$

where $Y_0(t)$ is the solution of (5) and $\tilde{\eta}(t)$ is the deviation from the corresponding equilibrium. Our macromodeling approach is based on the construction of a LPV model that approximates the local dynamics of (1) around the trajectory

$(\Xi(t), U_0(t), Y_0(t))$, induced by the instantaneous value of the bias component $U_0(t)$. Exploiting the model linearity, we proceed as follows

1) We build a LPV reduced order model for the map $\tilde{u}(t) \to \tilde{\eta}(t)$ (Sec. III-A).
2) We modify the above to guarantee that it also recovers the mapping $U_0(t) \to Y_0(t)$ (Sec. III-B).
3) We address a self-parameterizing approach to update the model working point at runtime (Sec. III-C).

III. Modeling framework

A. Reduced Order LPV Small-Signal Model

The analytical expression for the linearization of (1) around the trajectory $(\Xi(t), U_0(t), Y_0(t))$ reads

$$\begin{aligned} \dot{\tilde{\xi}}(t) &\approx \tilde{A}(U_0(t)) \cdot \tilde{\xi}(t) + \tilde{B}(U_0(t)) \cdot \tilde{u}(t), \quad \tilde{\xi}(0) = 0 \\ \tilde{\eta}(t) &\approx \tilde{C}(U_0(t)) \cdot \tilde{\xi}(t) + \tilde{D}(U_0(t)) \cdot \tilde{u}(t). \end{aligned} \tag{7}$$

where we dropped the dependencies of the Jacobians linearizations on the state $\Xi(t)$ since we assumed that (5) has a unique solution. For the above, we desire the following reduced order representation of order $n \ll N$

$$\begin{aligned} \dot{\tilde{x}} &= A(U_0(t))\tilde{x} + B(U_0(t))\tilde{u}, \quad \tilde{x}(0) = 0 \\ \tilde{y} &= C(U_0(t))\tilde{x} + D(U_0(t))\tilde{u}, \quad \tilde{y}(t) \approx \tilde{\eta}(t). \end{aligned} \tag{8}$$

Since the maps F, G are unknown in closed form, we build (8) starting from data. To do this, we observe that for frozen time instants, (7) is associated with a transfer function parameterized by $U_0 \in \mathcal{U}_0$, that reads

$$\tilde{\mathsf{H}}(s, U_0) = \tilde{D}(U_0) + \tilde{C}(U_0)(sI_N - \tilde{A}(U_0))^{-1}\tilde{B}(U_0). \tag{9}$$

We can thus build an approximation $\mathsf{H}(s, U_0)$ of order n for (9) and then cast this approximation into a state space parameterized by the instantaneous value of U_0 to obtain (8). We start by retrieving samples of (9) via AC sweeps, performed for a finite number of frequency values and static bias configurations

$$\tilde{\mathsf{H}}_{k,m} = \tilde{\mathsf{H}}(j\omega_k, U_{0m}), \quad k = 1, \dots, K \quad m = 1, \dots, M. \tag{10}$$

The reduced order transfer function is obtained by enforcing

$$\mathsf{H}(j\omega_k, U_{0m}) \approx \tilde{\mathsf{H}}_{k,m}, \quad k = 1, \dots, K \quad m = 1, \dots, M. \tag{11}$$

via PSK iteration [4], based on model structure

$$\mathsf{H}(s, U_0) = \frac{\mathsf{N}(s, U_0)}{\mathsf{D}(s, U_0)} = \frac{\sum_{i=0}^{n} \sum_{\boldsymbol{\ell} \in \mathcal{I}_{\bar{\boldsymbol{\ell}}}} R_{i,\boldsymbol{\ell}} \cdot b_{\boldsymbol{\ell}}^{\bar{\boldsymbol{\ell}}}(U_0)\, \varphi_i(s)}{\sum_{i=0}^{n} \sum_{\boldsymbol{\ell} \in \mathcal{I}_{\bar{\boldsymbol{\ell}}}} r_{i,\boldsymbol{\ell}} \cdot b_{\boldsymbol{\ell}}^{\bar{\boldsymbol{\ell}}}(U_0)\, \varphi_i(s)}. \tag{12}$$

In this model, $R_{i,\boldsymbol{\ell}} \in \mathbb{R}^{P \times P}$, $r_{i,\boldsymbol{\ell}} \in \mathbb{R}$ are unknowns, and $\varphi_i(s) = (s - q_i)^{-1}$ are partial fractions with $\Re\{q_i\} < 0$. The functions $b_{\boldsymbol{\ell}}^{\bar{\boldsymbol{\ell}}}(U_0)$ are multivariate Bernstein polynomials with multidegree $\bar{\boldsymbol{\ell}} = (\bar{\ell}_1, \dots, \bar{\ell}_P)$, while $\mathcal{I}_{\bar{\boldsymbol{\ell}}}$ denotes a set of admissible indices. Model structure (12) admits a representation in terms of state space (8). Technical details about the employed realization procedure are available in [3].

During model generation, we find the involved unknowns by guaranteeing that the final realization (8) remains stable for every possible trajectory of $U_0(t)$, a property known as *quadratic stability* [5]. This is possible thanks to the following Theorem, proved in [3].

Theorem 1 (Sufficient conditions for quadratic stability): let A_1 and B_1 be known constant matrices and

$$C_{1,\boldsymbol{\ell}} = \left[r_{1,\boldsymbol{\ell}}, r_{2,\boldsymbol{\ell}}, \dots, r_{n,\boldsymbol{\ell}}\right], \; d_{1,\boldsymbol{\ell}} = r_{0,\boldsymbol{\ell}}. \tag{13}$$

Then LPV system (8) is quadratically stable if there exists $Q_1^* \in \mathbb{R}^{n \times n}$ such that $Q_1^* = {Q_1^*}^\top \succ 0$ and

$$\begin{bmatrix} A_1^\top Q_1^* + Q_1^* A_1 & Q_1^* B_1 - C_{1,\boldsymbol{\ell}}^\top \\ B_1^\top Q_1^* - C_{1,\boldsymbol{\ell}} & -2d_{1,\boldsymbol{\ell}} \end{bmatrix} \prec 0 \quad \forall \boldsymbol{\ell} \in \mathcal{I}_{\bar{\ell}} \tag{14}$$

Condition (14) represents a Linear Matrix Inequality in the model denominator coefficients. This constraint can be incorporated in the model training phase, so that the resulting constrained fitting problem becomes equivalent to a standard convex optimization problem, which is solved through standard optimization libraries.

B. Reconstructing the Bias Component

At each time instant, the circuit output component $Y_0(t)$ is istantaneously determined by the corresponding value of $U_0(t)$, via the equilibrium mapping (5). Input-output samples of this mapping can be obtained by performing a DC sweep of the circuit netlist for different constant values of U_0. This procedure returns samples

$$Y_{0j} = Y_0(U_{0,j}), \quad j = 1, \dots J, \quad U_{0,j} \in \mathcal{U}_0. \tag{15}$$

When the small-signal system (8) is subject to static input $U_{0,j}$, the corresponding DC output reads

$$\mathsf{H}(0, U_{0,j})U_{0,j} \neq Y_{0j} \tag{16}$$

and is not expected to match the observations Y_{0j} because the bias component is not necessarily small. Therefore, we add a parameterized output correction term $Y_C(U_0)$ to the output equation of (8) in order to restore the desired equilibrium output for all bias conditions. This correction is generated by requiring that

$$Y_C(U_{0j}) \approx Y_{0j} - \mathsf{H}(0, U_{0,j})U_{0,j}, \quad j = 1, \dots J. \tag{17}$$

The above is a standard multivariate function approximation problem that can be tackled via any standard approach (e.g. least-squares regression). Adding the correction in the model output leads to the final model structure

$$\dot{x} = A(U_0(t))x + B(U_0(t))u \tag{18}$$

$$y = C(U_0(t))x + D(U_0(t))u + Y_C(U_0(t)), \tag{19}$$

which is fed with the total input $u(t)$ and returns the total output approximation $y(t) \approx \eta(t)$.

C. Real Time Parameterization

Model (18) is thought to be parameterized in real time with the value of the bias component $U_0(t)$ determining the current working point. However, during system operation, this input term is not directly observable, as mixed together with the small-signal at the circuit interface ports. Thus, the model is practically usable only in view of an automated procedure

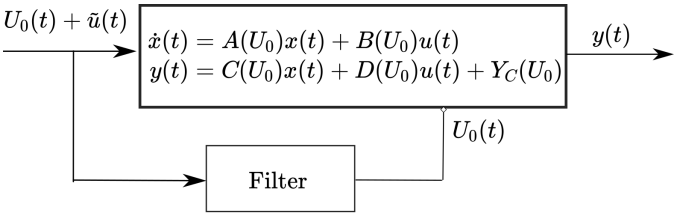

Fig. 1. Block diagram of the proposed self-parameterized LPV macromodel structure.

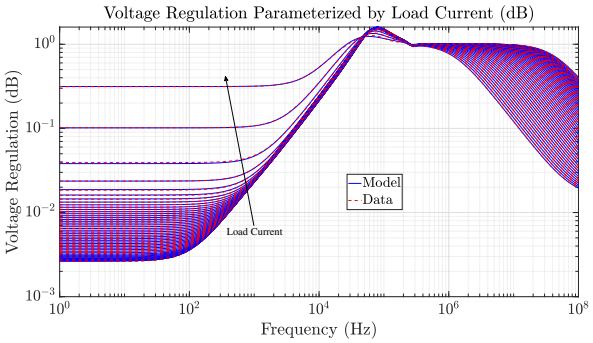

Fig. 2. Fitting of the LDO voltage regulation transfer function for $M = 50$ load current configurations.

aimed at isolating the bias and the small signal components. As assumptions (4), (5), require $U_0(t)$ to vary slowly with respect to the circuit dynamics, we perform real time parameterization as follows

1) During online operation we perform a low pass filtering operation over the the total input $u(t)$. This operation is performed based on a second order Butterworth filter.
2) We use the output of the filter to istantaneously parameterize model (18), as in Fig. 1.

In order to guarantee sufficiently slow variations of $U_0(t)$, we set the cut-off frequency of the filter to $\omega_c = 0.1\omega_p$, being ω_p the angular frequency of the slowest pole of model (12).

IV. Fast Post-Layout LDO Simulation

To test the proposed modeling approach, we instantiated in Cadence environment the Only-MOS low-power regulator design proposed in [6]. The circuit was designed including the layout, using a 40 nm CMOS process, resulting in a 30 MB equivalent netlist.

We performed fast circuit simulation under nonstationary loading conditions, characterized by admissible bias components $U_0^1 \equiv V_{DD} = 0.9$ V, and $U_0^2 \equiv I_L \in [0, 10]$ mA, in agreement with the design specifications. To this aim we built the small-signal model (12) with $n = 9$, in Hybrid representation, considering as input the unregulated voltage V_{DD} at port 1 and the load current I_L at port 2. The model was generated in 8.6 s starting from AC data retrieved for $M = 50$ load current configurations and enforcing the required stability constraints (14). The voltage regulation transfer function of the model is compared with the reference data in Fig. 2. Once (12) is generated, the required DC correction term $Y_C(U_0)$ is computed by enforcing (17) via linear regression, using $J = 50$ data samples of the reference function (15). Finally, a low-pass filter with cut-off frequency $\omega_c = 2\pi 500$ rad/s was designed and an equivalent netlist for model structure of Fig. 1 was instantiated in LTSpice environment. In this environment, we performed a 0.2 seconds long transient analysis by considering a load transition from $I_L = 5$ mA to $I_L = 8$ mA, taking place in $\Delta t = 6$ ms. A small-signal of amplitude 0.2 mA and flat power spectrum in the band $1 - 10$ kHz was added to the bias component I_L. The results of the simulation were compared with those obtained by performing the same analysis using the reference post-layout netlist. Fig. 3 shows the results of the comparison before ($t \in [0.41, 0.42]$ s), during ($t \in [0.42, 0.48]$ s), and after ($t \in [0.48, 0.49]$ s) the load current transition. In all these three situations, the model returns very accurate predictions of the circuit behavior. Using common laptop, the model is simulated in 16 s, while the original netlist in 13 minutes, with a speedup of about $50\times$.

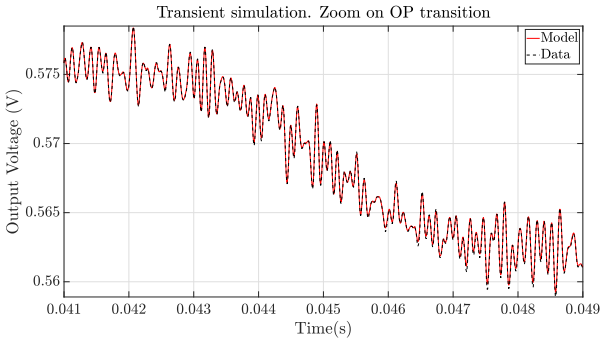

Fig. 3. Time domain validation of the proposed modeling approach.

V. Conclusions

We presented an approach for generating macromodels of analog circuit blocks under small-signal operation with a nonstationary operating point. The resulting macromodels prove to be accurate at reproducing the circuit behavior, while at the same time guaranteing significant runtime reduction.

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