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(Article begins on next page)

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***Abstract*—This contribution reports the design and comparison, at simulation level, of two 4 W Ka-band MMIC power amplifiers on a 100 nm GaN/Si commercial process. The amplifiers are designed targeting FMCW radar applications in the 35 GHz – 40 GHz range. The two amplifiers differ for the number of stages: one adopts only 3 stages, the minimum required to achieve the desired 20 dB small-signal gain, while the other features 4 stage to reach 20 dB also in compression. Both versions achieve in simulation an output power in excess of 36 dBm, at 5 dB gain compression, with associated power added efficiency and gain around 30% and 17 dB for the 3-stage version, and 25% and 22 dB for the 4-stage version.**

***Index Terms*—Millimetre-wave, power amplifiers, GaN, MMIC**

I. Introduction

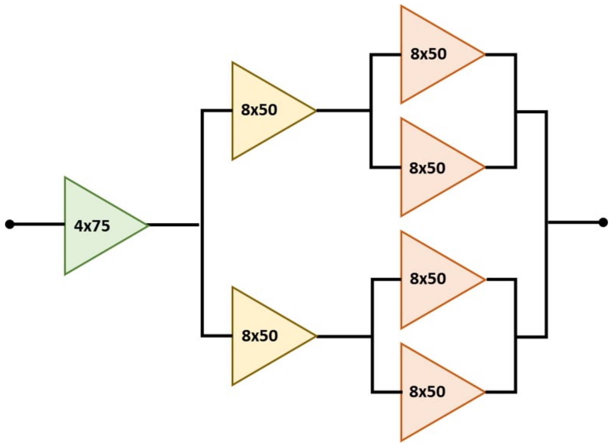
The Frequency Modulated Continuous Wave (FMCW) radar architecture is widely adopted in the automotive field [1], [2] as it allows to gather information on relatively small reflecting objects within a 1 km range by analyzing the properties of the echo signal. Thus it has been identified as the most promising solution for the detection and classification of Unmanned Aerial Vehicles (UAVs), which is becoming a hot topic, due to the wide spread of drones with very small radar cross-section down to micro- or even nano-scale dimensions [3]. The achievable resolution depends on the system's bandwidth and can be extremely high, allowing for the detection of very small objects [4]. To achieve wide bandwidths, millimetre-wave carrier frequencies (Ka-band or above) are employed, while gallium nitride (GaN) technology represents the most suitable choice to achieve high transmitted power, in the order of few watts, in a small chip, together with low noise figure and hence wide dynamic range. However, at such high frequencies, microwave monolithic integrated circuit (MMIC) design with short-gate-length processes is still a challenging task [5]–[10], especially from the power amplifier standpoint, where achieving high efficiency is of paramount importance to keep the radar system compact and lightweight.

This paper presents the design and simulation results of two 4 W MMIC power amplifiers (PAs) working in the 35 GHz-40 GHz frequency range. Targeting the highest portion of the Ka-band, the D01GH process from OMMIC, a commercial 100 nm GaN/Si process, has been selected. The use of silicon is a very interesting option as it reduces fabrication costs and opens tha way for a possible future integration, on the same substrate, of fully silicon technologies. However, this choice requires some additional design precautions to keep junction temperature under control, in particular below 200°C at a maximum ambient temperature of 50°C, due to the relatively poor thermal dissipation capabilities of this substrate [11]. The target output power is 36 dBm at a maximum gain compression of 5 dB, and the minimum corresponding gain and power added efficiency (PAE) are 15 dB and 25%, respectively. A challenging 5 GHz bandwidth is selected, to assess the potentiality of the technology for wideband power amplifier design and to account for possible frequency shifts, considering a bandwidth for the FMCW radar of 1.5 GHz [3].

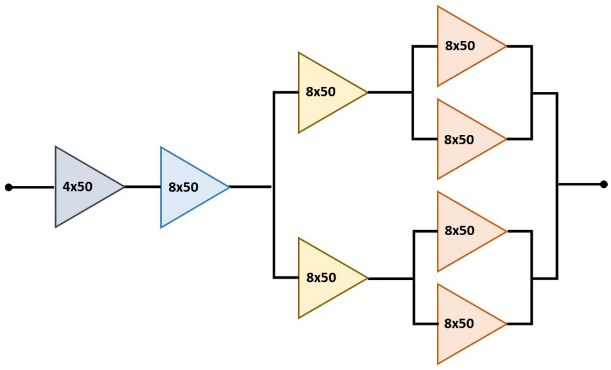
II. Design

As anticipated, the D01GH 100 nm GaN/Si HEMT process, released by OMMIC [12] is adopted for the MMICs design, thank to its high cutoff frequency of 130 GHz, which ensures reasonable gains in the target operating range. For an amplifier operating in continuous wave (CW) mode, the best performance, considering efficiency, linearity and bandwidth, is still represented by the classical combined class-AB architecture [13]. In particular, a 20 % class-AB bias, corresponding to roughly 250 mA/mm of quiescent drain current at 12 V drain bias voltage, is selected to trade off available gain and dissipated power. The expected output power density is around 3.3 W/mm, therefore, considering also the high frequency operation that makes more advisable the use of short fingers, the selected device size for implementing the final stage is 8x50 μm and 4 transistor are combined to achieve 1.6 mm of total periphery, which should be sufficient to achieve the target, once accounting for the combiner losses.

The design is carried out in Keysight ADS adopting the available foundry non-linear models. Device load-pull analysis was carried ut at the worst-case temperature of 50 °C. The relatively low thermal conductivity of the substrate, limits the maximum allowable dissipated power, which in turns impact on the selection of the optimum load and on the achievable output power. Nonetheless, simulations indicate for the 8x50 μm device an output power in excess of the foreseen 3.3 W/mm at reasonable compression levels, confirming the choice of combing 4 devices, with more than 1 dB margin



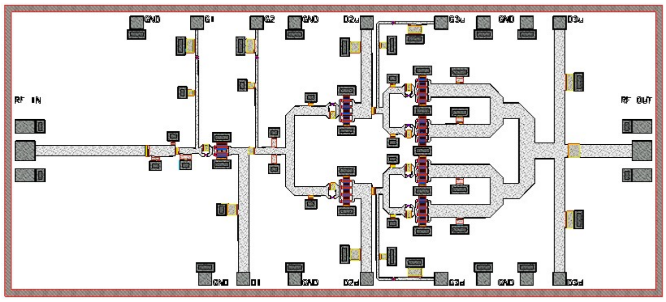
(a) 3-stage architecture.



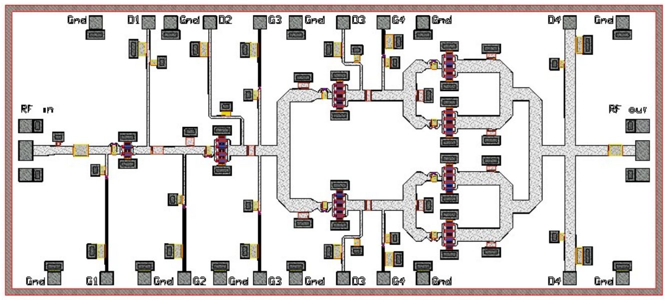
(b) 4-stage architecture.

Fig. 1: Designed power amplifier architectures.

on combing losses (ohmic and mismatch losses). The small-signal gain is above 7 dB, therefore 2 is the minimum number of driving stages to be added to achieve the target gain of 20 dB (in small-signal), hence the choice of a 3-stage architecture. However, to provide gain margins also in deep compression, a second version with 4 stages is also designed. In particular, as shown in Fig. 1, both versions adopt two parallel 8x50 μm devices in the last driver stage (0.8 mm periphery), with the same optimum load selected for the final stage, but operated in more mild compression. The 3-stage version then adopts a single 4x75 μm device (0.3 mm periphery) as pre-driver, while the 4-stage versions employs a single 8x50 μm device (0.4 mm periphery) as pre-driver and a 4x50 μm device (0.2 mm periphery) as gain-boosting stage. Fig. 2 reports the final layouts, as well as a picture of the fabricated MMICs: the chip size is $5.0 \times 2.2\,\text{mm}^2$ for both versions. All devices are made unconditionally stable in a wide frequency range by means of a parallel R-C network at the gates, and, despite sharing, in simulation, the same gate voltage (-1.25 V), each stage is biased independently to allow for tuning in measurement. All matching networks are simulated electromagnetically for better accuracy, accounting for the unavoidable coupling effects among adjacent elements (especially via holes) at Ka-band [14].



(a) 3-stage rchitecture.



(b) 4-stage architecture.

Fig. 2: Designed power amplifiers layouts.

III. Simulation results

In the following the simulation results obtained for the two amplifiers are reported and compared. Fig. 3 reports the small-signal (S-parameter) simulation results: as expected the small-signal gain S_{21} (green circles) is higher, in the 21.1 dB – 25.3 dB range, for the 4-stage architecture (dashed lines), while for the 3-stage architecture it is 17.3 dB to 21 dB across the entire 35 GHz – 40 GHz frequency band. For both amplifiers, input (S_{11}, red crosses) and output (S_{22}, blue triangles) matching to 50 Ω are better than -10 dB at all frequencies. Gain variation in the bandwidth, around 4 dB in both cases, is not considered as an issue, since, as anticipated, the expected operating bandwidth of the FMCW radar, target application of these designs, is roughly 1.5 GHz around the center frequency of 37.5 GHz, a range where gain variation remains within 1 dB for both MMICs.

The large-signal simulation results under CW excitation across the entire 35 GHz – 40 GHz range with 1 GHz step are shown in Fig. 4, Fig. 5 (vs. input power) and Fig. 6 (saturated performance vs. frequency). Both PAs match the minimum target requirements, but the 3-stage architecture outperforms the 4-stage one in terms of output power and efficiency, reaching, at roughly 5 dB compression, 38 dBm output power around the center frequency and 37 dBm at the maximum frequency of 40 GHz (worst case), while PAE is above 30% in the whole range (34% peak). On the other hand, the saturated gain fort he 3-stage architecture is in the 15 dB to 17 dB range (decreasing with frequency), while, the 4-stage architecture achieves, at the same 5 dB compression, 20 dB power gain, nearly flat in the entire bandwidth (less than 0.6 dB ripple),

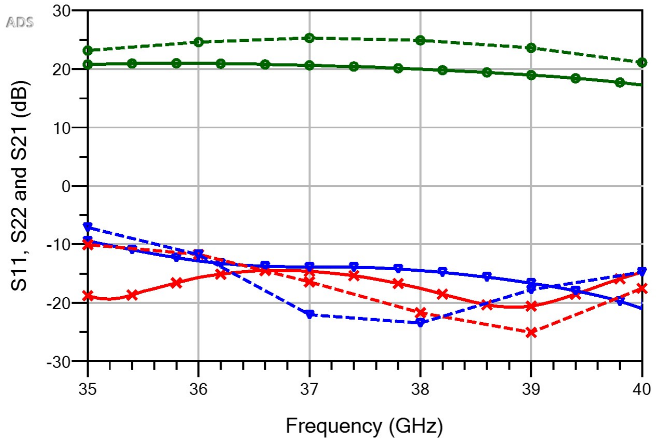


Fig. 3: S-parameter simulation results for the 3-stage (solid lines) and 4-stage (dashed lines) architectures.

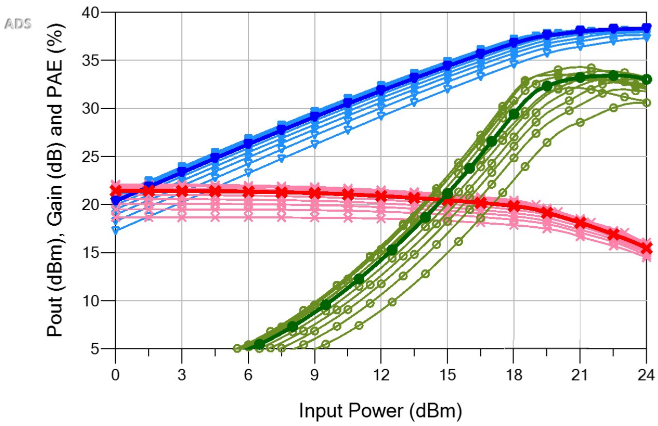


Fig. 4: Simulated power-sweep results for the 3-stage architecture: output power (blue triangles), power gain (red crosses) and PAE (green circles). Bold traces are the results at center frequency (37.5 GHz).

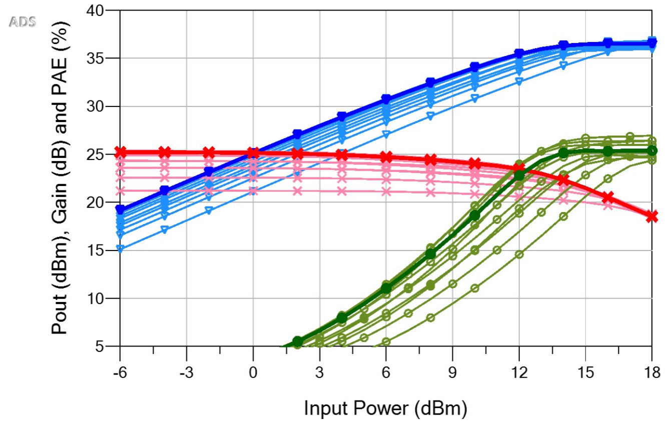


Fig. 5: Simulated power-sweep results for the 4-stage architecture: output power (blue triangles), power gain (red crosses) and PAE (green circles). Bold traces are the results at center frequency (37.5 GHz).

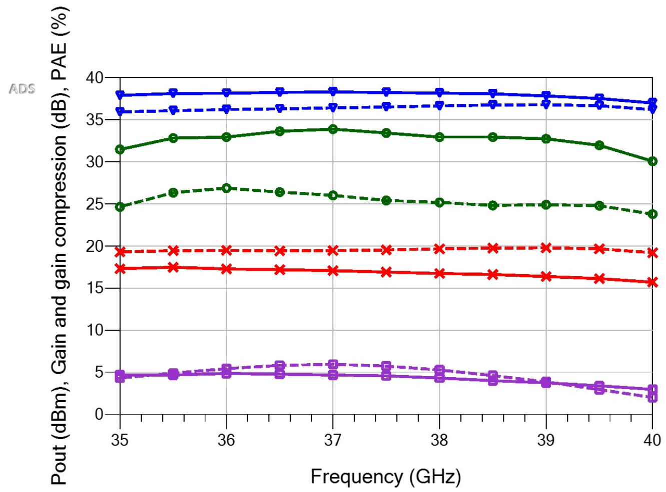


Fig. 6: Simulated results at saturation for the 3-stage (solid lines) and 4-stage (dashed lines) architectures: output power (blue triangles), power gain (red crosses), PAE (green circles) and gain compression (purple squares).

while still providing 36 dBm of output power and 25% PAE. Channel temperature of each individual device is evaluated from its dissipated power [15] adopting a fixed, worst-case, thermal resistance aorund 90°C/W: for all devices of both PAs it is kept within 200 °C, while the total dissipated power is around 12 W in both MMICs.

IV. Fabrication and Testing

The designed PAs have been both fabricated and mounted on a brass carrier for characterization, as shown in Fig. 7. The preliminary measurement results for the 4-stage architecture, on a restricted bandwidth, have been presented in [15], demonstrating the capability of this PA to provide the target 4 W at least up to 38 GHz (test-bench limit). The measured gain was significantly higher than simulation predictions, leading to an higher PAE, close to 30% but also to some instability issues in some of the MMIC samples. Unfortunately, much more pronounced instabilities are affecting the 3-stage PA, eventually preventing its characterization. This is due to a sensibly narrower stability margin, deliberately chosen in the design phase to maximize the devices' maximum available gain (MAG), in turn necessary for reaching the target 15 dB gain at saturation with only 3 stages.

V. Conclusion

The design and simulation results of two Ka-band GaN/Si MMIC power amplifiers for CW radar applications have been reported and compared. The two architectures, both combined class-AB amplifiers, differ mainly for the number of stages: one is adopting 4 stages to relax gain constraints and allowing for wider margins in the design of the stabilization networks, while the other aims at reaching 15 dB of saturated gain (20 dB in small signal) with only 3 stages. In simulation, the 3-stage

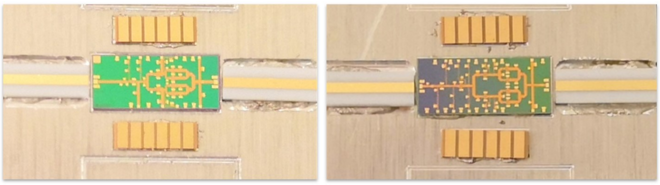


Fig. 7: Picture of the two fabricated MMICs.

PA achieves an output power in excess of 37 dBm together with a PAE above 30% at 5 dB compression, while fulfilling the gain target. At the same compression level, the 4-stage PA, achieves 36 dBm of output power with 25% PAE, together with a 20 dB gain (up to 25 dB in small signal).

Acknowledgment

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