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# K-band GaAs Doherty Power Amplifiers for microwave backhaul

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**Abstract**—This paper presents the design and characterization of two Doherty power amplifiers for K-band applications implemented with Qorvo’s 150 nm GaAs pHEMT technology. A 1 W module is developed first, and a 2 W amplifier is then obtained by combining on-chip two identical Doherty modules. The complete characterization of the two amplifiers demonstrates that the design approach, based on a matching combiner rather than a  $50\Omega$  combiner, leads to very good combining efficiency with a relatively compact layout. The combined amplifier achieves in the 23.2 GHz–25.2 GHz range an output power in excess of 32 dBm, a remarkably high power for a GaAs Doherty MMIC at these frequencies. The small-signal gain is around 10 dB, while power-added efficiency is higher than 24% and 19% at maximum power and at 6 dB back-off, respectively, over the whole frequency range.

**Index Terms**—Doherty power amplifier, GaAs, MMIC, K-band, microwave radios

## I. INTRODUCTION

The Doherty power amplifier (DPA) is a widely adopted solution in sub-6 GHz wireless transmitters to enhance back-off efficiency when dealing with high peak-to-average-power-ratio (PAPR) signals [1], [2]. Nowadays, both mobile and satellite communication systems are pushing toward higher carrier frequencies to achieve more bandwidths, hence the need of developing microwave monolithic integrated circuit (MMIC) DPAs at K-band and above. GaN and GaAs technologies are both exploited to this purpose, the former providing higher output power densities, while the latter being a more mature technology and thus representing a more reliable and less expensive choice, still able to provide watt-level output powers with good efficiency.

In this work we present two power amplifiers for K-band microwave backhaul applications, implemented on the  $0.15\mu\text{m}$  GaAs PWR HEMT MMIC process from Qorvo. A first module is a 1 W Doherty power amplifier, while the second, based on the combination on chip of two identical Doherty stages, targets around 2 W of output power. In measurements, the designed chips achieve, respectively, 30 dBm and 32 dBm saturated output power, both with an associated power-added efficiency (PAE) in excess of 22% in the 23.2 GHz–25.2 GHz frequency range. On the same bandwidth, the 6 dB back-off efficiency is better than 19%, while the small-signal gain is around 10 dB for both DPAs.

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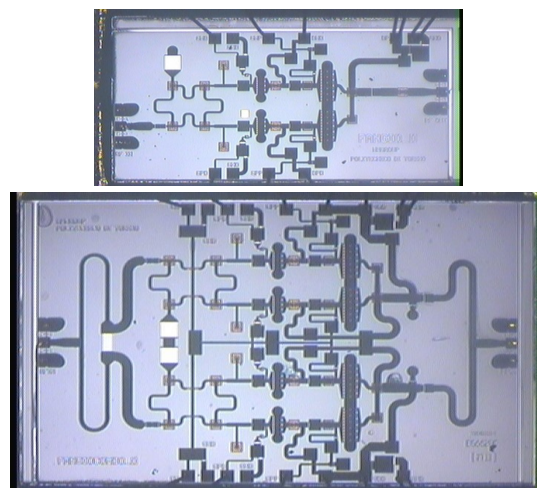


Fig. 1. Microscope pictures of the fabricated MMIC DPAs: single ( $2.88 \times 1.43\text{ mm}^2$ , top) and combined ( $3.77 \times 2.44\text{ mm}^2$ , bottom).

## II. DESIGN

The PAs are designed on the  $0.15\mu\text{m}$  PWR GaAs pHEMT MMIC technology from Qorvo. The substrate thickness is  $100\mu\text{m}$ , and the process provides three metal layers. When designing power amplifiers at high frequency there are limitations in the maximum size that can be selected for each individual transistor, hence the need for power combination.

The target output power is around 30 dBm for the single DPA, and hence around 33 dBm for the combined structure, in the 20.8 GHz–24 GHz range, which targets the 21.2 GHz–23.6 GHz backhaul band including guard rings. A cascade of a  $8 \times 50\mu\text{m}$  driver followed by a  $12 \times 85\mu\text{m}$  power device is adopted for both the main and auxiliary PA. As discussed in [3], the embedding of the driver in the two branches improves the achievable PAE compared to the use of a single driver before the splitter. The main and the auxiliary amplifiers adopt the same interstage and input matching network topologies, in order to minimize the impact of process variations on phase alignment, while a semi-lumped branch-line coupler is used to evenly split power between the two branches.

As detailed in [4], power combination at DPA level is

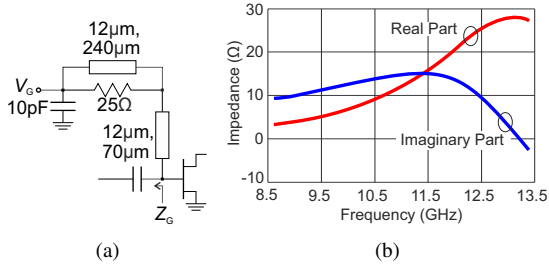


Fig. 2. Schematic (left) and equivalent impedance at  $f_0/2$  (right) of the gate bias feed in the interstage matching network, which has been identified as the cause of the observed parametric oscillations.

adopted, as it provides more favorable impedance levels in the output combiner and consequently an improved control of the load modulation over the bandwidth. This comes at the price of an increased complexity for the bias routing and DPA deployment on the chip, which therefore requires careful optimization. Two identical DPA cells are then combined adopting a Wilkinson power splitter at the input, and a non-isolating combiner which also provides output matching.

The manufactured MMICs are shown in Fig. 1, their chip size is  $2.88 \times 1.43 \text{ mm}^2$  and  $3.77 \times 2.44 \text{ mm}^2$ , respectively.

The amplifiers were initially characterized only at a single frequency (see [4]), as they suffered from parametric oscillations in the lowest portion of the band. They were thus analyzed through the CAD-simulation-based stability test proposed in [5], which allowed to ascribe the cause of oscillations to the interstage matching network. In fact, to maximize the gain, the impedance seen by the gate of the final stage device (see Fig. 2(a)) needs to be inductive, to compensate the gate capacitance, and with a comparably low resistive part. However, as shown in Fig. 2(b) the impedance resulted highly inductive and with very low resistance, also in the 8.5 GHz-11.5 GHz range, corresponding to the  $f_0/2$  sub-harmonic frequency. Since the structure of the basic DPA cell is identical in the two MMICs, they present oscillations of the same nature and at the same frequencies. The following Section presents the characterization and comparison of the single and combined DPAs in the oscillation-free portion of the band, which is still competitive at this frequency. The parametric oscillations have then been solved in [6], which presents a state-of-the-art 1 W single DPA, with no power combination.

### III. CHARACTERIZATION

For the characterization campaign, the chips are mounted on a brass carrier for on-wafer RF probing while the DC pads are bonded to external connectors, with off-chip decoupling capacitors to avoid low-frequency instability. The characterization is carried out at 6 V drain voltage, with a quiescent drain current of 100 mA/mm for both the driver and final devices in the main branch, while those of the auxiliary branch are biased at -1.3 V and -0.95 V, respectively.

Fig. 3 reports the comparison between simulated and measured scattering parameters in the 16 GHz–30 GHz frequency

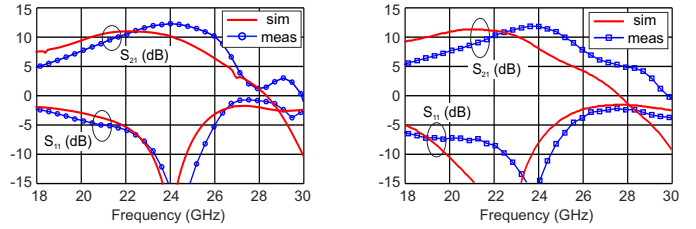


Fig. 3. Simulated (solid) and measured (symbols) scattering parameters of the single (left) and combined (right) DPAs in the 18 GHz–30 GHz range.

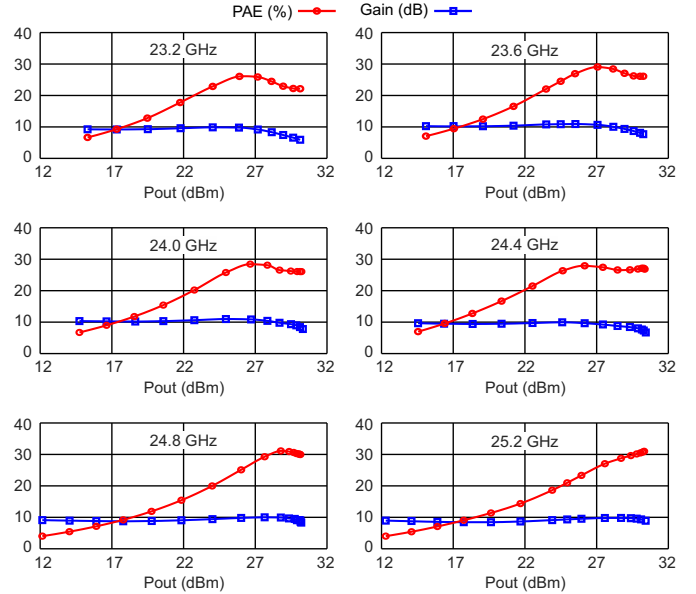


Fig. 4. Measured power sweeps (red circles: PAE, blue squares: Gain) of the single DPA from 23.2 GHz to 25.2 GHz in 400 MHz steps.

range. Both DPAs present an analogous frequency shift, of about 2 GHz towards higher frequencies, especially evident in the  $S_{21}$ . Since the measured DPAs result centered around 24 GHz, both in terms of gain and input matching, the large-signal characterization has been performed on the 22.8 GHz–25.6 GHz range.

Fig. 4 and Fig. 5 show the measured CW power sweeps at 23.6 GHz, 24 GHz, 24.4 GHz, and 24.8 GHz, for the single and combined DPA, respectively. Fig. 6 reports and compares the results obtained in the entire 22.8 GHz–25.6 GHz characterization range. Over the 23.2 GHz–25.2 GHz frequency band the saturated output power of the single DPA is higher than 30 dBm, while saturated and 6 dB back-off PAE is higher than 22% and 20%, respectively. The saturated output power of the combined DPA is higher than 32 dBm, while saturated and 6 dB back-off PAE is higher than 24% and 19%, respectively. Compared to the single DPA, the output power increases of 2 dB to 3 dB over the band, as expected. The ohmic losses in the output power combiner as well as some slight phase misalignment between the signals in the two branches, cause the power increase to be somewhat less than the ideal 3 dB

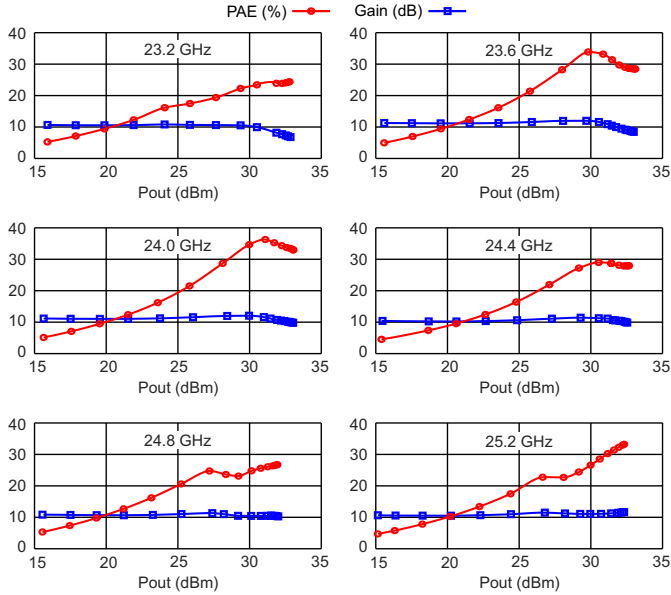


Fig. 5. Measured power sweeps (red circles: PAE, blue squares: Gain) of the combined DPA from 23.2 GHz to 25.2 GHz in 400 MHz steps.

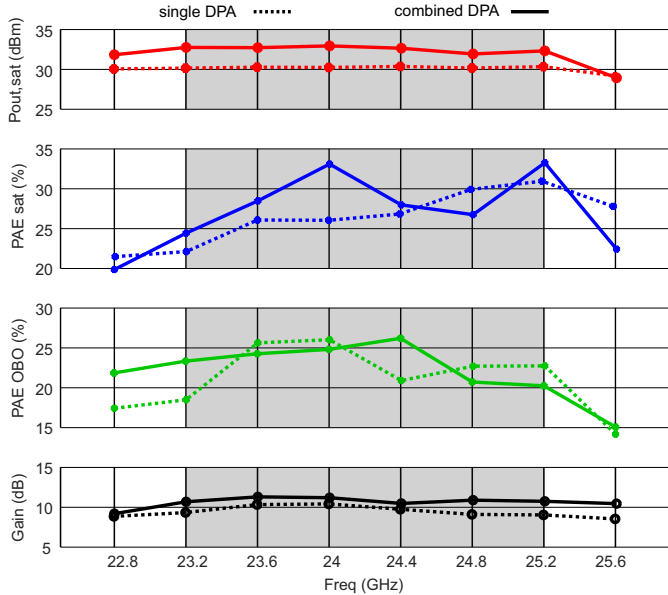


Fig. 6. Comparison of measured performance of the single (dashed) and combined (solid) DPAs in the 22.8 GHz–25.6 GHz range.

at some frequencies. The PAE achieved by the single DPA is maintained in the combined version, both at saturation and in back-off over the whole frequency band. The gain is also very similar, even if slightly higher for the combined DPA, probably thanks to a better input matching provided by the Wilkinson power splitter followed by the two branch-line couplers. As demonstrated in Table I, the DPAs presented in this work show the highest output power with respect to other state-of-the-art GaAs MMIC DPAs at this frequency, with comparable efficiency and competitive bandwidth.

TABLE I  
COMPARISON WITH PREVIOUSLY PUBLISHED GAAS MMIC DPAS.

Ref.	Freq. (GHz)	$P_{MAX}$ (dBm)	PAE <sub>SAT</sub> (%)	PAE <sub>OBO</sub> (%)	Gain (dB)
[3]	22.8-25.2	29.9	25	14	11
[7]	28.5-31.5	27.0	38	32	10.5
[8]	29-31.8	25.7	31	23	n.a.
[9]	26.4	25.3	38	27	10.3
[10]	26.6	27.0	42	32	10.5
[11]	28	28.5	37	27	14.4
[6]	21-25	29.5-30.2	30-37	19-24	10
<b>single DPA</b>	<b>23.2-25.2</b>	<b>30.1-30.3</b>	<b>22-31</b>	<b>20-26</b>	<b>9</b>
<b>comb. DPA</b>	<b>23.2-25.2</b>	<b>32-32.8</b>	<b>24-33</b>	<b>19-26</b>	<b>10.3</b>

#### IV. CONCLUSION

This paper presented a single and a combined GaAs MMIC Doherty power amplifiers in K-band. Despite a frequency shift toward higher frequencies, both DPAs achieve in the 23.2 GHz–25.2 GHz band a remarkably high output power, in excess of 32 dBm for the combined PA, among the highest for a GaAs MMIC DPAs at this frequency. The PAE is above 24% and 19%, at saturation and at 6 dB back-off, respectively, while both DPAs exhibit a small-signal of around 10 dB. The parametric oscillation issue affecting the two DPAs has been identified in [5] and solved in [6]: considering the output power boost brought by combination, future work will deal with the design of a combined DPA based on this module, covering the full band originally targeted.

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