FDMA Point-to-Multi-Point Fibre Access System for Latency Sensitive Applications

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Abstract *We present a demo for a multiple uplink access system with real-time services. Several terminals transmit and are detected simultaneously through FDMA. The system can allow latency-sensitive and best-effort applications to share the network. ©2022 The Author(s)*

Introduction

Fibre based point-to-multi-point (P2MP) networks have proven to be a reliable and low cost solution for residential optical access in the form of passive optical networks (PONs). The success of PONs relies significantly on the simplicity of the optical distribution network (ODN) deployed in the field, which is essentially based on power splitters creating the P2MP distribution fibre links. Besides the residential broadband application, other use cases have been proposed for P2MP networks in recent years. P2MP for machine-to-machine (M2M) networks in the framework of Industry 4.0 is a very demanding use case, as it requires data links with extremely low latency down to 1ms or less and jitter as low as 1µs [1-3]. While most M2M links will require low data rate, services like machine vision applications could potentially require Gb/s capacity to transmit low latency high definition video streams to the computing units for real-time decisions [4, 5].

Fibre based P2MP networks have several advantages compared to state of the art solutions in industrial networks (industrial Ethernet protocols and several other proprietary communications buses), which are almost entirely based on point-to-point electrical interconnects, namely: intrinsic immunity to electromagnetic interferences, simpler management of the head end since the traffic is aggregated in a single transceiver, thinner, lighter and generally less bulky cables. All these advantages can lead to a lower overall cost. While standardised residential PON systems have been proposed for this application, their time-domain sharing of the network capacity between multiple users inherently introduces high latency and jitter, which are not compatible with the M2M use cases. PON systems with a modified and optimized medium access control (MAC) have been recently demonstrated where dynamic bandwidth allocation is replaced by fixed time slot allocation to each user [6]. However, some jitter remains and buffers need to be added which enforce a trade-off between latency and jitter suppression. Alternative solutions propose to share the P2MP network capacity via frequency division multiple access (FDMA) [6, 7]. FDMA sub-channels effectively create continuous links between the optical terminal equipment (OTE) and the optical aggregation point (OAP), allowing for ultra-low latency and jitter.

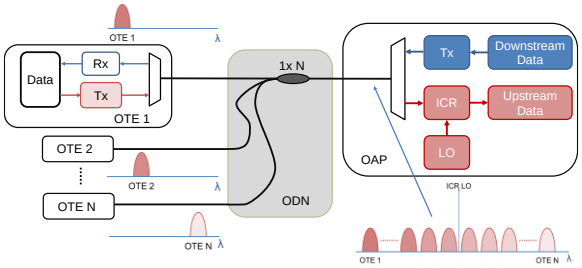

Fig. 1: P2MP access network system utilizing low latency FDMA sub-channels in the upstream.

In this real-time demonstration, we present a solution for an FDMA P2MP system (Fig. 1), using an integrated coherent receiver (ICR) to detect FDMA sub-channels, generated by the transmitters (Txs) in the OTE. FPGA-based prototyping platforms with compatible analog to digital converters (ADC) and digital to analog converters (DAC) implement low-latency real-time processing [8]. The demonstration focuses on the uplink from the OTE to the OAP, which has the additional challenge of having to maintain an accurate control of the OTE wavelengths to avoid interference between the sub-channels. The demonstration implements a closed loop wavelength control and registration protocol for the OTEs, and is capable of carrying Ethernet (ETH) traffic with low and deterministic latency between the OTE and OAP.

FDMA for Time-Sensitive P2MP Access Networks

As an alternative to conventional time-domain multiple access networks, we propose an FDM

approach in which the terminals can have slightly different wavelengths and transmit simultaneously without needing to compete for the network. This could be of particular interest in applications that require a deterministic latency or whose transmission time overlaps within certain periods.

In order to maintain the terminal equipment in a simple manner, we employ a directly modulated laser (DML) with a TEC control to stabilise the wavelength. Several OTEs are collocated as close as possible in the wavelength domain. A coherent Rx at the OAP detects simultaneously all the uplink signals and also extracts the spectral distance of the terminals to the local oscillator (LO) frequency. With this information from the OAP, we can fine-tune the OTE lasers. To avoid interference among the terminals, we propose the following registration procedure: Initially, the terminal heats to the maximum in order to move its emission frequency up to the registration spectral band (Fig. 2). With a low-frequency tone, the OTE communicates its serial number to the OAP, which measures the OTE wavelength and sends it back through the broadcast downlink channel. The OAP also informs the terminal to which spectral channel it should tune. Once the terminal knows its wavelength and the target channel, it cools down following the empirical rule of 0.1nm/°C.

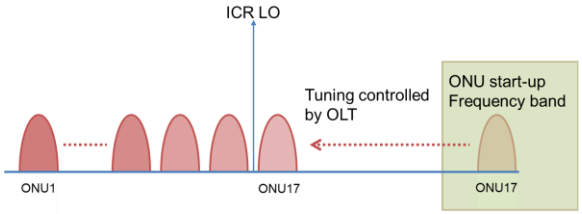

Fig. 2: Registration procedure for OTE controlled from OAP

Demo Description and user interfaces

For the demonstration setup (Fig. 3), we focus on the uplink. Firstly, we test the system with pseudo random binary sequences (PRBS) of several lengths. We generate the sequences directly in the FPGA and encode them with a consistent overhead byte stuffing (COBS) [9] for efficient, reliable and unambiguous packet framing which allows the receiver (Rx) OAP to recover from malformed packets.

Subsequently, we apply a G.709 forward error correction (FEC) encoder [10]. Next, the samples are differentially encoded and filtered by means of a squared-root Nyquist filter. A digital differentiator is implemented, but can be bypassed depending on the modulation format. Finally, an upsampling stage is added to match a 72 GSa/s DAC with 6-bit physical resolution, which converts to analog waveforms that either directly modulate a DFB laser or an optical modulator. The inverted output from the DAC modulates another Tx which acts as a second terminal.

Thanks to the differentiator, we can modulate the DFB in phase and get a binary phase modulated signal [11] which is sent through 20km of standard single-mode fibre. With an optical variable attenuator (VOA), we control the received optical power after the fibre. At the central aggregation point, a 20-GHz ICR detects both OTE signals. For reduced complexity and number of components in the Rx, we use the ICR in heterodyne mode by displacing the LO wavelength from the Tx one, and detect only the in-phase components of the two polarizations through a pair of 68 GSa/s ADC with 6-bit resolution. The Rx can easily be extended to intradyne operation, detecting also the quadrature components and increasing the available optical bandwidth.

Fig. 3 illustrates how samples from the ADCs are collected by two frontend FPGAs and processed by a backend FPGA. Before the Rx DSP, a downconversion stage translates each terminal signal to baseband and allows to separate them in frequency. Next, we apply downsampling and then decode the signals with an interferometer. Afterwards, the samples pass through a single-output 7-tap equalizer whose coefficients are adapted according to the constant modulus algorithm (CMA). A slicer then decides on the binary information and the bits are FEC decoded. When sending ETH packets, the frames are also COBS decoded. Finally, the bit error ratio (BER) is computed by direct counting of errors.

The wavelength of the DFBs is set and controlled in temperature by means of a TEC and a control circuit. The latter can be implemented either with analogue components or digitally. For

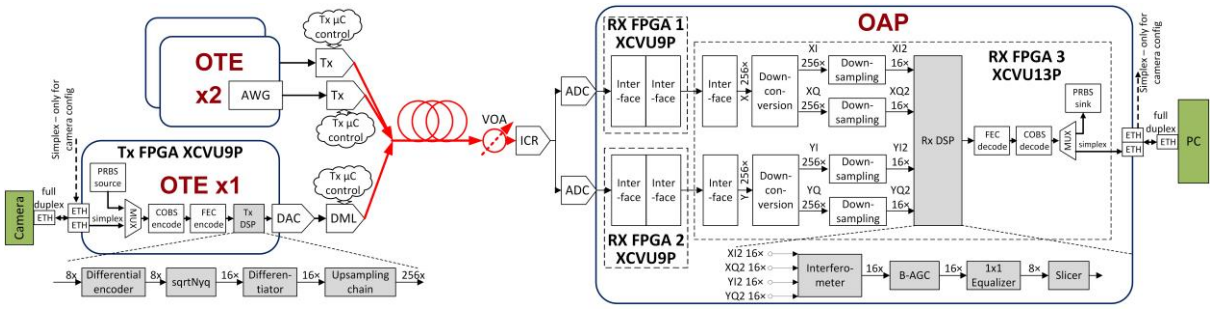

Fig. 3: End-to-end real time demo setup with FPGA-based DSP implementations

the communication with the DFB and control elements, we employ a Raspberry Pi processor. From the data captured by the FPGA, we compute the received optical spectrum as plotted in Fig. 4. This information in the Rx is useful to continuously monitor the emission wavelength of each user and close the control loop. Fig. 5 shows the stability measurements of the DFBs when these are not modulated.

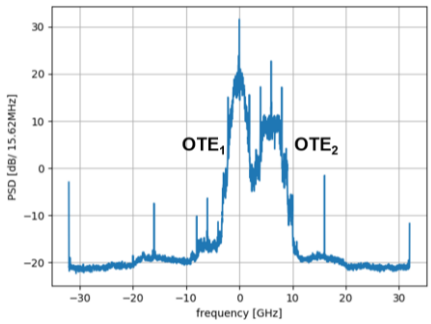

Fig. 4: Detected Rx spectrum

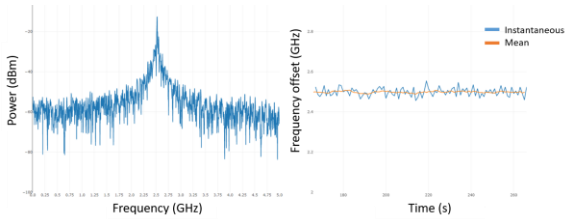

Fig. 5: Wavelength control and stability measurements

Fig. 6 and Fig. 7 depict the Rx graphical user interfaces (GUI) of OTE_1 and OTE_2, respectively. In particular, the BER before and after FEC is shown. We limit the optical power into the Rx to be just below the FEC threshold and proof that the error correction is functioning.

Fig. 6: Rx GUI for OTE_1

In order to show that the two users can be detected simultaneously, we tune the LO wavelength close to the one of OTE_1. OTE_2 wavelength is 5 GHz separated as seen in Fig. 4. The FPGA detects both users simultaneously.

In the demonstration of live services, a video signal from a HD camera is encoded and sent through ETH to OTE_1. Fig. 8 shows a picture of the setup. The optical signal is generated in OTE_1 and then transmitted to the OAP, The decoded

Fig. 7: Rx GUI for OTE_2

signal is sent to an ETH card which communicates with a PC to decode and display the video. We test the proper detection of the video signal in different intermediate frequencies by tuning the DFB wavelength. We count the total latency as sum of clock cycles (4 ns) that the FPGA requires for all the OTE and OAP operations and can confirm that number by measurements. The total processing latency with our current implementation, combining Tx DSP, Rx DSP, FEC en- and decoder is exactly 2.516 µs. For end-to-end transmission, there comes on top an additional ETH switching and data processing delay of up to 7.2 µs plus queuing delays and an additional fibre delay of approximately 5 µs/km [2]. In our FPGA implementation or equivalent ASIC implementations, the data processing jitter is deterministic and defined only by the clock cycle period, which is 4ns in our case.

This demo shows that the system keeps low and constant latencies among several users with minimal jitter.

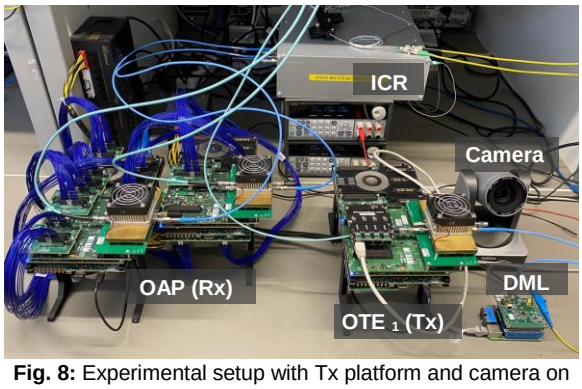

Fig. 8: Experimental setup with Tx platform and camera on the right hand side and Rx platform on the left hand side

Conclusions

In this FPGA-based real time transmission demonstration, we present the operation of the uplink of a P2MP access network system utilizing low latency FDMA sub-channels. The demonstration shows the streaming of a live HD video through Ethernet. The demonstration also implements a closed loop wavelength control and registration protocol for the OTEs.

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