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16 September 2026

An Adaptive Method to Reduce Undershoots and Overshoots in Power Switching Transistors Through a Low Complexity Active Gate Driver

Erica Raviola, *Member, IEEE*, Franco Fiori, *Member, IEEE*

***Abstract*—Active gate drivers lend themselves well to reducing over- and under- voltages during the commutations of hard switched power transistors, as well as to damping resonances. However, their control strategy is a major challenge, as it should account for variations of operating condition, parameter spread, and non linearities of the driven transistor. This paper proposes an effective control method to reduce overshoots and undershoots in a power transistor driven by an active gate driver. The modulation pattern is modified on-the-fly and none a-priori characterization is required. The presented method modifies the timing parameter to attain almost zero over- and under- voltages with the lowest power losses. This is achieved by combining a low complexity active gate driver with the measurements of peak values of the drain-source voltage. The technique was experimentally assessed for a 48-12 V DC-DC converter, and resulted in better switching performance than standard solutions and open loop control.**

***Index Terms*—Active Gate Driver (AGD), Electro-Magnetic Interference (EMI), switching waveforms, switching oscillations, power transistors.**

I. Introduction

The growing demand for e-mobility is expected to push power electronics forward to meet the demand for efficiency and power density. Besides high voltage equipment, a large amount of on-board systems will continue to require medium- and low-voltage supplies [1], for which several design constraints should be met. The commutations of fast power transistors have become crucial, as they directly affect efficiency, Electro Magnetic Emission (EME), as well as reliability. These transients can lead to overshoots and oscillations superimposed onto the switching waveforms, which are tough to mitigate without affecting losses. Voltage and current overshoots reduce the device lifetime, resulting in less reliable systems [2]. At the same time, high dv/dt and di/dt, as well as the presence of oscillations triggered by fast commutations (voltage and current ringing), have a detrimental effect on the EME delivered by power converters [3].

The cause of ringing lies in the inductive and capacitive parasitics included in High Frequency (HF) switching loops. Packaging and interconnections contribute to the overall parasitic inductance, which may resonate with the output capacitances of active devices. Current and voltage steps, which are caused by the switching of power transistors, can excite such HF LC circuits, resulting in unwanted overshoots [4].

To limit such over-voltages and over-currents, the most popular approaches involve the tuning of the gate resistance [5] and the insertion of snubbers [6], [7]. Some recent investigations have explored the use of source inductance [8]. However, these solutions have proven not to be optimal. A better trade-off between overshoots and losses can be achieved by Active Gate Drivers (AGDs) [9].

AGDs are able to shape the switching trajectory of the driven transistor from the gate terminal by controlling the gate charge during transients. Depending on the aim of the designer, they can reduce overshoots [10], [11], di/dt and dv/dt [12], and the delivered EME [13]. A crucial aspect of AGDs is their control strategy, i.e., the method used to determine the modulation pattern, which can be classified into open loop, direct feedback, model-based, and sequential approach [9]–[12], [14], [15]. In open loop AGDs, such as in [9], the modulation profile is fixed and found a-priori. However, under operating condition or temperature variations, such a profile results in a degradation of switching performance [16]. To find the best suited parameters in a large solution space, [10] proposed an optimization platform based on a meta-heuristic algorithm, which required from 165 to 572 s to run. The platform was developed using an oscilloscope, a controller PC module and a power analyzer, which are however not available in a practical implementation. Direct feedback AGDs are typically based on the sensing of $di/dt, dv/dt$, drain current and drain-source voltage to detect the different transient stages, and they can control each stage separately [17]. This can be achieved by an analog [18] or digital [17] controller. However, as transients are becoming faster, the sensing circuits and the AGD controller need to be fast as well, and the effectiveness of direct feedback AGDs can be limited. A different approach, which is usually referred to as model-estimator control, consists in building up a mathematical model to predict the switching trajectory. In [14], the current optimal profile was obtained in the s-domain. However, to account for non linear effects, the AGD timing parameters were obtained by simulation and stored in a Look Up Table (LUT) for the different values of load current. Similarly, the measurement of bus voltage and load current was exploited in [12], along with a mathematical model, to choose the most suited AGD voltage profile that optimizes the defined cost function. An analytical switching model and an optimization algorithm were proposed in [19] to trade off between losses

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and EMI noise based on Matlab software. In order to be effective, such solutions require an accurate model to predict the switching trajectory, for which the values of parasitic elements, the parameters to active devices, e.g., threshold voltage and parasitic capacitances, and the delays of the AGD itself should be known. However, these parameters are affected by process variations. The threshold voltage depends on the thickness of the epitaxial layer, by the channel length and by the concentration of interface traps, resulting in up to 0.7 V variations [20]. The internal gate resistance and the parasitic capacitances show a 12 % and 10 % spread, respectively [21]. Moreover, several studies have reported the dependence of such parameters on temperature and and its effect on the switching trajectory [22], [23].

In order to address the above uncertainties, a sequential control strategy can be exploited [24]. In this case, the AGD modulation profile is adapted cycle by cycle depending on the switching performance attained in the previous transient. In such a way, high speed components can be avoided, as there is no need to be faster than the transient, and uncertainties related to the model are no longer a concern, since the actual switching performance is fed back. Such kind of control was experimentally assessed in [24]. However, the test setup was based on an oscilloscope, Matlab software, and an isolated signal generator to drive the power transistor, which is not a viable solution in practical applications. The work proposed in [11] is based on a sequential control including a model estimator, but the relation between load current and variations of the output resistance of AGD was experimentally fitted, meaning that it suffers from the same issues of a model-based control. More recently, with the aim of suppressing ringing, the duration of Miller's plateau was measured and exploited to modify the profile of the AGD output resistance cycle by cycle in [25]. However, only simulation results were provided, and a fitted function was exploited to vary the gate resistance. To sum up, existing AGDs controllers have so far not truly performed the required calculations on-the-fly. This means that some LUT or previously extrapolated relation are required to find the proper modulation profile.

This paper presents an adaptive method that is a true sequential digital control, and is not based on any switching model or a-priori function extrapolation. This is obtained by exploiting a minimum search algorithm applied to a low-complexity driver, which continuously runs on the AGD controller itself. With respect to previous works, the undershoot and overshoot affecting the drain-source voltage are exploited as an indirect estimation of the oscillations taking place. On the basis of these measurements only, the controller adapts the AGD parameters to attain the lowest over- under- voltages. The method is able to find and to track the best-suited AGD parameters with no external aid, which makes it robust against variations of operating conditions, of power transistor parameters, and of parasitic values. Moreover, the technique is well suited for a chip integration.

The paper is organized as follows. In Sect. II, the turn on and the turn off of a hard-switched power transistor are analyzed referring to a leg. Then, in Sect. III, the proposed AGD is introduced, and its effectiveness experimentally assessed in Sect. IV. The proposed method is then explained in Sect. V, and experimentally validated in Sect. VI. Concluding remarks are drawn in Sect. VII.

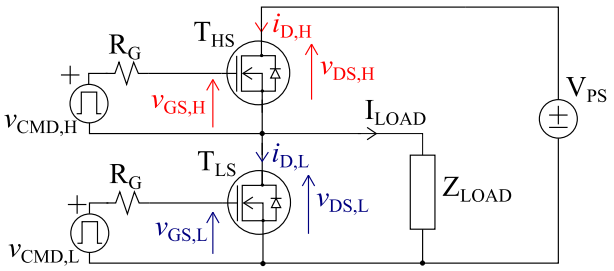

Fig. 1. Switching leg circuit. Transistors $T_{\rm HS}$ and $T_{\rm LS}$ are periodically turned on and off to supply an inductive load.

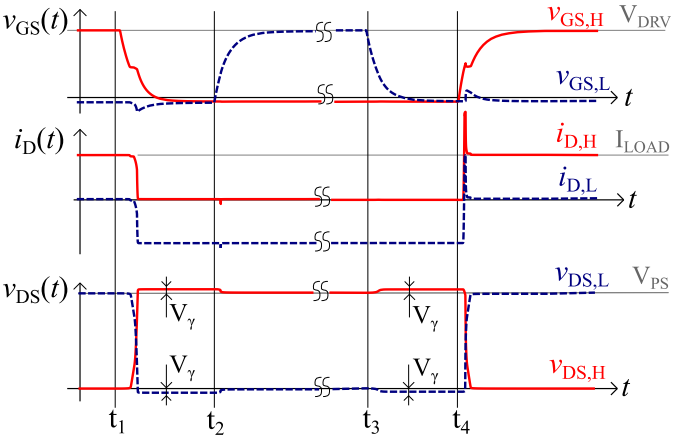

Fig. 2. Time domain waveforms referring to the circuit shown in Fig. 1. Solid lines refer to high side transistor ($T_{\rm HS}$), dashed lines to low side one (T_{LS}).

II. Switching Transients in a Half Bridge

Aiming to discuss the switching trajectories of power transistors, a hard switched leg is considered, as shown in Fig. 1. Such a circuit is of the utmost importance in power electronics as it is a basic building block for several topologies. It comprises of a high side ($T_{\rm HS}$) and a low side ($T_{\rm LS}$) power transistor, which are turned on and off to transfer power from the DC bus, modeled by an ideal voltage source ($V_{\rm PS}$), to an inductive load ($Z_{\rm LOAD}$). The power transistors are driven by two Conventional Gate Drivers (CGDs), represented by their Thevenin's equivalent ($v_{\rm CMD}, R_{\rm G}$). The voltage and current waveforms of $T_{\rm LS}$ and $T_{\rm HS}$ are shown in Fig. 2 by dashed and solid lines, respectively. The turn on and turn off commands ($v_{\rm CMD,L}$ and $v_{\rm CMD,H}$) are not overlapped, but some dead time is inserted in between to avoid cross conduction. At time $t = t_1$, $T_{\rm HS}$ is turned off by a high to low transition of $v_{\rm CMD,H}$. As $T_{\rm LS}$ is still off, the drain source voltage of $T_{\rm HS}$ ($T_{\rm LS}$) increases (decreases) to $V_{\rm PS}$ (zero), causing the turning on of the $T_{\rm LS}$ body diode. At this point, the load current is entirely diverted from $T_{\rm HS}$ to the $T_{\rm LS}$ body diode. Then, after a dead time equals to $t_2 - t_1$, $T_{\rm LS}$ is turned on, meaning that its body diode turns off and T_{LS} enters the triode region in the third quadrant, provided that $I_{\rm LOAD}$ is positive. When $T_{\rm LS}$ is turned off ($t = t_3$), $T_{\rm HS}$ is still interdicted,

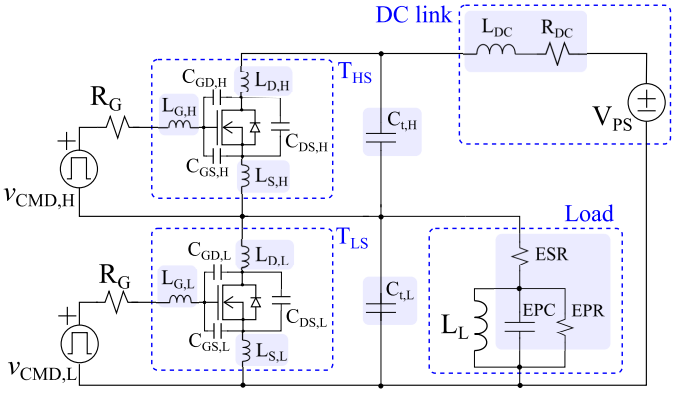

Fig. 3. Half bridge circuit complemented with parasitic elements of active switches, DC link and inductive load. Capacitive and inductive parasitics have been highlighted to be found at a glance.

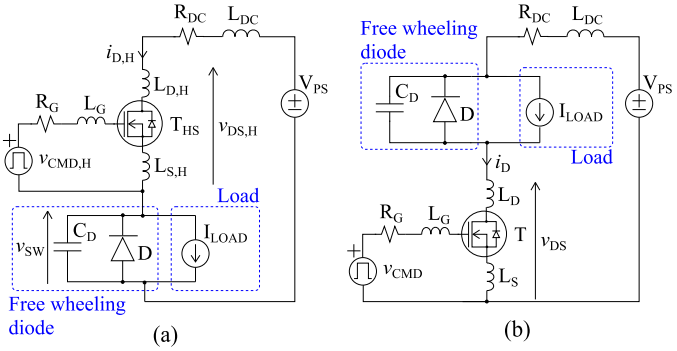

Fig. 4. (a) Simplified model for the turn on and turn off analysis of $T_{\rm HS}$ for the considered application. Such circuit can be further rearranged in that shown in (b).

therefore the body diode of $T_{\rm LS}$ turns on again, allowing the load current to flow. Finally, $T_{\rm HS}$ is turned on at $t = t_4$ to charge the load inductance, resulting in a $V_{\rm PS}$ and $I_{\rm LOAD}$ variation on the switching voltage and current, respectively. During this transient, the turning off of the low side switch is not immediate, as its body diode experiences reverse recovery. Although both $T_{\rm HS}$ and $T_{\rm LS}$ are turned on and turn off every half switching period, this brief analysis shows that only the $T_{\rm HS}$ commutations should be of interest for the the control of the output switching waveforms.

However, the curves shown in Fig. 2 refer to a rather ideal circuit, as parasitic elements have not been considered. To account for them, the circuit shown in Fig. 1 was modified, resulting in that shown in Fig. 3, with the parasitic elements highlighted. More precisely, inductances related to the packaging and interconnects of power transistor terminals (L_S, L_G, L_D) and to the DC link ($L_{\rm DC}$) have been included. Capacitances of active devices have been highlighted as well ($C_{\rm GS}, C_{\rm GD}, C_{\rm DS}$), together with those related to the switching node and the supply rails ($C_{\rm t,H}, C_{\rm t,L}$). Also the inductive load (L_L) was complemented with its series resistance (ESR), parallel resistance (EPR) and capacitance (EPC) [26].

The value of these parasitic elements is strictly related to the specific layout and to the exploited power switches. In medium-voltage automotive applications, power circuits are supplied by the 48 V bus, and their typical power rating is around 1 kW. Thus, MOSFET transistors are usually preferred. As far as 80-150 V power MOSFETs encapsulated in an SMD package, e.g., TO-263, are concerned, their output capacitance is around a few nF. The overall parasitic inductance is mainly determined by the size of the switching loop, i.e., the one encompassing $T_{\rm HS}, T_{\rm LS}$ and the DC link. For a square loop, such an inductance can be estimated as

$$L_{\rm SQ} \approx 2\frac{\mu_0}{\pi} l \left(\ln \frac{l}{r_w} - 0.774 \right), \qquad (1)$$

where l is the side of the square, r_w the wire radius and it is assumed that $l >> r_w$ [27]. For a loop with a side of a few centimeters, it results an $L_{\rm SQ}$ of approximately tens nH. The frequency of oscillations triggered at the turn on and the turn off of $T_{\rm HS}$ depends on the loop inductance and the output capacitance of active devices. Thus, this simple count results in an oscillation frequency of 10s MHz, which is in good agreement with the 10-60 MHz range found in the literature [4], [28]. With the purpose of discussing more in details the $T_{\rm HS}$ transients, the circuit shown in Fig. 3 can be simplified in the model reported in Fig. 4(a). The low side transistor has been replaced by an ideal diode (D) in parallel with a capacitance $C_{\rm D}$ to account for the junction capacitance of the $T_{\rm LS}$ body diode. For the sake of simplification, $L_{\rm D,L}, L_{\rm S,L}$ shown in Fig. 3 have been neglected as for the considered application they are typically much smaller than the loop inductance. About the inductive load (see Fig. 3), it is modeled by the impedance

$$Z_{\rm LOAD}(\omega) = ESR + \frac{j\omega L_{\rm L}}{1 + j\omega \frac{L_{\rm L}}{EPR} - \omega^2 L_{\rm L} EPC}. \qquad (2)$$

Thus, low frequency components of the load current flow though $L_{\rm L}$, whether high frequency ones through EPC. However, in practical applications EPC is typically much smaller then the output capacitance of active switches, meaning that it can be neglected. As transients are much shorter than the switching period, this means that the current flowing in $L_{\rm L}$ can be approximated as constant and equals to its DC value ($I_{\rm LOAD}$). Therefore, the load is modeled by a constant current source $I_{\rm LOAD}$. Similarly to the EPC, the parasitic capacitances $C_{\rm t,H}, C_{\rm t,L}$, which are related to the PCB layout, have not been considered as they are usually much lower than those of the switches. The model shown in Fig. 4(a) can be rearranged in that of Fig. 4(b), as high side and low elements are in series. Indeed, the turn on and turn off of the high side transistor shown in Fig. 3 can be analyzed referring to the simplified model reported in Fig. 4(b), as the $T_{\rm HS}$ switching trajectory is the same experienced by T.

A. Turn on and turn off oscillations

The turn on transient of transistor T can be analyzed referring to the switching waveforms reported in Fig. 5(a). At $t = t_0$, the $v_{\rm CMD}$ command goes high, and the $v_{\rm GS}$ voltage increases exponentially. As soon as $v_{\rm GS}$ reaches the T threshold voltage ($V_{\rm TH}$) at $t = t_1$, the transistor enters the saturation region, causing the drain current ($i_{\rm D}$) to increase. The drain source voltage $v_{\rm DS}$ decreases because of the voltage drop

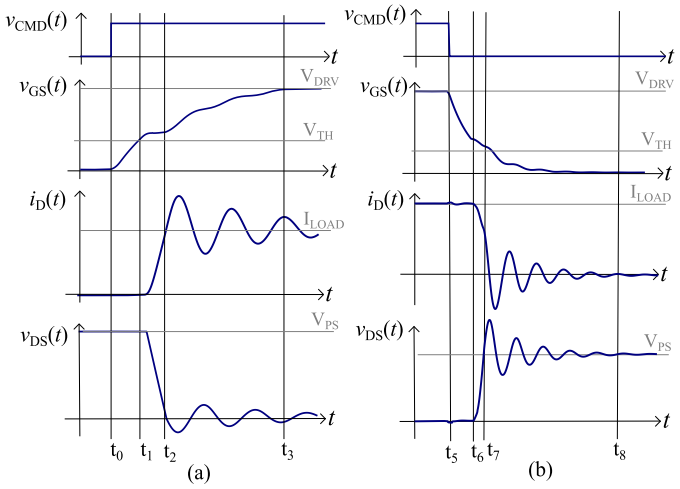

Fig. 5. Switching waveforms related to the (a) turn on and (b) turn off of the T transistor in the simplified model shown in Fig. 4.

across L_D, L_S, L_{DC} and of the discharge of $C_{\rm GD}$ through $R_{\rm G}$. More precisely, as far as T is in the Miller region, one can write

$$\frac{dv_{\rm DS}(t)}{dt} = -\frac{V_{\rm DRV} - V_{\rm GS}}{R_{\rm G} C_{\rm GD}} = -\frac{i_{\rm G}(t)}{C_{\rm GD}}. \tag{3}$$

For $t < t_2$, the load current flows in the diode D. However, with the $i_{\rm D}$ current equals to $I_{\rm LOAD}$ at $t = t_2$, the diode turns off. Capacitance C_D has to be charged to $V_{\rm PS}$, and this voltage step can excite the resonant circuit comprising the parasitic inductances and the capacitances to be charged. Such oscillations have been extensively studied, and several models are available in the literature [4], [6], according to which the circuit shown in Fig. 4(b) can be simplified to a second-order RLC series. In that case, by defining $L_{\rm LOOP}$ and $R_{\rm LOOP}$ as the overall inductance and resistance included in the output loop, one can derive $i_{\rm D}(t)$ under undamped conditions as

$$i_{\rm D}(t) = e^{-\alpha t}(A_1 cos\omega_{\rm d} t + A_2 sin\omega_{\rm d} t), \tag{4}$$

where the attenuation (α) and the damped natural frequency (ω_d) can be expressed as

$$\alpha = \frac{R_{\rm LOOP}}{2L_{\rm LOOP}}, \quad \omega_d = \sqrt{\frac{1}{(C_{\rm D} L_{\rm LOOP})^2} - \alpha^2}. \tag{5}$$

Coefficients A_1, A_2 depend on boundary conditions, i.e., initial values of $i_{\rm D}(t)$ and $di_{\rm D}(t)/dt$ [4]. Eqn. (4) quantifies the exponentially decaying oscillations shown in Fig. 5(a) for $t > t_2$. It is worth noticing that, although T is in the ohmic region, $v_{\rm DS}$ is affected by oscillations due to $L_{\rm D}, L_{\rm S}$.

Similarly to the turn on, also the turn off of transistor T can be discussed referring to the circuit shown in Fig. 4(b) and to the waveforms in Fig. 5(b). With $v_{\rm CMD}$ turned off $t = t_5$, the output waveforms remain constant until $t = t_6$. At this point, the channel current equals the load one, thus the output capacitance of the free wheeling diode discharges to zero. The drain current, which is the sum of load current (constant) with the one flowing in $C_{\rm D}$, decreases as $C_{\rm D}$ is discharging. At $t = t_7$, the voltage $v_{\rm DS}$ equals the input supply voltage, meaning that D turns on, shorting $C_{\rm D}$. The load current is now flowing in the diode, and $i_{\rm D}$ should step down to zero. However, the parasitic inductance in the power loop is still charged, and this current step can trigger the resonance with the output capacitance of the transistor. Also in this case one can derive $i_{\rm D}(t)$ as (4), with the foresight to substitute $C_{\rm D}$ with the T output capacitance in (5). Both for turn on and turn off, the higher the overshoot and undershoots on $v_{\rm DS}$, the higher the oscillation amplitude is.

B. Sensitivity to switching parameters

From the previous analysis, it appears that frequency and decaying factor of oscillations depend on the equivalent inductance, capacitances and resistance characterizing the switching loop. Coefficients A_1, A_2 include both initial and final values, i.e., $I_{\rm LOAD}$ and $V_{\rm PS}$ for $i_{\rm D}$ and $v_{\rm DS}$, as well as the initial di/dt. This current derivative in turn depends on the threshold voltage, the transconductance and the capacitance values of the transistor. As previously mentioned, these parameters are affected by process variations, temperature, and they are strongly related to the considered test case. Overshoot, ringing and switching losses are affected and, consequently, a spread of the switching trajectories occurs [29]. As the above mentioned parameters are not typically under the designers' control, model-based and sequential AGDs proposed so far exploit some interpolated relations or LUTs to get the most suited modulation pattern.

In previous investigations, the AGD control parameters were obtained by simulation to attain non oscillating waveforms with minimum switching losses [30], [31]. However, such a method failed when applied to a real test case, due discrepancies of simulation models. A different approach was later investigated. It is not based on models, and it does not require parameters related to the active devices or to the particular power circuit. The result of this second approach is the method presented in this paper, which is entirely implemented by the AGD controller on-the-fly. This is based on the $v_{\rm DS}$ undershoot and overshoot reduction at the turn on and turn off, respectively. By combining the developed algorithm with a low complexity AGD, oscillations amplitude can be reduced independently from variations of operating conditions or parameter spread.

III. Proposed Active Gate Driver

In order for the proposed method to control overshoots and undershoot cycle by cycle, a low complexity AGD is required. In such a way, the controller can tune the AGD parameters on-the-fly. From the previous transient analysis, an AGD should be able to slow down the driven transistor when turn on and turn off oscillations are being triggered. This means that the power transistor is exploited as a dissipative element to damp oscillations. Independently from the actual topology, AGDs are based on the modulation of gate charge. The exploited circuit, which was previously introduced in [32], [33], is shown in Fig. 6. Such an AGD is controlled by four on-off signals, named $v_{\rm ON1}, v_{\rm ON2}$ and $v_{\rm OFF1}, v_{\rm OFF2}$. The former are active during the turn on, the latter during the turn off, and they

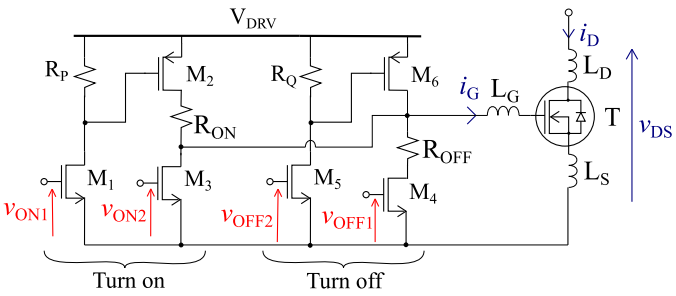

Fig. 6. Circuit of the proposed AGD, which is able to slow down the power transistor during its turn on and turn off.

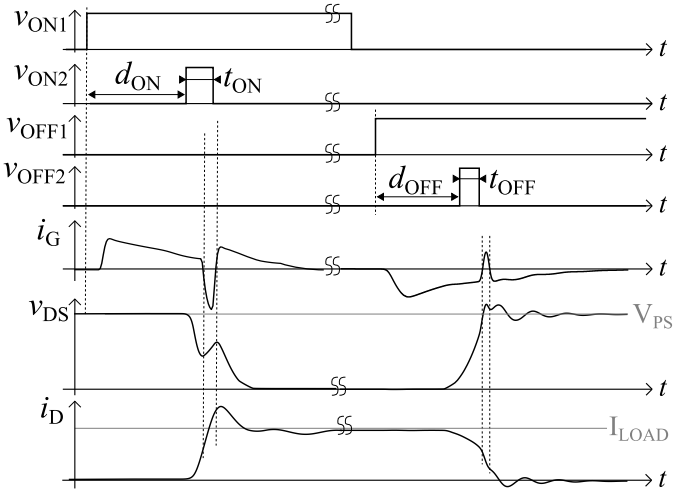

Fig. 7. Timing of the AGD control signals and output switching waveforms. By activating v_{ON2} (v_{OFF2}) during the turn on (off) commutation, it is possible to sink (inject) current from (to) the gate terminal to slow down T.

are all generated by the AGD controller (not shown in Fig. 6). Referring to Fig. 7, one can discuss the working principle of such an AGD for the turn on (left) and turn off (right) of the power transistor. It is assumed a suitable timing of the control signals, and that the AGD circuit is inserted in the simplified model shown in Fig.4(b). As far as the T turn on is concerned, the rising edge of v_{ON1} causes M_1, M_2 to switch from interdiction to the ohmic region, resulting in a positive gate current (i_{G}). Thus, T enters the saturation region and a drain current (i_{D}) flows. After a delay d_{ON}, the v_{ON2} signal is activated too, turning on transistor M_3. Due to the presence of R_{ON}, the current provided by M_2 is lower than that sunk by M_3, meaning that the gate current decreases even though M_1, M_2 are on. Transistor M_3 is kept on for a period t_{ON}, thus resulting in $i_{\mathrm{G}} < 0$, as shown in Fig. 7. Recalling (3), the time derivative of voltage v_{DS} is directly controlled by the gate current with T in saturation. Thus, a negative gate current causes v_{DS} to increase locally during its fall transient. In such a way T is slowed down, as its extra power losses are exploited to increase the resulting damping factor. When v_{ON2} is driven low, M_3 turns off and M_2 continues to inject an $i_G > 0$ until the gate-source voltage reaches V_{DRV}. As far as the turn off of the driven transistor is concerned, v_{ON1} is turned off, and v_{OFF1} is driven high, leading the T input capacitance to discharge. The control signal v_{OFF2} is then activated after a

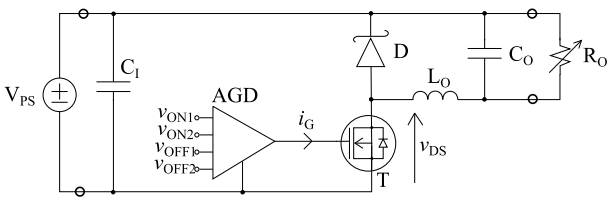

Fig. 8. DC-DC converter designed assess the AGD shown in Fig. 6. It is an asynchronous low side Buck converter.

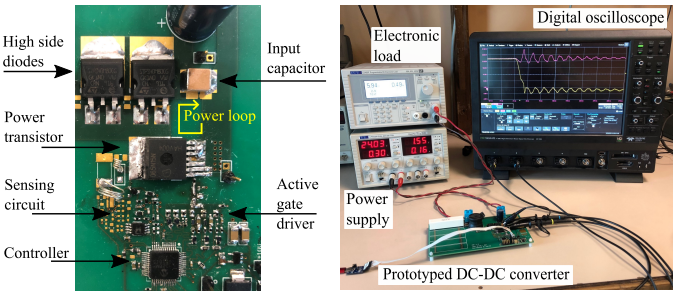

Fig. 9. Photograph of (a) the prototyped AGD and the switching loop, (b) the test bench exploited.

delay d_{OFF} when v_{DS} is approximately V_{PS}, as shown in Fig. 7 on the right. More precisely, with $i_{\mathrm{G}} >0$, the drain current increases, and it counteracts the i_{D} step, which would cause the oscillation triggering. As a result, the v_{DS} voltage locally decreases, and its overshoot is reduced. In such a way, the AGD can damp the turn off oscillation as well. Then, after a t_{OFF}, as shown in Fig. 7, v_{OFF2} is driven low and the turn off process end through M_4. The timing of the control signals, i.e., the value of $t_{\mathrm{ON}}, d_{\mathrm{ON}}, t_{\mathrm{OFF}}, d_{\mathrm{OFF}}$, determines the amount of charge injected and sunk in the different stages of the turn on and turn off. Therefore, the timing of these signal is crucial in shaping the switching trajectory of T.

IV. Undershoot Mapping

With the purpose of assessing such an AGD, it was included in an asynchronous low side Buck converter to drive the power transistor T, as shown in Fig. 8. A photograph of the experimental test bench is shown in Fig. 9(b), with the main components labeled. The proposed AGD is located close to T, and it was prototyped exploiting discrete components only, as shown in Fig. 9(a). With the AGD parameters $d_{\mathrm{ON}}, t_{\mathrm{ON}}$ in the (10,50) ns range, all combinations were tested. The resulting color maps are shown in Fig. 10, in which (a) refers to the v_{DS} undershoot with the Buck operating at I_{LOAD}=3 A and V_{PS}=48 V, and (b) to the magnitude of the v_{DS} spectrum at the turn on oscillation frequency (f_{ON}=36 MHz). From Fig. 10(a), more than a darker region, i.e., characterized by a small value of v_{DS} undershoot, occur.

The waveform corresponding to the central point of the leftmost darker region (circle marker in Fig. 10(a)) is shown in Fig. 11(a) by solid line and that related to the center region (diamond marker) by dashed line. Both of them are characterized by a v_{DS} local increase, as predicted in Sect. III, and resulted in non-oscillating waveforms. Such a local

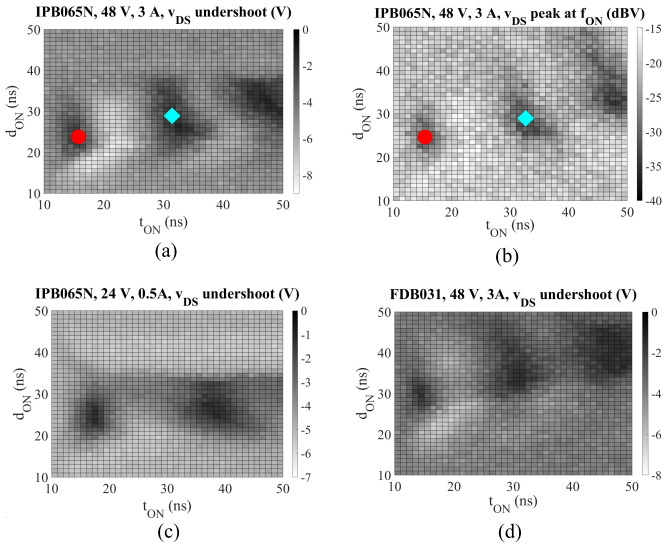

Fig. 10. Color maps reporting (a) the $v_{\rm DS}$ undershoot and (b) the magnitude of the $v_{\rm DS}$ frequency spectrum at $f_{\rm ON}$ with $V_{\rm PS}$=48 V and $I_{\rm LOAD}$=3 A. The undershoot is also reported in (c) in case of $V_{\rm PS}$=24 V and $I_{\rm LOAD}$=0.5 A, and in (d) with a different power transistor exploited.

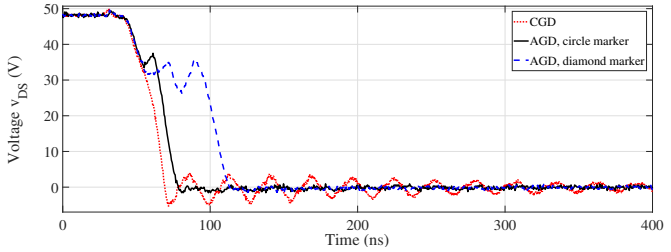

Fig. 11. Comparison between the $v_{\rm DS}$ waveforms for the CGD (dotted) and the AGD with different set of parameters. Solid and dashed lines refer to the circle and diamond marker of Fig. 10(a), respectively.

increase is the effect of the gate current modulation, and the solid line is in agreement with the $v_{\rm DS}$ shown in Fig. 7. Finally, the $v_{\rm DS}$ voltage obtained by exploiting the proposed AGD as a CGD, i.e., with $v_{\rm ON,2}$ not turned on, is reported in dotted line for comparison. The solid curve should be preferred as its $v_{\rm DS}$ fall time is lower than that related to the dashed curve, meaning that oscillations are damped with a lower losses increase. Such an aspect can be explained as the longer the $v_{\rm DS}$ local increase, the longer the switching time will be. Similarly, with a $d_{\rm ON}$ too small, the current sinking is ineffective, as T is interdicted, whether with $d_{\rm ON}$ too high, T is already in the ohmic region. As a consequence, the AGD parameters affect the switching losses of the power transistor, thus the conversion efficiency of the converter. Indeed, with ($d_{\rm ON}$, $t_{\rm ON}$) corresponding to the diamond marker, the measured efficiency was equal to 91.2 %, and with those corresponding to the circle marker, the efficiency dropped to 90.7 %. The darker regions in the $v_{\rm DS}$ undershoot also corresponds to minima in the corresponding frequency spectrum, as the color map shown in Fig. 10(a) is in good agreement with that in Fig. 10(b). Indeed, the position of local minima, which is identified by markers in the two subplots, is the same. With the operating conditions modified, such local minima still occur, but their position is

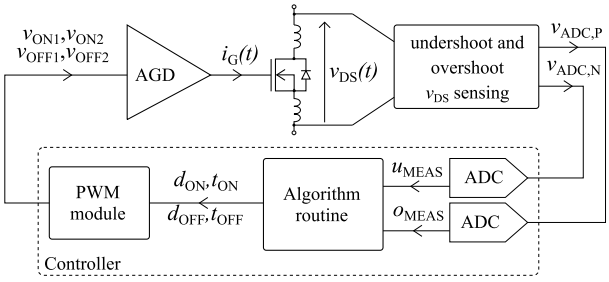

Fig. 12. Scheme representing the sub-blocks of the proposed adaptive method.

different. For example, with $I_{\rm LOAD}$=0.5 A and $V_{\rm PS}$=24 V, the undershoot color map is shown in Fig. 10(c). This is quite different from that in (a), and it is in accordance with the results reported in [33]. Recalling Sect. II-A, different $I_{\rm LOAD}$ and $V_{\rm PS}$ result in a different oscillation amplitude, meaning that the T trajectory should be modified accordingly. Finally, the driven power transistor [34] was substituted with a different one, which is in the same package but is characterized by a higher input capacitance [35]. In this case, the undershoot color map is reported in Fig. 10(d), and similarly to (c), the local minima occur with different set of AGD parameters.

To sum up, the AGD effectiness was assessed, as it was able to damp oscillations. Several combinations of AGD parameter resulting in non oscillating waveforms occur. However, they are not equivalent in terms of power losses. By considering the left most minimum, i.e., that corresponding to the lowest $t_{\rm ON}$, the set of AGD parameters is not fixed, but it is affected by several parameters, which can be hardly considered analytically altogether.

V. Sequential Adaptive Method

The developed adaptive method combines the measurement of the $v_{\rm DS}$ undershoot with a minimum search algorithm. This can be implemented on a resource-limited digital controller, e.g., a microcontroller. As previously discussed, the $v_{\rm DS}$ undershoot depends on the amplitude of oscillations, meaning that it can be exploited to assess the presence of ringing. The block scheme of the proposed architecture is shown in Fig. 12. A sensing circuit is exploited to measure the undershoot and overshoot affecting the $v_{\rm DS}$ voltage, which are then converted into a digital value by means of two Analog-To-Digital Converters (ADCs). The measured values of undershoot (u_{meas}) and overshoot ($o_{\rm meas}$) are fed to the minimum search algorithm, which exploits such data to modify the AGD timing parameters. A Pulse-Width Modulator (PWM) outputs the AGD control signals, eventually. For the sake of concisenesses, the proposed method is discussed referring to the turn on only, but the same procedure holds at the turn off as well.

A. Undershoot/overshoot voltage sensing

A negative peak detector ($D_{\rm H}, C_{\rm H}$) followed by a differential amplifier is exploited, as shown in Fig. 13, to measure the $v_{\rm DS}$ undershoot. When the power transistor is steadily off, the voltage across the hold capacitance ($v_{\rm PN}$) is about zero as

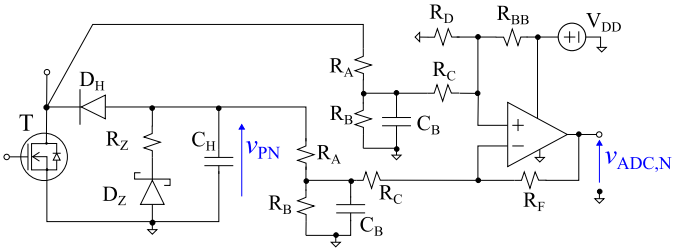

Fig. 13. Sensing circuit exploited to measure the v_{DS} undershoot.

C_{H} has discharged through R_{Z}. This means that the opamp output ($v_{\mathrm{ADC,N}}$) is saturated to the positive supply voltage as $v_{\mathrm{DS}} = V_{\mathrm{PS}}$. As T is turned on and the v_{DS} undershoot occurs, the voltage v_{PN} decreases equaling the v_{DS} minimum expect for the voltage drop across the diode D_{H}, which is named V_{Dh} hereinafter. With the turn on oscillation decaying exponentially, the voltage across C_{H} remains constant. At the same time, the opamp experiences an under damped transient due to its limited slew rate. Then, as long as the power transistor is steadily on, the amplifier output equals the difference between v_{DS}, which is approximately zero, and v_{PN}.

Once the power transistor is turned off, $v_{\mathrm{ADC,N}}$ saturates again. In order to acquire a meaningful value of v_{PN}, the voltage $v_{\mathrm{ADC,N}}$ should be sampled with T is steadily on. Thus, with $v_{\mathrm{ADC,N}}$ acquired Δt_{ADC} after the v_{ON1} rising edge, it is

$$u_{\mathrm{MEAS}} = \frac{v_{\mathrm{ADC,N}}(t_1) - V_{\mathrm{B}}}{\left(\frac{R_{\mathrm{A}}}{R_{\mathrm{A}}+R_{\mathrm{B}}}\frac{R_{\mathrm{F}}}{R_{\mathrm{C}}+(R_{\mathrm{A}}||R_{\mathrm{B}})}\right)\left(1-\frac{\Delta t_{\mathrm{ADC}}}{R_{\mathrm{Z}}C_{\mathrm{H}}},\right)} + V_{\mathrm{Dh}}, \tag{6}$$

where V_{B} is an offset added to the opamp output, the discharge of the hold capacitance is linearly approximated, and it is assumed $R_{\mathrm{F}} = R_{\mathrm{BB}}||R_{\mathrm{D}}$.

B. Minimum search algorithm

On the basis of $u_{\mathrm{MEAS}}, o_{\mathrm{MEAS}}$, the algorithm should determined the AGD parameters to attain non oscillating transients. As suggested in previous works, this problem can be thought of as a minimum search [10], [11], for which several algorithms are available [36]. Those methods require the definition of a cost function, which should include both the switching energy and the oscillation amplitude for the considered application. Referring to Fig. 10(a) and 11, the selection of the left-most local minimum resulted in a non oscillating waveform. The resulting switching trajectory is characterized by the lowest losses, as the v_{DS} fall time is lower. Thus, it is possible to exploit the v_{DS} undershoot itself as the cost function to be minimized, provided that the algorithm can track the left most minimum. To this purpose, the method is divided into two steps, which are described in what follows.

1) Left-most minimum detection: This step is executed once at the power on with the aim of approximately locating the left most minimum. The AGD controller tests all possible values of $d_{\mathrm{ON}}, t_{\mathrm{ON}}$ in the $(d_{\mathrm{ON,MIN}}, d_{\mathrm{ON,MAX}}), (t_{\mathrm{ON,MIN}}, t_{\mathrm{ON,MAX}})$ ranges with a coarse time step, and store the corresponding u_{MEAS} values in the microcontroller. Then, such a matrix

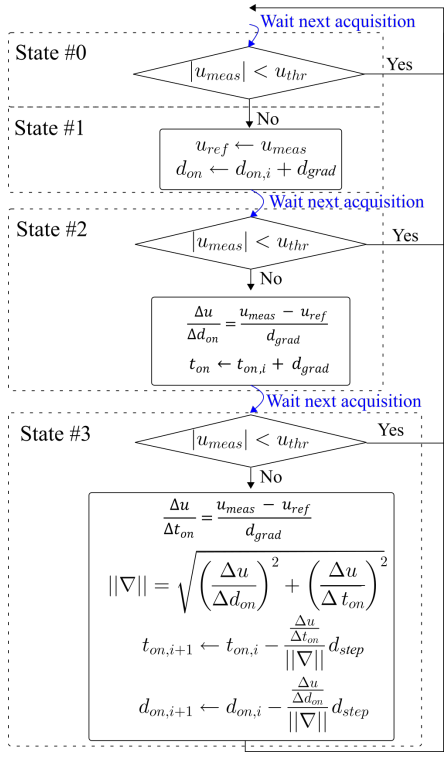

Fig. 14. Flowchart of the control algorithm during the minimum tracking phase.

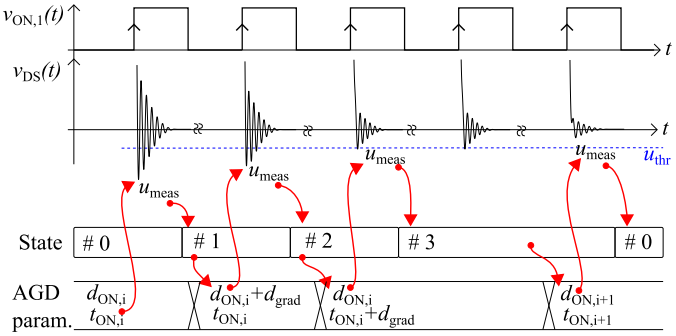

Fig. 15. Timing of the control algorithm during the tracking phase applied to the power transistor turn on.

is scanned to find all local minima by exploiting an $O(N^2)$ algorithm. The minimum with the lowest t_{ON} is considered, and its coordinates are taken as the starting point of the next step. It is worth noticing that such an operation is performed only once at the power on, and it is required to account for parameter spread. By choosing a fixed initial set of AGD parameters, e.g., by inspection of the color map shown in Fig. 10(a), or a random set, the algorithm may converge to a local minimum different than the left-most one, and result in higher switching losses. As the position of such minimum is affected by several parameters, this first step allows the AGD to detect it autonomously.

2) Minimum tracking: With the initial set of AGD parameters defined, a gradient method can be applied to refine them further and to track the minimum undershoot under variations of operating conditions. By defining a target u_{THR},

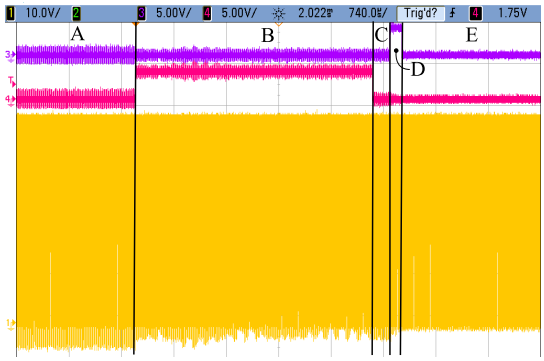

Fig. 16. Oscilloscope screen shot showing the convergence of the proposed algorithm at the power on. Channel 1 was connected to measure $v_{\rm DS}$, 3 and 4 to debug outputs of the microcontroller.

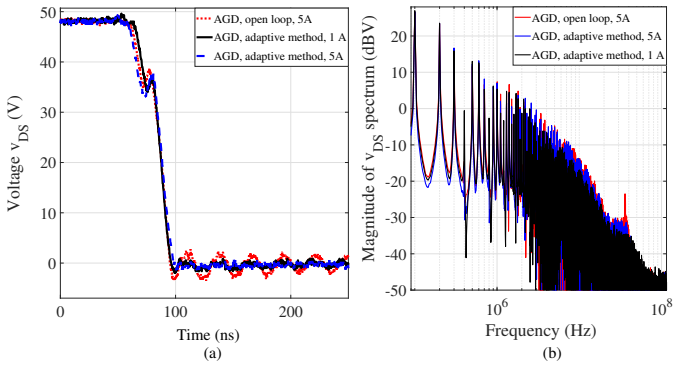

Fig. 17. Comparison of the $v_{\rm DS}$ in (a) time and (b) frequency domain for the AGD exploiting the adaptive method with 1 A (solid), and 5 A (dashed) load current. Dotted line refers to an open loop AGD tuned at 1 A and then exploited at 5 A.

the gradient method modifies the AGD parameters to attain a $u_{\rm MEAS}$ lower or equal than $u_{\rm THR}$. This algorithm can be discussed referring to the flowchart shown in Fig. 14, and to the timing diagram reported in Fig. 15. After a $\Delta t_{\rm ADC}$ delay from each T turn on transient, a new $u_{\rm MEAS}$ sample is available from the ADC peripheral. With $u_{\rm MEAS} > u_{\rm THR}$ and AGD parameters equal to $d_{\rm ON,i}, t_{\rm ON,i}$, the algorithm moves from state #0 to #1, and the current undershoot is stored in $u_{\rm REF}$ as reference. Before the next T turn on, the $d_{\rm ON}$ parameter of the AGD is increased by $d_{\rm grad}$. As the new $u_{\rm MEAS}$ is available, the discrete partial derivative of $u_{\rm MEAS}$ with respect to $d_{\rm ON}$ is evaluated, and the $t_{\rm ON}$ value increased by $d_{\rm grad}$. At the next switching cycle, the partial derivative of $u_{\rm MEAS}$ with respect to $t_{\rm ON}$ is evaluated, and the local gradient ($||\nabla||$) can be estimated. Thus, the new AGD parameters are modified according to the direction, which minimizes the undershoot the most. Finally, the algorithm moves back to state # 0. Such a procedure is performed $k_{\rm item}$ times, i.e., until an undershoot value lower than the threshold is found.

VI. Experimental validation

The DC-DC converter and the experimental setup introduced in Sect. IV were used again to validate the adaptive method. With the algorithm converged to a proper solution, a comparison with the same AGD exploited in an open loop manner, is carried out under load current variations. Then, the transient response of the proposed method is investigated to estimate the convergence time of the algorithm. Finally, the proposed method is set against the use of a standard technique to suppress ringing.

A. Assessment of the proposed algorithm

The search algorithm described in Sect. V-B was implemented on the microcontroller enslaved to the AGD. This controller can output $v_{\rm ON,1}, v_{\rm ON,2}, ..$ with a 250 ps time resolution, and it was set $\Delta t_{\rm ADC}$=1 μs. In Fig. 16, the waveforms related to the proposed algorithm are shown, and each step identified by a letter (A,..,E). During step A, the AGD was not tuned, and when the algorithm started to run, it detected the position of left most minimum. To this purpose, it was set $d_{\rm ON,MAX}$=$t_{\rm ON,MAX}$= 50 ns and a coarse time step of 2 ns exploited. As the power transistor is turned on and off with a 100 kHz switching frequency, the time required to test all $d_{\rm ON}, t_{\rm ON}$ values was equal to 3.3 ms. This is the duration of step B indeed. It is worth noticing that the $v_{\rm DS}$ undershoot is not constant, but it varies as the AGD parameters are modified cycle by cycle. The algorithm scanned the matrix in step C and found an approximated position of the left most local minimum. It resulted a $d_{\rm ON}$=25 ns and $t_{\rm ON}$=13 ns for the Buck operating at $V_{\rm PS}$= 48 V and $I_{\rm LOAD}$= 1 A. Then, the undershoot affecting the $v_{\rm DS}$ voltage was reduced from 1.54 V to 1.4 V during the tracking phase (D step) in 170 μs. The parameters of the gradient method were set to $u_{\rm THR}$=1.4 V, $d_{\rm grad}$=1.5 ns, $d_{\rm step}$=1.5 ns. The time required by the microcontroller to execute one iteration of the procedure depicted in Fig. 14 was equal to $t_{\rm iter}$=40 μs, as three $u_{\rm meas}$ measurements are needed to evaluate a new set of AGD parameters and the last step (state #3) requires an extra switching cycle to complete the calculations. Indeed, four iterations of the procedure were required to obtain $u_{\rm meas} < u_{\rm thr}$ (step D in Fig. 16). As the algorithm was able to converge, it monitored the $v_{\rm DS}$ undershoot during step E.

B. Comparison with open loop AGD

The proposed adaptive method was later validated against load current variations, and compared to an open loop control. More precisely, at the end of step D, the resulting $v_{\rm DS}$ is shown in Fig. 17(a) by solid line for an initial current of 1 A. By increasing $I_{\rm LOAD}$ to 5 A, the algorithm modifies the $d_{\rm ON}, t_{\rm ON}$ values, resulting in the $v_{\rm DS}$ waveform shown by dotted line. Both curves are not affected by oscillations, and the corresponding frequency spectra, are not characterized by a peak at $f_{\rm ON}$, as shown in Fig. 17(b). On the contrary, with the AGD exploited in open loop, its parameters have been tuned at 1 A, and then the load current was increased. It resulted in the $v_{\rm DS}$ shown in Fig. 17(a) by dashed line. The corresponding undershoot is higher than in case of the adaptive method. By comparing the $v_{\rm DS}$ spectrum at 5 A, the peak related to the open loop control is 9 dB higher than with the adaptive method. Thus, the effectiveness of the presented technique was assessed under operating condition variations.

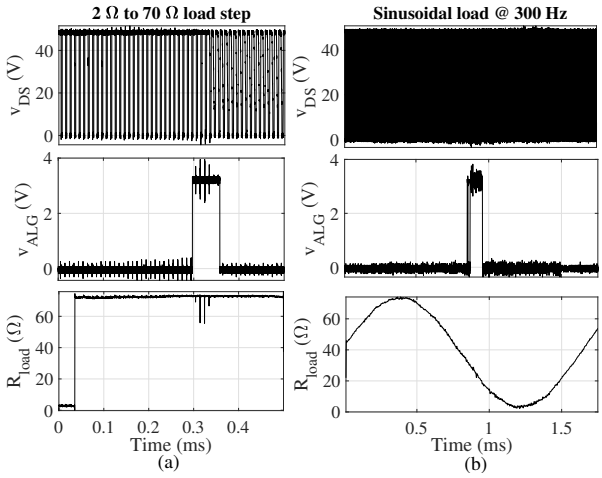

Fig. 18. Transient response of the adaptive method under (a) step and (b) sinusoidal variations of the load resistance.

TABLE I
COMPARISON BETWEEN CGD AND AGD, AT 48 V, 5 A

Setup	$v_{\rm DS}$ fall time	$v_{\rm DS}$ undershoot	$\lvert V_{DS}(j\omega)\rvert$ @$f_{\rm ON}$	η
CGD, $R_{\rm G}$=4.7 Ω	23.5 ns	-5.62 V	-18 dBV	91.2 %
CGD, $R_{\rm G}$=40 Ω	58 ns	-2.5 V	-27.5 dBV	88 %
AGD, $R_{\rm G}$=4.7 Ω	31 ns	-1.1 V	-31 dBV	91 %

C. Transient response under load variations

With the proposed method outperforming an open loop control of the AGD in steady state conditions, as discussed in Sect. VI.B, the transient response of the system was investigated. The time required by the algorithm to find a new set of AGD parameters depends on $t_{\rm iter}$, which for the considered setup is equal to 40 μs as discussed in Sect. VI.A, and on the number of iterations ($k_{\rm iter}$) required. The latter is in turn affected by the parameters of the gradient algorithm, i.e., $u_{\rm thr}$,$d_{\rm grad}$,$d_{\rm step}$ reported in Fig. 14, and by the initial set of $d_{\rm ON}, t_{\rm ON}$. Step and sinusoidal variations of the load were considered, as they are both of practical interest, resulting in the waveforms shown in Fig. 18(a) and (b), respectively. A digital output of the microcontroller ($v_{\rm ALG}$), which is driven high as long as the measured undershoot is higher than the threshold, was acquired by a digital oscilloscope to measure the time $k_{\rm iter}t_{\rm iter}$, i.e., the convergence time for load variations. As far as Fig. 18(a) is concerned, it corresponds to a 5 A to 0.2 A load current variations. In that case, the algorithm took 60 μs to find a new set of suitable AGD parameters. However, this time is not constant as it depends on the starting $d_{\rm ON}, t_{\rm ON}$ values. It was found that the convergence time spread in the [20 μs, 450 μs] range for both positive and negative current steps. Then, sinusoidal variations of the load were also investigated, as shown in Fig. 18(b). Also in this case, the algorithm was able to track the load variations on time, with the undershoot being higher than the threshold for approximately 10 % of the sine wave period.

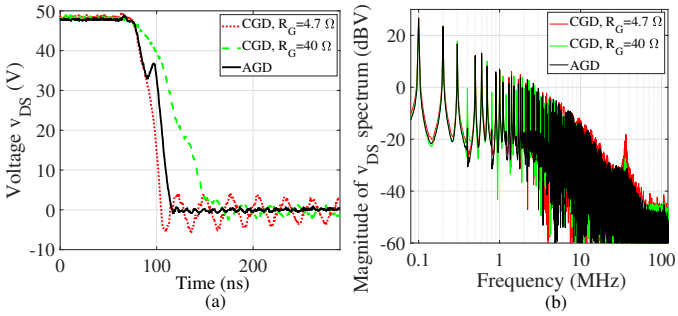

Fig. 19. Comparison of the $v_{\rm DS}$ in (a) time and (b) frequency domain for the AGD (solid) and the CGD with a gate resistance equal to 4.7 (dotted) and 40 Ω (dashed line) with 5 A load current.

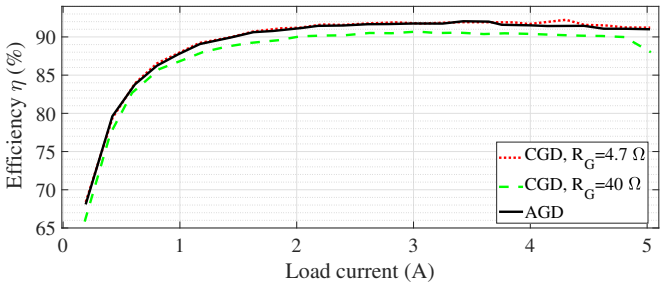

Fig. 20. Conversion efficiency of the Buck converter with the AGD (solid) and the CGD with a low (dotted) and high (dashed lines) gate resistance.

D. Comparison with standard solution

The method was also compared to a standard solution to limit over- and under- voltages, i.e., the tuning of the gate resistance. Indeed, with $v_{\rm ON2}, v_{\rm OFF2}$ not activated during transients, the designed AGD can be exploited as CGD, where the gate resistance ($R_{\rm G}$) is set by $R_{\rm ON}, R_{\rm OFF}$ shown in Fig. 6 for the turn on and turn off, respectively. The resulting waveforms are shown in Fig. 19 for (a) the time domain, and (b) the frequency domain with a 5 A load current. These curves have been experimentally acquired and then combined for convenience. With the lowest gate resistance, i.e., $R_{\rm G}$=4.7 Ω, the $v_{\rm DS}$ (dotted line) is affected by oscillations. The ringing is partially damped when a higher value (40 Ω) is exploited, as shown by dashed line. The $v_{\rm DS}$ curve is reported in solid line when the AGD is tuned by the adaptive method. This last waveforms is characterized by no peak at $f_{\rm ON}$ in the frequency domain. In order to compare further the two solutions, the values of $v_{\rm DS}$ fall time (90% to 10%), undershoot, magnitude of the frequency spectrum at $f_{\rm ON}$, and efficiency of the overall power converter are reported in Table I for a 5 A load current. More precisely, the efficiency was evaluated as the ratio between the power delivered to the load by the Buck converter and the input one. Although the last two cases ($R_{\rm G}$=40 Ω and AGD) are similar in terms of undershoot and frequency peak reduction, the corresponding $v_{\rm DS}$ fall time differs by 27 ns, which in turn results in a 3% lower efficiency than in case of the AGD. This aspect was further investigated, and the efficiency of the converter was measured for load current ranging from 0.2 A to 5 A. The results are shown in Fig. 20 for the AGD (solid) and the CGD with $R_{\rm G}$=4.7 Ω (dotted)

and 40 Ω (dashed line). The efficiency curve with the AGD exploited is overlapped with that with the oscillating CGD (R_{G}=4.7 Ω). Therefore, the proposed technique does not affect the conversion efficiency adversely. In contrast, with the CGD exploiting a 40 Ω gate resistance, the efficiency is lower than in case of the AGD for all load current higher than 1 A. To conclude, the discussed method resulted a better trade off between oscillations and losses than traditional solution.

VII. Conclusion

To limit over- and under- voltages during the transients of hard-switched power transistor, a low complexity AGD controlled by a novel adaptive method is described. Through the sensing of the v_{DS} undershoot and overshoot, the technique tunes the AGD parameters to attain damped waveforms with minimum switching losses. As the method was entirely implemented on a resource-limited microcontroller, the technique described in this paper is more robust than those proposed in literature, as it is not based on any a-priori calculations or on some knowledge of the particular case study. Indeed, with respect to previous work, a true adaptive control of the AGD modulation pattern is achieved, which can be exploited to address parameter spread due to process variation, aging and temperature, as well as variations of operating condition. Delays of the AGD are automatically compensated too, meaning that the method is robust against different power transistors or different performance of the AGD in a hard-switched leg. The method was experimentally assessed, and it resulted in better switching performance with respect to open loop AGDs and traditional solutions. The transient response of the method was assessed too, resulting in a convergence time which allows the proposed technique to be applied in practical applications. Moreover, the proposed system lends itself well to integrating the AGD, the sensing circuit and the required logic in a single chip.

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