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Modeling the electrical characteristic of InGaN/GaN blue-violet LED structure under electrical stress

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Abstract

The role of deep defects and their physical origin in InGaN/GaN LED are still widely investigated and debated, in particular their impact on the electrical and optical characteristics and on the reliability of the device. In this paper we evaluate the electrical and optical behaviour of a single quantum well InGaN/GaN 420 nm LED during a medium-term accelerated ageing test. From these measurements, an increase in the sub-turn on current was observed: this process was ascribed to the stress-induced generation of defects in proximity of the active region and thus related to an increase of the correlated trap assisted tunnelling. Subsequently we modelled the device electrical characteristics, evidencing the fundamental role of deep defects in determining the shape of the I-V curve in low forward bias. We reproduced with high accuracy the experimental current-voltage curves acquired during the ageing test, demonstrating that the increase in forward leakage can be entirely ascribed to the increase in concentration of a sole defect deep level located near midgap. These results provide a better understanding about the defect formation mechanism, that can be used to model and understand the behaviour of the devices during ageing.

1. Introduction

The presence of deep defects has a significant impact on the performance of InGaN/GaN Light-Emitting Diodes (LEDs). This defects in proximity of, or within the active region (AR), are in fact responsible for non-radiative recombination [1], and their presence impacts on the efficiency of the devices. In order to minimize defect-mediated recombination, different strategies have been proposed, including the use of InGaN or AlInN under layer (UL) grown below the AR, that results in the incorporation of point defects in buried semiconductor layers [2,3]. The presence of deep defects may impact on the optical performance of the devices, and influence the sub turn-on current characteristics, by causing trap assisted tunneling [4,5]. This mechanism becomes more marked during the ageing of the LED, leading to an increase in the forward leakage current. This latter is of great interest in commercial applications since it is correlated with device reliability, luminescence efficiency and electrostatic discharge sensitivity [6]. Moreover, since LED matrixes are increasingly being used as the backlight of modern displays and TVs, the variation of the optical (and electrical) characteristics of the emitter at very-low bias levels is becoming a critical issue in applications where the light intensity has to be dimmed by several orders of magnitude [7,8]. Having a correlation between defect generation and leakage current is of crucial importance for this kind of applications. In this paper we propose a model that reproduces with high accuracy the electrical characteristics of a InGaN/GaN single quantum well

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(QW) LED during a stress test. In a first step, we fabricated the LEDs and tested their reliability by means of a constant current stress test. Additionally, we defined a model for the current-voltage characteristics of the devices, considering trap-assisted tunneling as the main sub-threshold leakage mechanism and by leveraging on earlier studies on the topic [4,6–8]. The good matching obtained with the experimental data collected before and during stress allows to further clarify the role of the deep levels during device degradation.

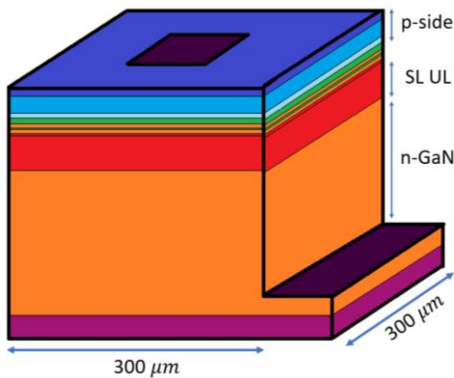
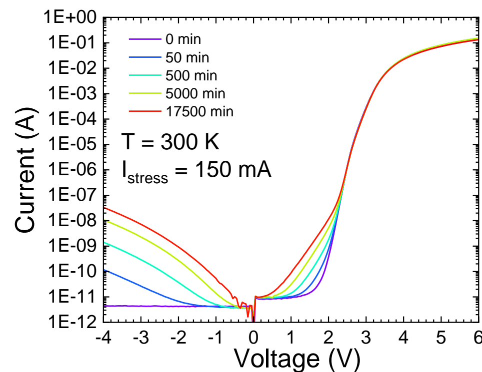


Figure 1: (a) Schematic representation of the structure of the LED analyzed within this paper and (b) a 3D sketch of the device.

2. Sample structure and fabrication

The LEDs, with an area of 300 x 300 µm^2, were grown on sapphire substrate by metalorganic vapor phase epitaxy (MOVPE). The epitaxial structure, reported in Figure 1, consists of a single 2.8 nm $In_{0.12}Ga_{0.88}N$ QW placed between two 7.5 nm barriers (N_D = 3 x 10^{18} cm^{-3}) and two spacers. The upper spacer is undoped and the lower one is over-doped (N_D = 1 x 10^{20} cm^{-3}). The typical emission wavelength of the devices is about 420 nm, at 110 A/cm^2. The precursors used for InGaN layer are triethyl-gallium (TEGa) and trimethyl-indium (TMIn) with nitrogen as a carrier gas. The 7.5 nm GaN barriers were grown in similar conditions. Between the over doped spacer and the n-doped GaN buffer (800 nm) with N_D = 3 x 10^{18} cm^{-3}, a super-lattice (SL) UL constituted of 24 layers of $Al_{0.17}In_{0.83}$/GaN (2.1 nm/1.7 nm) is included. These layers were grown at 770°C using trimethyl-aluminium and TMIn. In the underlayer, the first 22 layers have a doping concentration equal to N_D = 3 x 10^{18} cm^{-3}, whereas the last two ones are over-doped with N_D = 10^{20} cm^{-3}. Above the undoped spacer, a p-doped $Al_{0.06}Ga_{0.94}N$ layer was used as electron blocking layer (EBL) with N_A = 5 x 10^{18} cm^{-3}, followed by a p-doped 180 nm GaN layer with the same doping concentration. The anode contact is made of platinum, which is placed on top of a p-doped 20 nm GaN layer with N_A = 2 x 10^{19} cm^{-3}. The role of the undoped spacer adjacent to the p-doped EBL is to favor the extension of the depletion region toward the QW. On the other hand, the purpose of the overdoped spacer is improving carrier injection into the QW, since the lattice mismatch at the second AlInN/GaN interface increases spontaneous polarization leading to a high negative fixed charge density. This charge creates a barrier for electrons that is compensated by introducing the aforementioned overdoped layer [9,10].



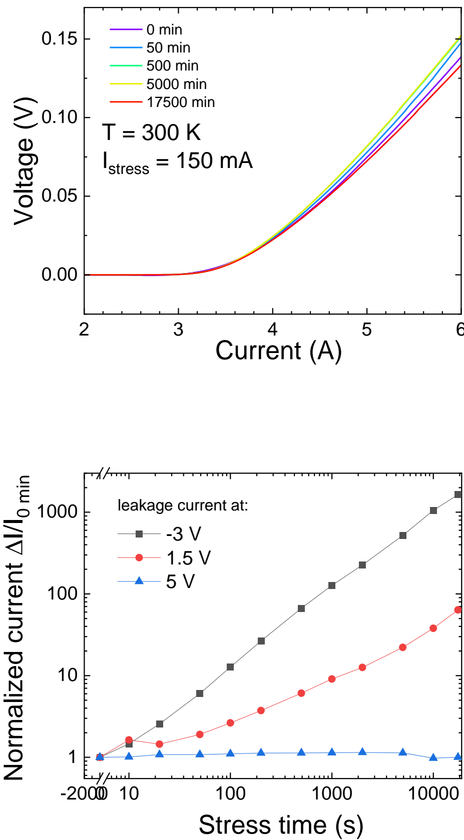


Figure 2: (a) Electrical characteristics of the device during the stress in semi-logarithmic scale and (b) linear scale. (c) An increase of the sub-threshold forward and reverse current is observed. The observed trends are monotonic.

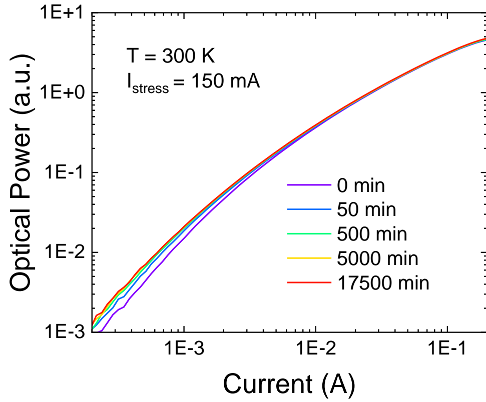
3. Results of the accelerated stress test

By means of a preliminary characterization, several tens of devices have been analyzed in order to select a single sample representative of the average characteristic of these LEDs. The selected device has been subjected to medium-term degradation tests, to evaluate the stability and to describe their electrical behavior during stress. A constant current stress has been performed at 150 mA (167 A/cm^2) for a duration of 17500 min. The stress current has been chosen based on the results of a preliminary step-stress, during which stress current has been gradually increased at 1 hour intervals, until device failure was reached (at about 420 mA). We also found that for stress current greater than 200 mA the contacts were exhibiting a fast and anomalous degradation, that brought the devices to an open circuit condition. The selected stress current of 150 mA was found to be a reasonable trade-off, which allowed us to evaluate the gradual degradation of the semiconductor material/device, without inducing catastrophic contact degradation. During the constant current stress, at logarithmically spaced time intervals, the electrical characteristics of the device were monitored by means of current–voltage (I–V) measurements, whereas the optical characteristics were analyzed through light-current (L−I) measurements by means of a photodetector. These measurements have been performed by means of a Keysight B2912A source parameter with a hold time set at 200 ms for both I-V and L-I measurements in order to avoid the measurement errors related to the fast (<< 200 ms) thermal transient of the device. The integration time is about 250 µs shorter than the time constant of the thermal transient. However, the presence of self-heating does not alter the results of our investigation, since we focused on the analysis of the IV characteristic below the turn on voltage, and therefore at negligible power dissipation levels. In Figure 2 we report the variation of the electrical characteristics during stress. As can be noticed, the initial I–V exhibits a very low leakage current component, and the stress procedure was found to induce a monotonic increase both in sub turn-on forward leakage and in reverse-bias.

It is well known that in the low forward voltage region, at room temperature, conduction is mainly dominated by trap-assisted tunneling (TAT), [7,11–14]**.** This conduction mechanism strongly depends on the density of defects in the depletion region, therefore the observed increase in forward leakage indicates an increase in defect concentration induced by the stress experiment. The increase in leakage current in reverse bias instead could also be due to other mechanisms, such as variable-range hopping (VRH) conduction [15], nearest-neighbor hopping (NNH) conduction [16], space-charge-limited conduction [17], field-emission tunneling, interband tunneling and Poole–Frenkel emission [18].

In Figure 3 the L-I measurements are reported before and during stress. Only minor changes are observed, mainly consisting in an increase in the optical power emitted at low measuring currents. This can be explained by considering a current-induced activation of the doping on the p-side of the devices [19], during the initial phase of the stress. Another possibility is an increase of carrier injection efficiency towards the QW, that may be caused by an increase of trap assisted

tunneling through the quantum barrier adjacent to the over-doped spacer [20].



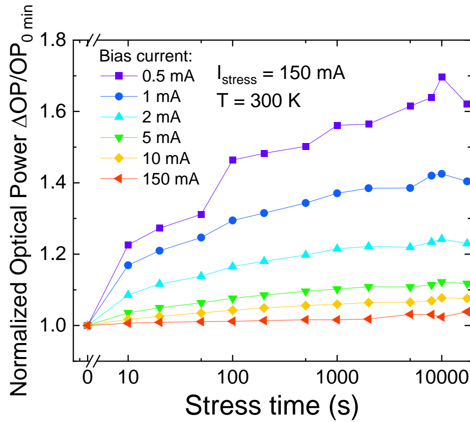


Figure 3: (a) Optical characteristics of the device during the stress. (b) At low current a slight increase in the optical power is observed (violet curve), while no substantial variations can be noticed at high current (red curve).

4. Numerical simulations of the electrical behavior of the LEDs

To validate our hypotheses, we tried to relate the stress-induced variation of the electrical behavior of the devices to the presence of deep levels within the AR. This goal was achieved by means of numerical simulations carried out through the TCAD Sentaurus suite from Synopsys Inc. [21,22]. To be more specific, the structure reported in Figure 4 has been implemented in the SDE environment as shown in Figure 1, and the layers have been doped by inserting the dopant species (Si and Mg) as traps with the characteristic energy levels described in literature [23–26]. For the simulations, the τ_{SRH}, B and C coefficients, respectively related to the SRH, radiative and Auger recombination mechanisms, have been fixed at the values commonly reported in literature [27,28]. The main material parameters for these mechanisms in binary and ternary compounds have been reported in Table 1.

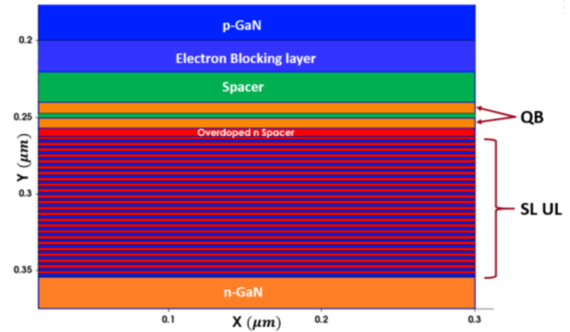


Figure 4: The device implemented in Sentaurus TCAD following the scheme indicated in Figure 1.

Finally, also thermionic emission process and direct tunneling through thin barriers were implemented in the simulation deck.

In order to improve the model, the series and shunt resistances of the real LED have been extrapolated from the I-V measurements. Such resistive components have been added to the simulated device. The purpose of the shunt resistance (fixed at $12E10\ \Omega$) is to simulate the current leakage due to parasitic paths, that impacts on the electrical characteristic at low voltages (near 0 V). On the other hand, the series resistance takes into account the non-idealities due to the contacts, buffer layers, partial activation of doping, etc.. [29] and was fixed at 15 Ω.

	GaN	AlGaN	InGaN	AlInN
x content	-	6%	12%	17%
SRH lifetime (s)	5E-8	5E-8	5E-8	5E-8
B (cm^3/s)	1E-12	1E-12	1E-12	1E-12
C (cm^6/s)	1E-31	1E-31	1E-31	1E-31
donor activation energy (meV)	20	-	-	150
acceptor activation energy (meV)	150	200	-	-

Table 1: Main parameters adopted in TCAD simulations for the LED materials.

The goal of the numerical simulations was to model the stress induced increase in forward leakage

current by considering an increase in the trap assisted tunneling. This conduction process has been implemented following the same procedure adopted in our previous paper [8] and in Mandurrino et al.[30]. In this framework, TAT is implemented as an additional SRH recombination process, whose rate is given by:

$$R_{TAT} = \frac{N_T c_n c_p (np - n_i^2)}{c_n\left(n + \frac{n_i}{g_n} e^{\frac{E_T}{k_B T}}\right) + c_p\left(p + \frac{n_i}{g_p} e^{-\frac{E_T}{k_B T}}\right)} \quad (1)$$

where N_T is the trap density, E_T is the energy level from the intrinsic Fermi level, $g_{n,p}$ are the electron and hole degeneracy factors, $c_{n,p}$ are the capture rates and T is the temperature. These latter rates depend on the combination of two capture/emission mechanisms: a phonon-assisted inelastic process and an elastic transition process [31][30][22][32]. For further details of the model, the reader should refer to [8]. The main parameters that determine these capture/emission rates are the energy level of the traps E_T, the interaction volume of the trap V_T, the Huang-Rhys factor S, the energy of the phonons involved in the transition $\hbar\omega\ (E_{phon})$ and the tunneling electron effective mass m_t. In the simulations we have set $S = 10$, $V_T = 2 \times 10^{-7}\ \mu m^3$, $E_{phon} = 91\ meV$, the electron and hole cross-section of the trap $\sigma_e = 1 \times 10^{-11}\ cm^2$ and $\sigma_h = 1 \times 10^{-11}\ cm^2$. These values were chosen in agreement with previous literature reports [7,30,33,34]. Other parameters, like the activation of piezoelectric charge and the relative tunneling mass, have been empirically adapted according to previous literature reports [8,35–37].

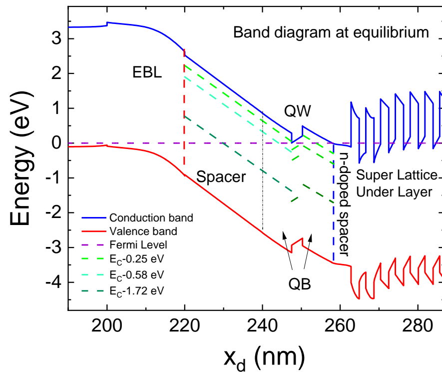


Figure 5: Simulated band diagram of the device at equilibrium. Three defect levels have been placed within the depletion region. Trap assisted tunneling is implemented both for holes and electrons in the region delimited by the blue and red dashed lines.

In Figure 5, the simulated band diagram at equilibrium of the device has been reported. The region where TAT has been implemented corresponds approximately to the width of the depletion region at equilibrium, which goes from the interface between the EBL and the undoped spacer to the interface between the quantum barrier and the overdoped spacer (respectively the blue and red dashed lines in Figure 5). The main issue we faced during the implementation of our simulation deck was represented by the choice of the deep levels and their concentration, for reproducing the TAT phenomenon. First of all, the simulations showed that only the traps placed in the undoped spacer, between the n and p side of the device, were having significant impact on the sub turn-on behavior, as shown in Figure 6, where traps have been alternatively included in the different device layers. In fact, in order to have a good tunneling probability it requires not only to have free carriers available for tunneling in proximity of empty deep levels, but also to have a proper alignment between the energy position of the carrier that is undergoing TAT and the position of the deep level.

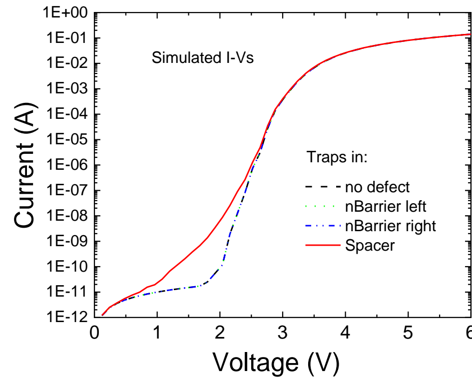


Figure 6: The simulated IV characteristics obtained by alternatively including trap states in the different device layers. the contribution to TAT for traps placed in the Quantum Barriers is null (the black, green and blue curves are overlapped). Only the defects in the Spacer contribute to TAT.

Additionally, we found that the defects that determine the TAT at low bias voltages are energetically placed close to midgap. In particular, Armstrong et al. [38], in agreement with our previous research [8] on similar

samples, identified a level optically activated at $E_C - 2.11\ eV$ with Franck-Condon energy $d_{FC} = 0.39\ eV$, thus exhibiting a thermal ionization energy of $E_C - 1.72\ eV$ (which corresponds exactly to the midgap of GaN). Similar results have also been found in [39,40]. The physical origin of these deep levels is still under debate. It has been supposed they are caused by interaction between indium atoms and intrinsic GaN surface defects, like nitrogen vacancies, formed during growth at high temperatures. Another hypothesis associates them at the presence of divacancies $(V_N - V_{III})$, as discussed in [2][41].
Other two well documented and commonly observed levels, related to intrinsic defects formed during the crystal growth, have been included into the model: a first one at $E_c - 0.25\ eV$, typically ascribed to the presence of nitrogen vacancies [42–44], and second one caused by nitrogen antisites at $E_c - 0.58\ eV$ [45][46].

Simulation of the experimental I-V characteristics

The initial defect concentration for the three deep levels have been chosen in order to reach a good initial matching with the I-V of the unaged device and has been assumed to be uniform for simplicity. The defect concentrations identified are $5E14\ cm^{-3}$ at $E_{T,1} = E_C - 0.25\ eV$ and $1E14\ cm^{-3}$ at $E_{T,2} = E_C - 0.58\ eV$. These values are comparable with previous papers [38] [46] that show similar results for GaN layers. Instead, the simulated initial defect concentration at $E_C - 1.72\ eV$ is very low $(1E11\ cm^{-3})$, since the unaged device exhibits a very-low leakage current at low voltages, and within this bias range conduction was found to be dominated by the shunt resistance component. To model the I-V curves during the stress, we made the assumption that the only parameter subjected to variation is the concentration of the $E_C - 1.72\ eV$ defect, which reaches $4.3E14\ cm^{-3}$ after 17500 min of stress. In Figure 7 a comparison between the measured and simulated I-V characteristics is reported. One can notice a very good accuracy of the electric characteristics during the constant current stress for over ten orders of magnitude.

Stress time	N_T (at $E_{T,3} = E_C - 1.72\ eV$)
0 min	1E11 cm^{-3}
50 min	6E12 cm^{-3}
500 min	3.5E13 cm^{-3}
5000 min	1.1E14 cm^{-3}
17500 min	4.3E14 cm^{-3}

Table 2: the simulated increase in defect concentration for the trap level near midgap during the stress test.

The results of the analysis highlight that: I) the trap assisted tunneling is the main mechanism that causes the sub-turn on forward leakage current; II) the increase of defect mostly concerns the deep level near midgap, that produces an increase on the leakage current at low voltages; III) the region more involved in this first process is the undoped spacer, rather than the QW, which justifies why no relevant optical degradation is observed. The trend observed in the forward current is common to InGaN/GaN LEDs [47–49], and can be ascribed to the generation or relocation of defects in proximity of the active region of the device. This observation can provide useful information for the investigation of the physical mechanisms involved in the aging of these kind of devices.

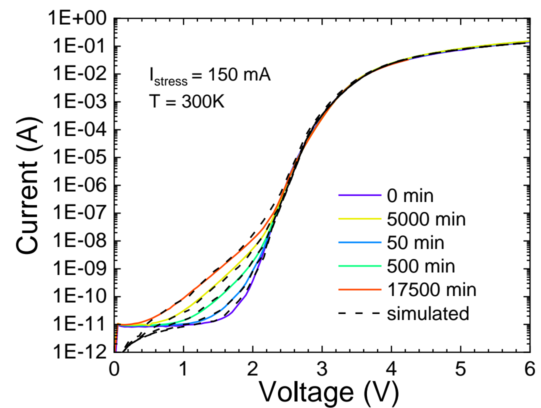


Figure 7: Comparison between the experimental electrical characteristics during the constant current stress test and the simulated curves obtained by increasing the defect concentration of the deep level located at E_c-1.72 eV.

Conclusion

In this paper we have first analyzed the electrical and optical characteristics of a SQW InGaN/GaN LED under constant current stress test. A monotonic increase of both reverse and forward leakage current has been observed. This process was ascribed to the increase in defect concentration in proximity of the active region, which is compatible with the increase in TAT-related current observed for positive voltages. The optical behavior during the stress instead presents no significant degradation, and just a minor increase in optical power emitted at low current levels.

Subsequently we proposed a model capable of emulating the electrical behavior of the devices [8,30], by assuming TAT as the main mechanism responsible for low forward-bias conduction. Through this methodology, we have been able to reproduce by simulation the increased forward leakage current, and to estimate the related increase in trap density during stress. A good correspondence was obtained between the simulated and experimental I-V curves for over 10 orders of magnitude. These results highlight the role of deep levels in the quite early aging of the device and in determining the magnitude of the (forward) TAT process, also providing a useful tool for predicting the LED behavior and ageing indicators during long-term ageing tests.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Acknowledgment

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