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(Article begins on next page)

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Design of an Analog and of a Digital-Based OTA in Flexible Integrated Circuit Technology

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***Abstract*—In this paper, an Analog and a Digital-Based Operational Transconductance Amplifier (OTA) in a 800 nm Indium-Gallium-Zinc-Oxide (IGZO) Thin-Film Transistors (TFT) Flexible Integrated Circuits (FlexICs) technology are presented and compared on the basis of post-layout simulations.**

The analog OTA (A-OTA) and the Digital-Based OTA (DB-OTA) occupy a total area of 42,624μm^2 and 25,207μm^2, respectively and - based on post-layout Monte Carlo (MC) simulations on 100 samples operated at 3.3V with 50pF capacitive load - they achieve an average gain-bandwidth product (GBW) of 58 kHz and 86 kHz, respectively, with an average power consumption of 90 μW and 113 μW. The simulated standard deviation of the input offset voltage is 22.3 mV for the A-OTA and 7.2 mV for the DB-OTA while the input-referred integrated noise over the entire GBW is 8.8 μV$_{\text{RMS}}$ and 87 μV$_{\text{RMS}}$ for the A-OTA and DB-OTA respectively.

***Index Terms*—Flexible Integrated Circuits (FlexICs), Operational Transconductance Amplifier (OTA), Digital-Based Circuit, Indium-Gallium-Zinc-Oxide (IGZO), Thin-Film Transistors (TFT).**

I. Introduction

Flexible Integrated Circuits (FlexICs) made by Thin-Film Transistors (TFT) integrated over low-cost substrates (plastic, paper or metal foil) are gaining more and more attention from the IC designer community due to their low fabrication costs, low thickness and intrinsic pliability [1–5]. These unique features, indeed, make FlexICs potentially disruptive in a wide range of applications, from disposable sensors for food [6] to smart bandages [7].

Following this trend, a flexible 32-bit ARM processor [1] (PlasitcARM), a flexible MOS 6502 microprocessor [8] (Flex6502) and an hardwired machine learning processing engine [2], have been designed in Indium-Gallium-Zinc-Oxide (IGZO) TFT technologies, and have been experimentally demonstrated in the last years.

Even though several FlexIC digital circuits and mixed-signal interfaces can be found in recent literature [1–5], [8–12], the contributions on flexible analog building blocks as Operational Transconductance Amplifiers (OTAs) are still limited in number [13–17]. Moreover, the OTAs in IGZO technology proposed so far suffer of relatively poor performance due to the intrinsic limitations of the IGZO technology and in particular to the lack of complementary devices.

Aiming to address such limitations, the adoption of digital-based analog design techniques, which have been recently proposed to address the challenges of CMOS ICs for IoT applications [18–22], is explored in this paper. For this purpose, a digital-based OTA (DB-OTA) [19–22] and an analog OTA (A-OTA) are designed in a 800nm TFT FlexIC technology and their performance is compared on the basis of post-layout simulations.

The paper is organized as follows: in Sect.II, the operation and the design of both A-OTA and DB-OTA circuits are described. In Sect.III, the performance of the flexible A-OTA and DB-OTA are compared and discussed on the basis of post-layout Monte Carlo simulations, while some concluding remarks are finally drawn in Sect.IV.

II. Flexible Analog and Digital-Based OTA Circuit Description and Design

A. A-OTA Circuit Design

The IGZO A-OTA is based on a traditional two-stage topology, including a differential pair input stage, a source follower and a source-degenerated common-source output stage, as shown in Fig.1a.

Since complementary devices are not available in IGZO technology, the differential pair and the output stage are loaded by high-resistivity resistors available in the design kit, and the source follower stage is employed as a level-shifter, to adapt the output voltage level of the differential pair to the input voltage range of the common-source output stage. Source degeneration is finally introduced in the output stage to limit nonlinear distortion.

The bias current of the differential pair is set to 10μA as a good compromise between noise, gain and power consumption. The same bias current is set for the source follower and for the output stage. The layout of the Analog OTA IGZO implementation is shown in Fig.1b.

B. DB-OTA Circuit Description and Design

The schematic of the proposed DB-OTA is shown in Fig.1c. The architecture is derived from the Digital-Based Analog Differential Circuit first presented in [19].

As in [19–22], the operation of the circuit relies on the logical outputs of the cascaded inverters with trip point V_{T}, driven by the $v'_{\text{IN}+}$ and $v'_{\text{IN}-}$ signals, obtained adding a common-mode compensation signal V_{CMP} to the external inputs $v_{\text{IN}+}$ and $v_{\text{IN}-}$ by a resistive summing network.

In details, since the digital outputs OUT$+ = 1$ and OUT$- = 0$ (OUT$+ = 0$ and OUT$- = 1$) uniquely denote that $v'_{\text{D}} = v'_{\text{IN}+} - v'_{\text{IN}-} > 0$ ($v'_{\text{D}} < 0$), when such condition is detected,

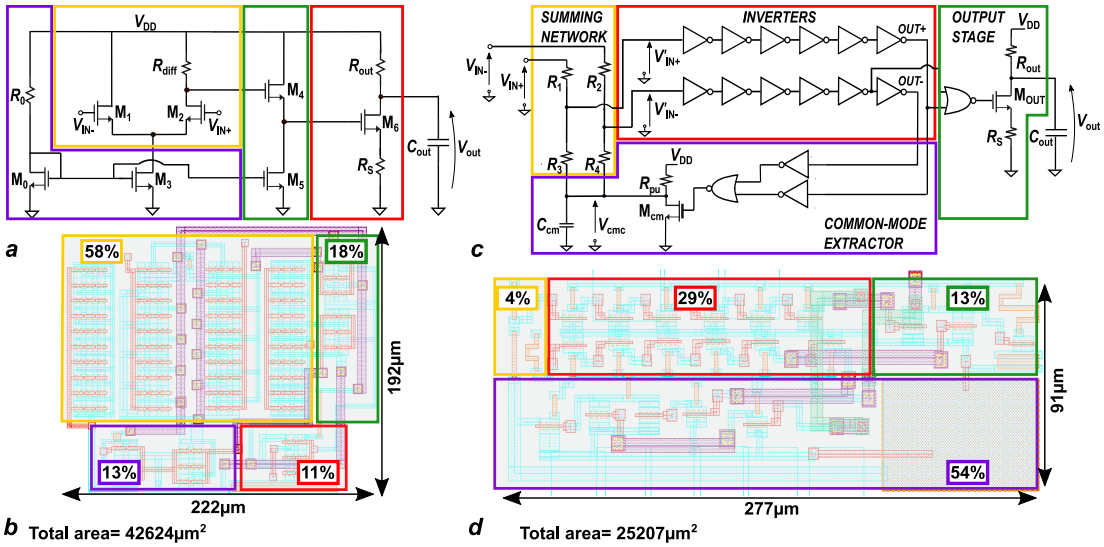


Fig. 1. A-OTA schematic(a), A-OTA layout (b), DB-OTA schematic (c), DB-OTA layout (d).

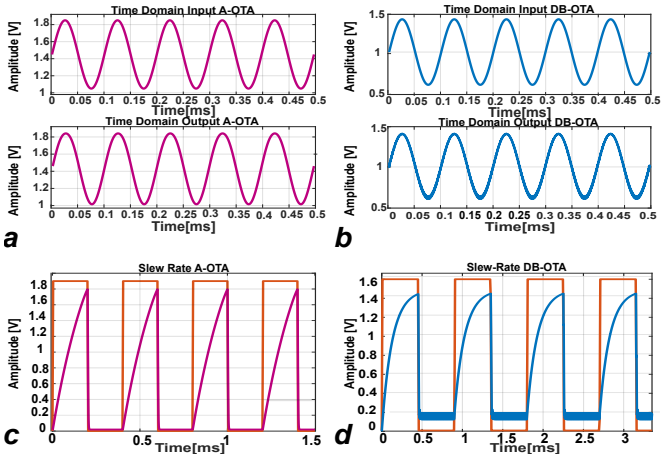


Fig. 2. Simulated input and output voltages in voltage follower configuration of A-OTA (a) and DB-OTA (b). Simulated input and output voltages under square wave input of A-OTA (c) and DB-OTA(d).

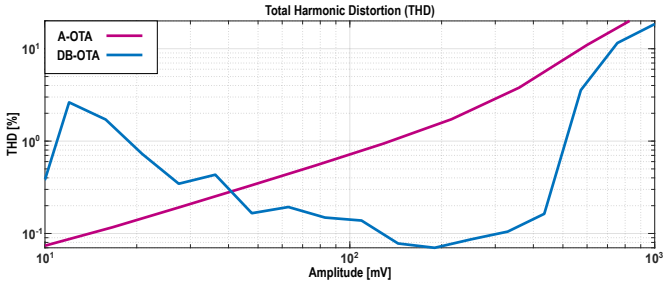


Fig. 3. THD (%) versus input amplitude.

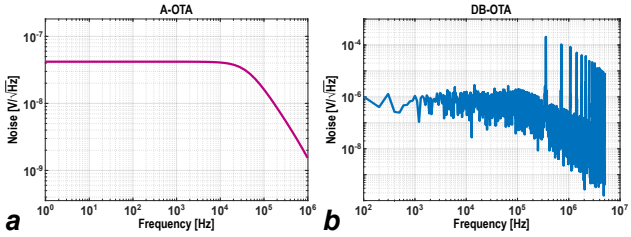


Fig. 4. Noise spectral density of A-OTA (a) and DB-OTA (b).

the output transistor M_{OUT} is operated to increase (decrease) the output voltage.

By contrast, as observed in [19], when OUT+ = 1 and OUT− = 1 (OUT+ = 0 and OUT− = 0), the sign of the CM input voltage cannot be inferred, but it can be concluded that $v'_{CM} = \frac{v'_{IN+}+v'_{IN-}}{2} > V_T$ ($v'_{CM} < V_T$). Under such condition, the CM-extractor is activated and the common mode compensation signal V_{cmc} is decreased (increased) so that to drive v'_{CM} closer to the trip point of the inverters, as demanded to detect the sign of the differential input voltage.

Thanks to the intrinsically mostly-digital architecture, the DB-OTA has been ported in 800nm IGZO technology by simply replacing CMOS logic gates with nMOS logic gates [23] consisting of minimum-length transistors.

The DB-OTA circuit has been designed following the guidelines presented in [19] targeting the same performance of the A-OTA design. The input summing network resistors R_1, R_2, R_3 and, R_4 are chosen in the MΩ range to reduce the loading effect on the source and the feedback network, and have been designed so that $R_1 = R_2 < R_3 = R_4$ to accomodate for the lower trip point of nMOS logic with respect to the CMOS logic.

The value of C_{cm} (R_{pu}) is chosen large (small) enough to keep the output impedance of the CM extractor sufficiently low, while introducing a limited area overhead.

The output stage transistor is designed along with the output resistor R_{out} to increase the gain, while source degeneration is introduced by R_S to limit the stage distortion. The layout of the DB-OTA IGZO implementation is shown in Fig.1d.

III. Simulations Results

The post-layout simulation results have been obtained using the PragmatIC [24] model libraries for 800nm IGZO TFT process [1], [2], [8] at room temperature.

A. Post-Layout Simulated Performance

The time-domain input and output waveforms of the proposed flexible A-OTA and DB-OTA in the voltage follower

TABLE I
COMPARISON WITH STATE-OF-THE-ART AMONG FLEXIBLE OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS

	[13]$^{+}$	[14]$^{+}$	[15]$^{+}$	[16]$^{+}$	A-OTA*	DB-OTA*
Technology	a-IGZO	a-Si	Dual-gate, self-aligned a-IGZO	Dual-gate, self-aligned a-IGZO	Flexible IGZO	Flexible IGZO
Min. Feature Size [um]	5	8	3	**3**	0.8	0.8
Amplifier Type	OpAmp	OpAmp	Fully Diff. OpAmp	OpAmp	OpAmp	OpAmp
#Stages/Topology	1 gain stage + 1 output stage	1 gain stage + 1 output stage	Single	2 stages internally compensated	2 stages	Single
Stage Load Type	positive-feedback	positive-feedback	Pseudo-PMOS	Pseudo-PMOS	Resistive	Resistive
DC Gain [dB]	19	42.5	40	**57**	35.2	36.3
GBW [kHz]	**330**	30	61	311	58	86
Load	15pF	20pF // 1 MΩ	30pF on PCB	-	50pF // 8 MΩ	50pF // 8 MΩ
Ph. Margin [deg.]	70	-	**98**	75	88	87
Supply Voltage [V]	6	25	10	10	**3.3**	**3.3**
Power[mW]	6.78	3.55	0.45	2.43	**0.090**	0.113
Area mm^2	25.2	5.1	0.425	3.69	0.0426	**0.0252**
PSRR [dB]	-	-	-	-	29	**39**
CMRR [dB]	-	-	-	-	**59**	45
In-band noise [μV_{RMS}]	-	-	-	-	**8.8**	87
Slew Rate [V/mS]	-	5.2	**210**	-	112	187
FOM** [MHz·pF/mW]	0.73	0.147	4.06	-	32.2	**38.05**

$^{+}$experimental; *simulation, MC mean value; **FOM = $\frac{\text{GBW}\cdot C_{\text{out}}}{\text{Power}}$; **best performance in bold**;

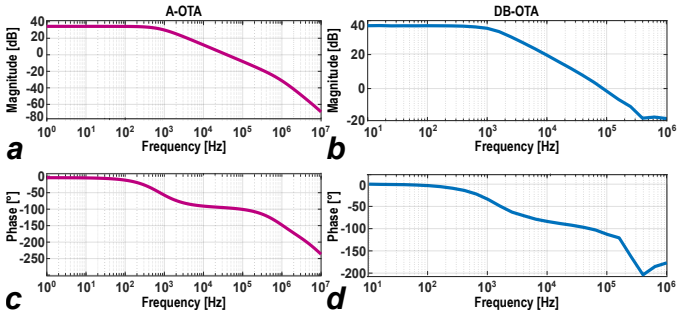


Fig. 5. Simulated A-OTA and DB-OTA frequency responses.

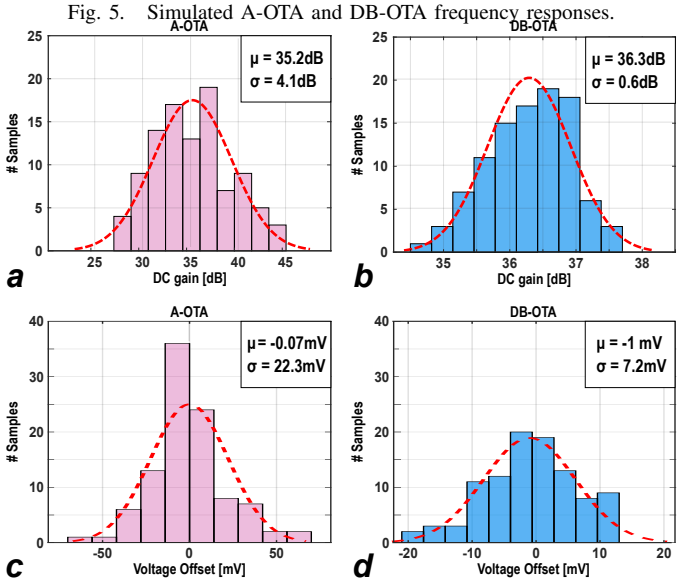


Fig. 6. Monte Carlo DC gain distributions of A-OTA (a) and DB-OTA (b). Offset voltage distributions of A-OTA (c) and DB-OTA(d).

TABLE II
MC ANALYSIS FOR THE FLEXIBLE A-OTA AND DB-OTA

Performance	A-OTA			DB-OTA		
	Mean (μ)	Std. Dev. (σ)	$\frac{\sigma}{\mu}$ [%]	μ	σ	$\frac{\sigma}{\mu}$ [%]
DC Gain [dB]	35.2	4.1	11.6	36.3	0.6	1.7
GBW [kHz]	58	31.9	55	86	15.5	18
Power [μW]	90	14.77	16.3	113	20.4	18
Voltage Offset [mV]	-0.07	22.3	-	-1	7.2	-
SR_{ave} [$\frac{V}{mS}$]	112	4.9	4.3	187	16.9	9
FOM [MHz · pF/mW]	32.2	16	49.7	38.05	11.4	30

Monte Carlo simulations on 100 samples.

configuration at $V_{\text{DD}} = 3.3$V, with a 10Hz, 400mV sine wave input (corresponding to about 80% of the amplifier input swing) and having $C_{\text{out}} = 50$pF as capacitive load are reported in Fig.2 (a) and Fig.2(b), respectively. They reveal proper operation of both OTAs with a Total Hamornic Distortion (THD) of 3.88% for A-OTA and 0.31% for DB-OTA.

It is worth noting that the DB-OTA output in Fig.2 (b) shows an out-of-band ripple component resulting from its inherently digital operation, as detailed in [22]. Fig.2 (c) and (d) are also output signal plots where square wave are applied at input using the same voltage follower configuration. Based on such simulations, the A-OTA average slew-rate is $SR_{ave_{A-OTA}} = 112$ V/ms and the DB-OTA average slew-rate is $SR_{ave_{DB-OTA}} = 187$ V/ms.

1) Total Harmonic Distortion: The simulated THD under 10 Hz sinewave input excitation is reported versus amplitude in Fig.3 for the A-OTA and DB-OTA. While the A-OTA THD is monotonically increasing with amplitude, a higher THD is observed in DB-OTA at low input amplitude due to the "dead zone" effect highlighted in [20].

2) Frequency Response: The frequency response of the A-OTA has been evaluated by AC analysis while DB-OTA by transient simulations, since AC analysis is not suitable for DB-OTA. As in [25], the DB-OTA differential amplification

frequency response ($A_{\mathrm{d}}(f) = \frac{V_{\mathrm{out}}(f)}{V_{\mathrm{d}}(f)}$) has been estimated in magnitude and phase taking the ratio of the Fast Fourier Transform (FFT) at the fundamental frequency of the output and of the differential voltage. The A-OTA and DB-OTA frequency response for the typical case reported in Fig.5(a) and (b) respectively exhibit 34.4 dB and 37.6 dB DC gain, 58 kHz and 86 kHz Gain Bandwidth Product (GBW) with phase margin equal to 88° and 87°.

3) Input noise power spectral density: The input-referred noise power spectral density, obtained by AC noise analysis for A-OTA and by transient noise analysis for the DB-OTA, are plotted in Fig.4(a) and (b), respectively. The in-band noise is $8.8\mu V_{\mathrm{RMS}}$ for the A-OTA and $87\mu V_{\mathrm{RMS}}$ for the DB-OTA.

B. Monte Carlo simulation results

Both OTAs have been verified under process variations by Monte Carlo (MC) analysis performed on 100 samples. In Fig.6(a) and (b), the mean value of the DC gain distribution is 35.2 dB for A-OTA and 36.3 dB for DB-OTA, while the standard deviation is 4.1 and 0.63 dB respectively. In Fig.6 (c) and (d), a relevant difference in the input offset voltage variability can be observed. While the A-OTA shows a 22.3 mV input offset voltage standard deviation, it is just 7.2 mV (67.7% lower) for the DB-OTA. The main performance of the two OTAs are summarized in Table II, where the figure of merit defined as in [21] is also reported.

C. Comparison with the State of the Art

Based on the post-layout MC simulation results of the two proposed flexible OTAs and measurements of the ones found in recent literature, whose performance is summarized in Tab.I, a comparison is made. The DB-OTA presented here with minimum feature size of 800 nm has the smallest area which is about one half of the A-OTA's.

The simulations suggest that the proposed A-OTA and DB-OTA achieve the lowest power consumption among Flex-IC designs (90μW and 113μW, which is 5X and 4X less than [15] respectively) with comparable GBW.

A-OTA and DB-OTA drive the highest C_{out} compared to proposed flexible amplifiers in recent literature. Based on the simulation results, the proposed DB-OTA is supposed to achieve the best FOM ($38.05\,\mathrm{MHz}\cdot\mathrm{pF/mW}$) due to its GBW of 86 kHz and rather large driving capability (50pF) at reasonably low power consumption while having one of the best reported slew rate performance.

IV. Conclusion

This paper has compared the implementation of two flexible OTAs in the 800nm IGZO TFT process: Analog and Digital-Based. The herein proposed flexible A-OTA and DB-OTA have squeezed the total area compared to the current state-of-the-art, while reducing the power by 5 and 4 times, respectively, resulting in the best reported energy efficiency FOMs. Even if the simulated results are compared with measured state-of-the-art designs, the presented flexible DB-OTA is promising, as in CMOS, and could possibly achieve better area and power while keeping reasonable performance.

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