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Design and efficiency analysis of an LCL Capacitive Power Transfer system with Load-Independent ZPA

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Keywords

≪Contactless Power Supply≫, ≪Current Source DC-DC≫, ≪DC-DC Converter≫, ≪Efficiency≫.

Abstract

This paper proposes a design procedure of an LCL compensation circuit for a capacitive power transfer (CPT) system. The design enables the achievement of load independent zero phase angle (ZPA) operation in order to increase the overall efficiency of the system by using a minimum number of compensation components. The proposed approach is supported and validated by circuital simulations and confirmed by the results of experimental tests carried out on a specifically designed prototype.

Introduction

Capacitive power transfer (CPT) is a method of delivering power without electric wires, through time-varying electric fields between two metallic plates forming a capacitance. The simple, light and cheap interface makes this technology an interesting alternative to the inductive power transfer (IPT) [1]. In addition, since electric fields can pass through metal materials without generating significant power losses, this technology is being actively studied for electric vehicle charging applications [2].

In charging applications, a constant current (CC) or constant voltage (CV) charging profile depending on the battery state of charge (SoC) is desirable to ensure its safety and durability [3]. A desirable feature in battery charger is the zero phase angle (ZPA) between the inverter output current and voltage, to reduce the volt-ampere rating and to enable soft-switching operation. This condition should be ensured for the entire charging profile, in other words, ZPA operation must be load independent [4].

According to [5], at least three passive components are required to obtain load independent ZPA operation with CC or CV output. In this article, an LCL compensation network is proposed, and a design procedure to obtain a CC output with load independent ZPA operation is given. The LCL network is able to improve the power delivered to the load and the power transfer efficiency [6]. In addition, a dc-dc efficiency analysis is performed [7], in which an analytical expression of the system efficiency as a function of the load is developed.

The proposed approach is validated both through circuital simulations and experimental tests. To this purpose, a prototype that include a half-bridge inverter and the LCL network designed to achieve ZPA

as described in this paper is tested and measurement results are compared to those obtained by the simulations showing good agreement.

Load-independent ZPA operation analysis

Fig. 1 shows the proposed topology, which is composed of a half-bridge inverter (M_1, M_2), a diode bridge rectifier (D_1 through D_4) and a resonant network. This network consists of the LCL compensator (L_1, C_2 and L_2) and the interface capacitors (C_{int1} and C_{int2}).

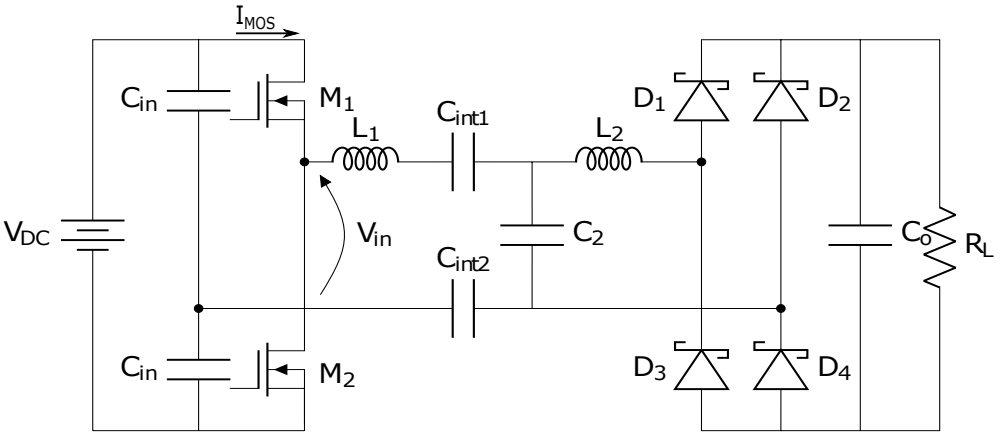


Fig. 1: CPT system with LCL compensator

This system can be simplified as shown in Fig. 2, using the fundamental harmonic approximation (FHA) [8] [9].

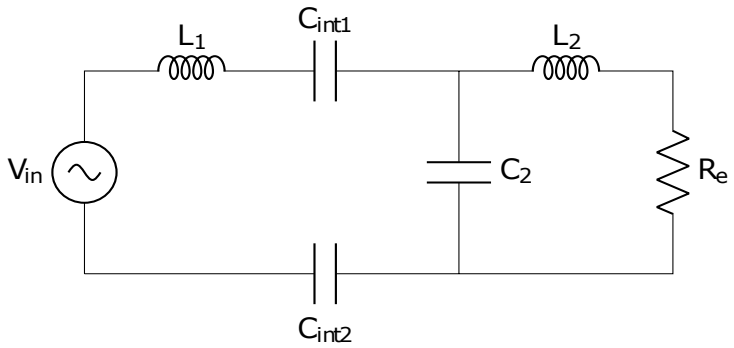


Fig. 2: Equivalent linear circuit

To this purpose, in what follows V_{in} is the fundamental component of the inverter output, which is assumed to be a pure sinusoidal with magnitude equal to:

$$V_{\text{in}} = \frac{2V_{\text{DC}}}{\pi} \tag{1}$$

and R_e is the equivalent resistance of the load with rectifier, calculated as:

$$R_e = \frac{8}{\pi^2} R_L \tag{2}$$

To obtain ZPA operation, the reactive part of the input impedance seen by V_{in}, $Z_{\text{in}} = R_{\text{in}} + jX_{\text{in}}$ must be

zero. By circuit analysis, the reactance is found to be:

$$X_{\text{in}} = \frac{R_e^2 \dfrac{\omega_0 L_1^2}{L_1 + L_2}}{R_e^2 + \left(\dfrac{\omega_0 L_2^2}{L_1 + L_2} \right)^2} - \frac{1}{\omega_0 C_1} \tag{3}$$

C_1 is the series combination of the interface capacitances:

$$C_1 = \frac{C_{\text{int1}} \cdot C_{\text{int2}}}{C_{\text{int1}} + C_{\text{int2}}} \tag{4}$$

ω_0 is the resonance frequency:

$$\omega_0 = \frac{1}{\sqrt{C_2 L_{\text{p}}}} \tag{5}$$

where $L_{\text{p}} = L_1 \parallel L_2$.

According to (3), C_1 can be designed to achieve zero input reactance. Simply solving this equation for C_1 and selecting interface capacitors to obtain the required capacitance would not lead to a robust design, since the input reactance is load dependent, and consequently ZPA operation as well.

However, based on (3), load independent ZPA operation must be gauranteed when the following inequality is satisfied:

$$R_e^2 \gg \left(\frac{\omega_0 L_2^2}{L_1 + L_2} \right)^2 \tag{6}$$

If this is true, then the much smaller term is neglected with respect to R_e^2 in the denominator of (3), making the input reactance approximately load independent,

$$X_{\text{in}} \approx \frac{\omega_0 L_1^2}{L_1 + L_2} - \frac{1}{\omega_0 C_1} \tag{7}$$

$$C_1 = \frac{L_1 + L_2}{(\omega_0 L_1)^2} \tag{8}$$

Under such condition, for (8), X_{in} is effectively cancelled for any load and consequently load independent ZPA operation can be obtained for a particular frequency.

Design procedure

A design procedure for the CPT converter of Fig. 1 with load independent ZPA operation is proposed in this section. The specifications of the proposed system are given in Table I. The design of the system consists of calculating the components of the compensation network, to obtain the load independent ZPA operation previously explained and to fulfill the output requirements. By circuit analysis, the circuit is proven to work as a current source. Therefore, it makes sense to express the output requirements in terms of current rather than power, using $P_o = I_o^2 R_L$.

Simplified equations to calculate the component values can be obtained by considering the assumption $L_1 \gg L_2$. The design begins with the calculation of the inductance L_2, to obtain the required output current according to the following equation:

$$L_2 = \frac{4}{\pi^2} \frac{V_{\text{DC}}}{\omega_0 I_o} \tag{9}$$

The (6) is assumed to be:

$$R_e^2 = 10 \times \left(\frac{\omega_0 L_2^2}{L_1 + L_2} \right)^2 \tag{10}$$

Using (2), the (10) is solved for the inductance L_1 to guarantee ZPA condition for loads as low as $R_{\mathrm{L,min}}$:

$$L_1 = \frac{\pi^2 \sqrt{10}}{8} \frac{\omega_0 L_2^2}{R_{\mathrm{L,min}}} \tag{11}$$

Once both inductances are calculated, the equivalent capacitance of the capacitive interface is designed to compensate the input reactance, as shown in (8). Finally, C_2 is calculated to make the system resonant at the working frequency, expressed in (5):

$$C_2 = \frac{1}{\omega_0^2 L_{\mathrm{p}}} \tag{12}$$

Based on the specifications of Table I, the passive components computed using conventional design for $R_{\mathrm{e}} = 12\,\Omega$ are shown in Table II. Applying the above procedure to get load independant ZPA operation to the same specifications of Table I, the optimal normalized passive components along with parasitics [10] are shown in Table III. The value of interface capacitors are not kept equal in order to have equivalent capacitance more closer to the computed value which is 55.04 pF.

Table I: System specifications

Parameter	Value
V_{DC}	60 V
f	1 MHz
P_o	4 W
R_L	15 Ω
$R_{\mathrm{L,min}}$	3 Ω

Table II: Conventional passive components

Component	Value
L_1	50 µH
L_2	7.74 µH
$C_{\mathrm{int1-2}}$	1436 pF
C_2	3.76 nF

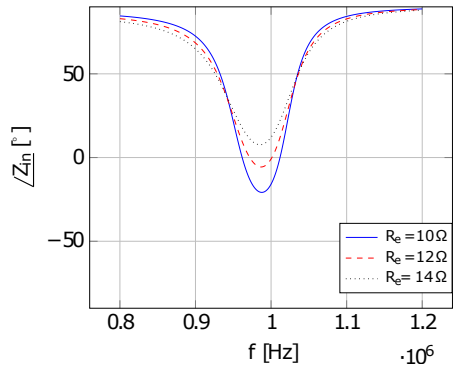
Table III: Optimal normalized passive components

Component	Value
L_1	470 µH
DCR_{L_1}	3 Ω
L_2	10 µH
DCR_{L_2}	0.08 Ω
C_{int1}	100 pF
C_{int2}	120 pF
$\mathrm{ESR}_{C_{\mathrm{int}}}$	0.05 Ω
C_2	2.7 nF
ESR_{C_2}	0.025 Ω
$\mathrm{R}_{ds,on}$	0.03 Ω

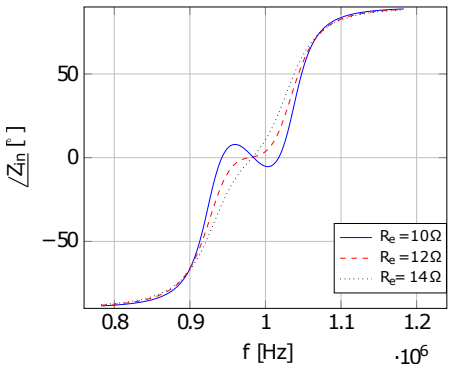
Simulation results

The circuit shown in Fig. 1 has been simulated in MATLAB/Simulink for the components value specified in Table II and Table III and the corresponding results are reported in Fig. 3. This is observed in Fig. 3a where the phases of the input impedance Z_{in} for three different loads R_{e}, i.e., 10 Ω, 12 Ω and 14 Ω are shown. The zero phase angle condition is achieved at different frequencies for each load. If the system works at a frequency of 1 MHz, only the curve for R_e =12 Ω achieves ZPA condition, meaning that only for this load soft switching is obtained, which is verified in Fig. 3c where the transistor currents are shown for the same three loads.

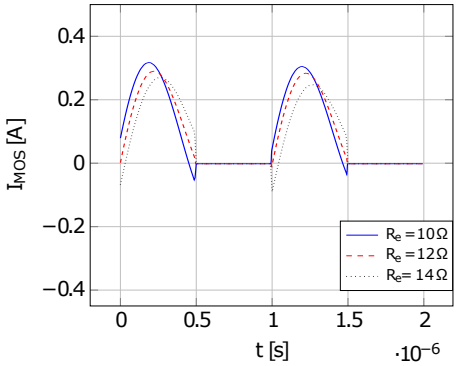
However, in Fig. 3b, there are zero phase input reactances at a frequency of 978 kHz for all three loads. The resonant frequency is obtained at 978 kHz instead of 1 MHz since the normalized component values are little different from the computed values. The load independent soft switching operation is achieved at this working frequency, as seen in Fig. 3d where the transistor currents for the same three loads are shown.



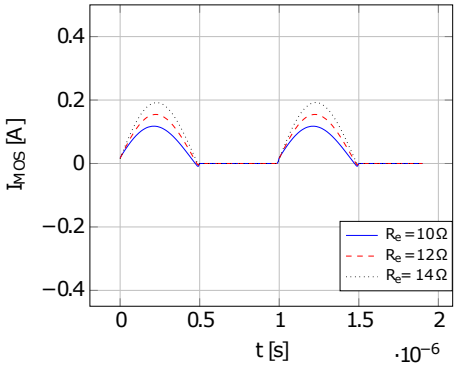
(a) Load dependent phase angle



(b) Load independent phase angle



(c) Load dependent transistor current



(d) Load independent transistor current

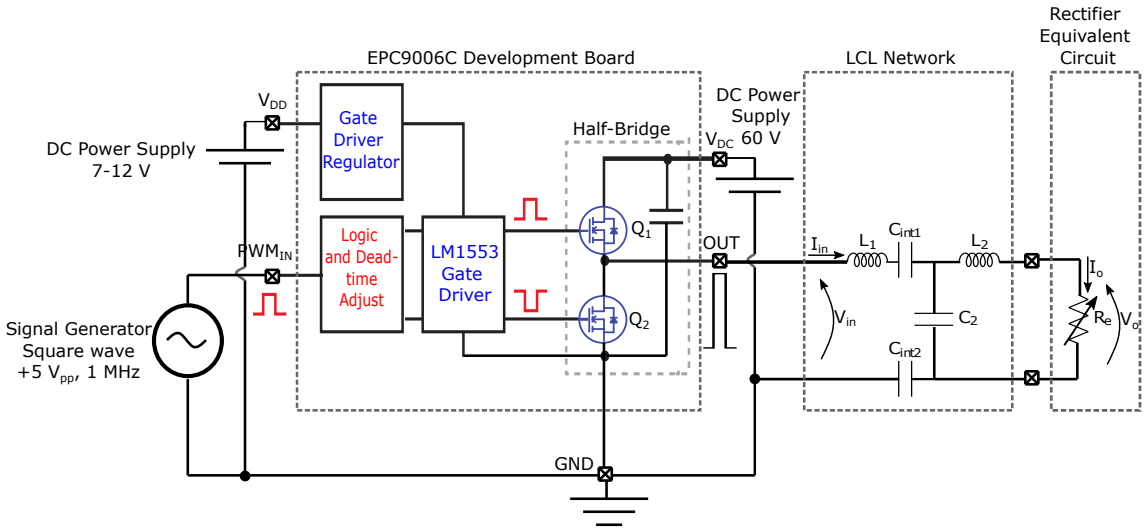
Fig. 3: Simulation results for load dependent and independent input reactance phase angle (a), (b), and load dependent and independent transistor current (c), (d)

Experimental setup and results

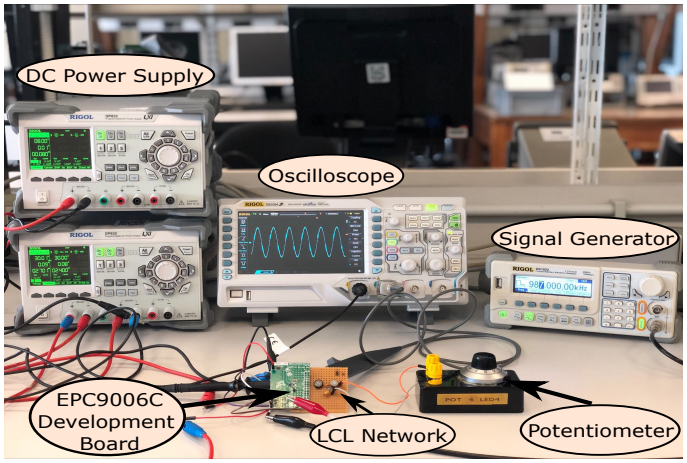
In order to validate the proposed design procedure, a prototype has been implemented and its performances have been experimentally characterized and compared to simulations. The schematic of the test setup is shown in Fig. 4a. It includes an EPC9006C development board [11] implementing the half-bridge with EPC2007C GaN enhancement mode field effect transistors (FET) (Q_1, Q_2). The input to the half-bridge is V_{DC} which can take a maximum value of 100 V. The board also contains the FET driver circuit, i.e., LM1553 gate-driver which is driven by V_{DD} = 7 V to 12 V and pulse-width modulation (PWM) circuit whose input is PWM_{IN} which can be maximum +6 V_{PP}, 6 MHz square-wave signal [11]. The LCL network components designed to obtain ZPA operation as explained in previous section, are mounted on a breadboard and connected to the EPC9006C development board as shown in Fig. 4a (V_{in} port). At the output, the equivalent resistance R_e described in the previous section (see eq.(2)) is considered instead of diode bridge rectifier.

The picture of the test setup is shown in Fig. 4b. The EPC9006C development board is mounted on the breadboard alongwith LCL network components specified in Table III. The potentiometer whose range is 0 to 50 Ω is placed and connected to the output through wires. The V_{DD} = 8 V to the driver circuit and V_{DC} = 60 V to the half-bridge inverter is provided by DC power supply [12]. The +5 V_{PP}, 1 MHz square-wave signal is given to PWM_{IN} by signal generator [13]. The input voltage and current (V_{in}, I_{in}) and respective output voltage and current (V_o, I_o) waveforms are taken on the oscilloscope [14] for various loads at different frequencies.

Since the real component values are slightly different from the nominal values, so the resonant frequency is obtained at 987 kHz instead of 978 kHz. At this frequency, the load is varied from 1 Ω to 30 Ω. It can be noted that the zero-phase angle operation is maintaned for all the loads above $R_{L_{min}}$. For three different loads, i.e., 10 Ω, 12 Ω and 14 Ω, the input phase is measured at all the frequencies ranging from



(a)



(b)

Fig. 4: Experimental test setup of the LCL CPT system with load-independent ZPA operation (a) Test setup schematic (b) test setup picture.

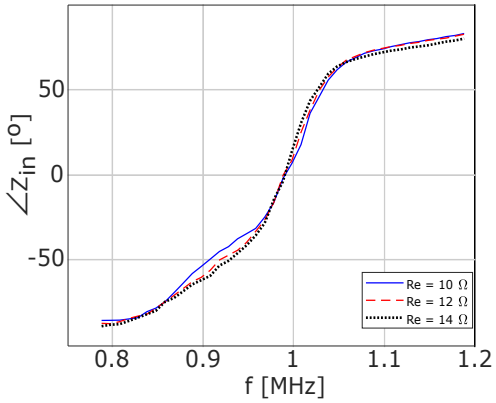
0.8 MHz to 1.2 MHz. The input phase versus frequency plot is generated and is reported in Fig. 5a. It is shown that, all three loads have almost zero-phase at working frequency. The phase difference increases for higher frequencies and symmetricaly decreases for lower frequencies.

Since, the transistor current (I_{MOS}) flows inside the EPC9006C board, so it can not be directly measured. However, we can measure the input current (I_{in}). The I_{MOS} is exactly the same as the I_{in} for the case when $V_{in} = 60$ V and zero when $V_{in} = 0$. Post processing of the current waveform I_{in} is perfomed in order to plot the I_{MOS} current and compare it to that shown in Fig. 3d. The resulting transistor currents are shown in Fig. 5b which verifies the ZPA operation for the same three loads (10 Ω, 12 Ω and 14 Ω).

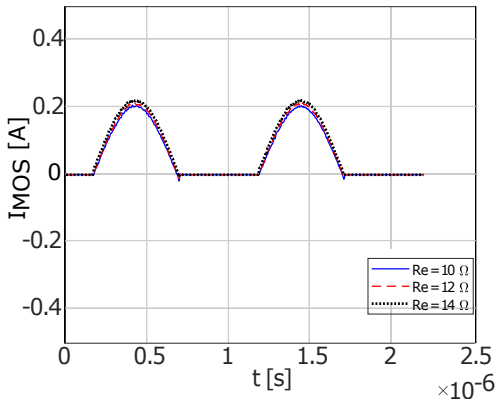
Efficiency analysis

In this section, the efficiency of the CPT system is studied. The efficiency depends on the losses of the devices, which are generated by parasitics specified in their datasheets, and are sometimes difficult to estimate. Therefore, to obtain a simple model, the following simplifications are considered:

- The losses generated by the passive components are represented by a series resistor (DCR for the inductors, ESR for the capacitors)
- The losses generated by the MOSFETs are modelled with a series resistor ($R_{ds,on}$) and by a constant contribution due to the gate capacitance



(a) Load independent phase angle



(b) Load independent transistor current

Fig. 5: Experimental results for load independent input reactance phase angle (a) and load independent transistor current (b)

- The losses generated by the Schottky diodes are caused by the forward voltage drop, V_{F}

In this way, the losses on all the devices are modelled using parameters specified in their datasheets. The goal is to obtain an analytical expression to represent the system efficiency as a function of a certain output quantity, such as the load. To this purpose, the efficiency is expressed as:

$$\eta = \frac{P_{\mathrm{o}}}{P_{\mathrm{o}} + \sum_i P_{\mathrm{Loss,i}}} \tag{13}$$

If the output power is expressed as $P_{\mathrm{o}} = I_{\mathrm{o}}^2 R_{\mathrm{L}}$, and the losses on the many devices are calculated with the simplifications considered, the efficiency can be expressed as follows:

$$\eta = \frac{R_{\mathrm{L}}}{\alpha + R_{\mathrm{L}} + \beta R_{\mathrm{L}}^2} \tag{14}$$

where α and β are parameters that depend on component values and their parasitics, and are calculated by circuit analysis as shown below.

$$\alpha = \frac{\pi^2}{8}\left(\mathrm{DCR}_{\mathrm{L_2}} + \mathrm{ESR}_{\mathrm{C_2}} + 4V_{\mathrm{F}}\frac{\omega_0 L_{\mathrm{P}}}{V_{\mathrm{DC}}} + V_{\mathrm{gs}} Q_{\mathrm{g}} f\left(\frac{\pi\omega_0 L_{\mathrm{p}}}{V_{\mathrm{DC}}}\right)^2\right) \tag{15}$$

$$\beta = \frac{8}{(\pi\omega_0 L_{\mathrm{p}})^2}\left(\mathrm{DCR}_{\mathrm{L_1}} + 2\mathrm{ESR}_{\mathrm{C_{int}}} + R_{\mathrm{ds,on}}\right) \tag{16}$$

With this model, the efficiency is represented as a function of the load, and efficiency versus load curves are developed. Selecting real components for Table III, the curves of Fig. 6 are generated both through computations and measurements. It is seen that the both curves are in close agreement to each other achieving a maximum of around 92% through computations (continuous line in Fig. 6) and 83% through measurements (dashed line). However, for the higher loads, there is a difference in the curves which is due to the fact that the proposed efficiency model doesn't take in to account the AC losses of the inductor which are high for higher loads, since the input current is high.

Conclusion

A design procedure for a CPT system using the LCL topology is explained in this article. This topology is able to provide a CC output with load independent ZPA operation, using just three passive components. In addition, the dc-dc efficiency is studied, and the system is expected to provide an efficiency of around 83% at nominal load. Effectiveness of the proposed procedure has been validated experimentally.

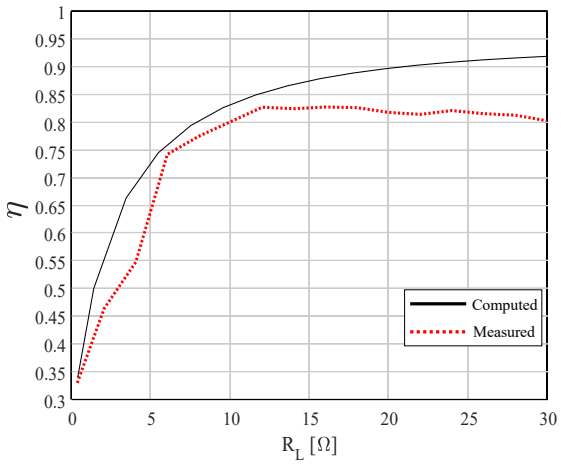


Fig. 6: Efficiency versus load

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