A Zero-Transient Dual-Frequency Control for Class-E Resonant DC-DC Converters

A Zero-Transient Dual-Frequency Control for Class-E Resonant DC–DC Converters

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***Abstract*—In this article, a dual-frequency control method for regulating the output power in class-E resonant dc–dc converters has been introduced. As in the standard ON–OFF control or other recently proposed dual-frequency controls, the approach is based on the ability of the converter to alternately operate in a high- and a low-power state. The proposed solution has a twofold advantage: on the one hand, soft-switching capabilities (i.e., zero-voltage and zero-voltage-derivative switching) are preserved in both operating states; on the other hand, it is possible to reduce to zero the transient time required to switch from one state to the other one. The most straightforward consequence is the possibility to increase to very large values the frequency at which the two operating states are switched, up to the same order of magnitude as the main switching frequency of the converter. In this way, the additional ripple introduced by the proposed dual-frequency control can be decreased to a negligible value. The approach has been validated by measurements on a prototype operating between 4 and 8 MHz and in which it has been possible to increase the control frequency up to 500 kHz.**

***Index Terms*—Class-E converters, dual-frequency control, ON–OFF control, resonant converters.**

I. Introduction

RESONANT dc–dc converters have been introduced to allow operations at high switching frequencies with many advantages in terms of power density [1], [2], [3], EMI [3], [4], [5], and dynamic performances [6], [7]. They usually take advantage of techniques commonly used in radio-frequency power amplifiers [8], [9], [10], [11] to reduce switching losses and overcome the drawback of hard-switching converters [12], [13], where losses increase with the operating frequency. As such, resonant converters are capable of operating in the frequency range from a few megahertz to hundreds of megahertz.

In this article, we focus on *class-E* resonant converters that feature the well-known soft-switching technique, in opposition to the hard-switching one that characterizes the *class-D* family [9], [14], [15], [16]. More specifically, we refer to zero-voltage switching (ZVS) if the reactive components, used in the converter, reshape the voltage across a switch—either a controlled (e.g., a power MOS) or noncontrolled one (e.g., a rectifying diode)—in a way that it slowly goes to zero before turn-ON, and gradually moves from zero after turn-OFF. Additionally, we refer to zero-voltage-derivative switching (ZVDS) if the zero voltage level is approached with zero time derivative, too. If both ZVS and ZVDS are satisfied, the class-E converter is said to operate under *optimum* condition. If only ZVS is satisfied, the class-E converter is said to operate under *suboptimum* condition.

The critical aspect of all resonant topologies, including the class-E one, is that the optimum or suboptimum behavior can be ensured for a given operating point only (e.g., the one that guarantees the nominal output power). As a consequence, in order to cope with different output power levels, several control methodologies have been presented so far in [17], [18], [19], [20], [21], [22], [23], [24], [25], and [26].

In this article, we aim to significantly progress in this direction by introducing an optimized dual-frequency control method. The core idea is to allow the converter to alternatively operate between a high-power and a low-power state so that the average output power can be regulated by changing the relative duration of the two states. The following two important advantages characterize this approach when compared to existing methods:

1) The optimal ZVS-ZVDS conditions are *preserved* in both operating states, thus maximizing converter efficiency;
2) The transient response, i.e., the time required for switching between the two states, can be reduced to zero, allowing to increase the control frequency to a value of almost the same order of magnitude as the main switching frequency.

This is fundamental to reduce the additional output ripple introduced by the control strategy to a negligible level. Our approach relies its theoretical background on the exact class-E design approach proposed in [15].

This manuscript is organized as follows. In Section II, we present an overview of the state of the art of class-E control methodologies. In Section III, we show the basic principle

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and the optimization of the proposed technique. In Section IV, measurements results from a suitably implemented prototype are presented. Finally, Section V concludes this article.

II. State of the Art in Class-E Output Power Regulation

Control methodologies that ensure the correct output power even when the load is variable or when the input voltage is not precisely known are desirable but they typically violate ZVS and/or ZVDS. The most common control techniques adopted in the regulation of resonant dc–dc converters are: pulse frequency modulation (PFM), pulsewidth modulation (PWM), and ON–OFF control.

PFM output power regulation basically relies on the variation of the converter switching frequency according to the desired output power. The side effect is the loss of soft-switching properties, achievable at the resonant frequency only. As an example, in [14], a class-E converter in which the optimum behavior is achieved at the maximum output power only is designed. At a lighter load, the converter is regulated by increasing the switching frequency, but the system is not able to maintain the optimum class-E condition anymore. Most recently, in [19], an asymmetric pulse frequency modulation is proposed, characterized by constant on time for series resonant converter in high-voltage and high-power applications.

In PWM control, the converter operates at constant switching frequency while the pulsewidth of the waveform, which controls the turn-ON and turn-OFF of the power switch, is suitably modified. The main issue is that soft switching can be maintained at the nominal duty cycle only since, by varying the pulsewidth, the instant at which the power switch turns ON may not be equivalent to the instant at which the voltage across it vanishes. In [20], a PWM controller is used together with a lookup table for a dc–dc class-E buck–boost converter in which the pulsewidth changes according to the load. In [21], an FPGA-based dynamic duty cycle controller is built to modulate the duty cycle and the frequency of the gate driving signal so that ZVS and ZVDS are always achieved for a different level of input voltage while the output voltage is regulated via ON–OFF control.

The ON–OFF control has proven to be one of the most popular techniques in the megahertz-range applications [22], [24], [25], [26]. Its basic principle is a low-frequency *dimming* of the output power: the converter is turned ON and OFF at the frequency f_d. When the converter is ON, it is working at the nominal average power $P_{\rm nom}$, whereas when OFF, the power decreases to zero. Indicating with D the dimming ratio (i.e., the fraction of the period in which the converter is on, with $0 \leq D \leq 1$), and assuming an output low-pass filter that delivers to the load the *average* power generated by the converter only, we get

$$P_{\rm out} = P_{\rm nom} \cdot D. \tag{1}$$

A detailed analysis of a 20-MHz class-E dc–dc converter with ON–OFF control over a wide input voltage range is provided in [23]. Similarly, the design and control of a 10-MHz class-E dc–dc converter employing the ON–OFF control technique are reported in [26], where the possibility to reduce the voltage stress across the main switch at lighter load is analyzed.

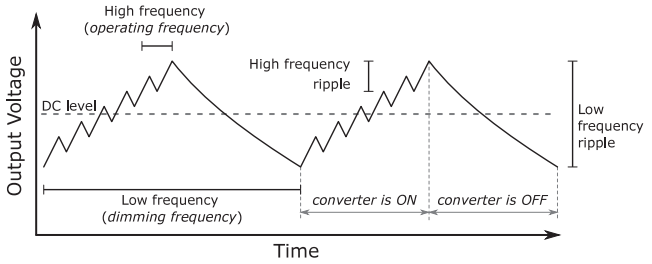

Fig. 1. High-frequency and low-frequency components in the output voltage ripple of an ON–OFF controlled converter.

However, one of the major problems of the ON–OFF control is the very long transient time characterizing the start-up/shut-down of each ON–OFF cycle [22], which sets an upper bound on the dimming frequency f_d.

The consequence is an increase in the output voltage ripple, as sketched in Fig. 1. When the converter is OFF, the load is powered by drawing energy from the output filter. By reducing the energy accumulated in the filter, the output voltage reduces, and an additional (low frequency) ripple superimposed to the standard (high-frequency) ripple of the converter is observed. Typically, the low-frequency ripple is the dominant one.

A simple analysis, assuming the output voltage almost constant, the high-frequency ripple negligible with respect to the low-frequency one, and a capacitance $C_{\rm out}$ as output filter, easily leads to estimate the output ripple as

$$\Delta V = \frac{P_{\rm nom}}{V_{\rm out}} \frac{1}{f_d\, C_{\rm out}} D(1-D). \tag{2}$$

A direct consequence of the aforementioned result is that f_d must be set to the largest possible value to either reduce ΔV given $C_{\rm out}$, or reduce $C_{\rm out}$ given ΔV.

Furthermore, the existence of long turn-ON and turn-OFF transients in which there is no sufficient time for the converter to reach its steady-state condition, and thus, ZVS-ZVDS cannot be ensured, leads to significant energy losses at each ON–OFF cycle. This affects the overall power converter efficiency, especially at higher f_d values. In other words, contrarily to (2), which suggests that a sufficiently high dimming frequency should be used to reduce ΔV, the efficiency constraint sets a competing constraint in terms of an upper bound for it.

Note that ensuring a sufficiently large f_d will also have beneficial effects in terms of electromagnetic interference (EMI) reduction. Even if an exact and rigorous analysis is out of the scope of this article, we can say that, in converters of this class, the most important contribution to EMI is the conducted emission generated by the converter input current propagating through the power-supply wires. The expected spectrum includes components at f_d and its harmonics, at the main switching frequency and its harmonics, and at all the intermodulation frequencies. It yields that by increasing f_d, the low-frequency components are moved higher in the interference spectrum, making it easier for an input EMI filter to attenuate them.

The frequency issue can be further highlighted by considering some of the results recently presented in the literature when a resonant converter enjoys ON–OFF control. As two noteworthy examples, in [23], measurements on a prototype working at the operating frequency of $20\,\mathrm{MHz}$ show a dimming frequency, which is about $1000\times$ smaller, i.e., $f_d = 30\,\mathrm{kHz}$ with $D = 50\%$. In [26], the authors use a variable f_d. In the provided example, with $D = 17\%$, one can estimate from measurements a value of $f_d \approx 150\,\mathrm{kHz}$, which is almost $100\times$ smaller than the operating frequency.

In settings similar to the ones above, the low-frequency ripple dominates. This is the reason why many works can be found in the literature trying to solve the transient time issue. Some solutions use a second-order harmonic filter [27] or reduce the input inductance value [28]. However, due to the difficulties in achieving ZVS during both start-up and shut-down transient response, extra snubbing elements, as the ones generally adopted to mitigate the effects of the hard switching, are used to ensure soft switching at every cycle. As an example along this line, in [22], an additional zero voltage transient (ZVT) cell is proposed to be added to the converter to speed up the turn-OFF time. This article shows measurement results from a 3-MHz quasi-resonant boost converter with the additional ZVT cell, which uses an ON–OFF control at $f_d = 300\,\mathrm{kHz}$. Furthermore, in [24], an extra control is added to the latter boost converter to manage the first switching period of each power pulse, in order to reduce the transient power losses of the ON–OFF control.

More recent works replace the ON–OFF control with a *dual-frequency control*, in which the converter is not switched between an ON- and an OFF-state, but between a higher power $P_{\mathrm{nom}}^{(1)}$- and a lower power $P_{\mathrm{nom}}^{(2)}$-state, typically by modifying the main clock signal. Indicating, as in the standard ON–OFF case, with f_d the dimming frequency and with D the dimming ratio, defined as the ratio of time in which the converter operates at $P_{\mathrm{nom}}^{(1)}$, (1) is replaced by

$$P_{\mathrm{out}} = P_{\mathrm{nom}}^{(1)} \cdot D + P_{\mathrm{nom}}^{(2)} \cdot (1 - D) \tag{3}$$

and a condition similar to (2) holds for the ripple. The advantage of this solution is that, since the converter is never turned OFF, transient times are substantially reduced. Yet, the additional problem of ensuring optimal or suboptimal condition is still present and must be addressed to prevent unacceptable drops in the efficiency.

As an example, the authors of [25] implement a class-E dc–dc converter designed to operate at multiple switching frequencies (more precisely, at the two frequencies $f_s^{(1)} = 20.5\,\mathrm{MHz}$ and $f_s^{(2)} = 22.5\,\mathrm{MHz}$) in order to deal with multiple input power levels. In the provided example, the dimming frequency is set to $f_d = 17.9\,\mathrm{kHz}$ with $D \simeq 0.7$ (estimated from the figure in the article). Therefore, f_d results to be about $1200\times$ smaller than $f_s^{(2)}$. The main issue is that the converter topology remains unchanged when switching from $f_s^{(1)}$ to $f_s^{(2)}$, which results in the converter being able to operate only at suboptimal condition and just in the neighborhood of the designed working frequency of $f_s = 20\,\mathrm{MHz}$.

From the aforementioned considerations and examples, one can readily conclude that the issues that arise from the ON–OFF control, are only partially solved in the classic dual-frequency designs. The main reason for this is that the achieved transient time, which has indeed been considerably reduced, has still an appreciable negative effect on the converter efficiency drop so further improvements are needed in this respect. Additionally, the proposed state-of-the-art dual-frequency techniques either introduce extra control elements, as in [23], or they are not able to ensure soft-switching during frequency transition, as in [25].

In this article a dual-frequency control method, simply based on the modification of the value of two capacitances, is applied to a resonant class-E converter. The method is *capable of mitigating both problems* of the standard dual-frequency approach. More precisely, we will show the following for the proposed solution:

1) the circuit operates under *optimum soft-switching condition* in both high- and low-power states;
2) it is possible to optimize the converter and *achieve a zero-transient (ZT) time* when switching from one state to the other.

Despite the apparent similarity, the proposed control technique must not be confused with works such as [29], [30], and [31], in which the circuit is dynamically tuned to achieve impedance matching in order to compensate for environmental effects or component tolerances that may alter the desired operating point (and in particular, the resonant frequency). As a matter of fact, the key idea of this work is to intentionally (and dynamically) change the converter operating point to allow a dimming between two frequencies in order to modulate the output power and overcome the ON–OFF control issues.

III. Theoretical Analysis

The basic schematic of the converter topology considered in this article is shown in Fig. 2(a). This topology is known as the *boost* class-E converter [3], [14], [15], [32], [33], [34], [35], since it ensures $V_{\mathrm{out}} > V_{\mathrm{in}}$, and includes five resonant elements, i.e., according to the naming system of the figure, the inductances L_{inv}, L_{rec}, and M, and the capacitances C_{inv} and C_{rec}. Capacitance C_{out}, instead, is simply used as output filter capacitance. For the sake of simplicity, a resistive load R_L is considered.

A. Single-Frequency Class-E Converter Design

The converter design relies on the results reported in [15]. Instead of considering the standard sinusoidal approach, this work bases the design of the converter on the exact and semianalytical design methodology first proposed in [36], introducing a few improvements and analyzing many tradeoffs. The analysis is limited to the scheme of Fig. 2(b), which is, however, shown to be equivalent to many class-E converter topologies, including the one in Fig. 2(a). In the proposed analysis, the five resonant elements are replaced by expressions of the corresponding five dimensionless parameters k_I, k_R, q_M, q_I, and q_R. The procedure is, however, very complex, and even if based on exact and analytic equations, requires many numerically computed constants. For this reason, it is not possible to report here

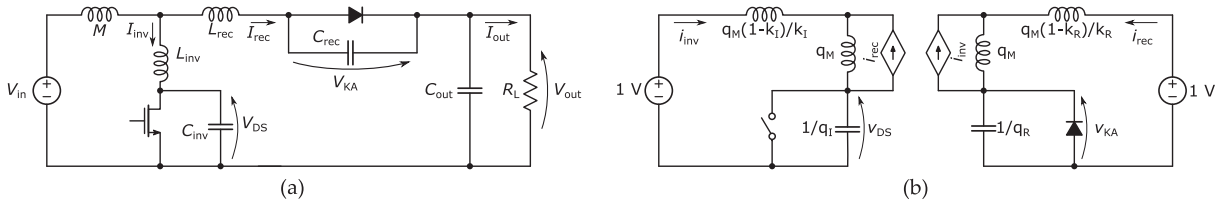

Fig. 2. (a) Basic schematic of the standard class-E boost converter considered in this article. (b) Schematic of the normalized $1\,\mathrm{V}-1\,\mathrm{V}$, $1\,\mathrm{W}$ $1\,\mathrm{rad/s}$ equivalent class-E converter considered in [15] for the design of the converter in Fig. 2(a).

simple equations capable of computing the optimal values of the parameters. Indeed, Celentano et al. [15] provide tools for the easy computation of them.

The main advantages of the approach proposed in [15] and [36], with respect to the many others proposed so far, can be summarized as follows.

1) The main sources of losses for all active and passive devices can be taken into account.
2) A normalized converter, i.e., a 1 W, 1 V-to-1 V converter, whose main switch is operating at $1\,\mathrm{rad/s}$ with any desired duty cycle. The converter parameters are then denormalized to fit the desired input/output voltage combination, operating frequency, and output power.
3) In the most general case, two among the five dimensionless parameters are degrees of freedom. In all examples provided in [15], k_I and k_R are selected by the designer, whereas q_M, q_I, and q_R are computed accordingly to ensure the optimal class-E condition.

The aforementioned point 1) is of paramount importance to ensure adherence between the design model and the real converter behavior. As such, we will always implicitly consider lossy models in our converter design; yet, to keep the discussion as simple as possible, we will not consider lossy terms in the rest of this section. The interested reader is referred to [15] for a more detailed discussion.

Roughly speaking, once the duty cycle has been selected, the normalized procedure in [15] is used to get a set of dimensionless parameters k_I, k_R, q_M, q_I, and q_R ensuring the optimal class-E condition. Then, given the desired values of input and output voltages V_{in} and V_{out}, of the output current I_{out} and of the operating frequency f_s, the values of the inductors L_p, L_s, M and the capacitors C_{inv}, C_{rec} can be computed as

$$\begin{aligned} C_{\mathrm{inv}} &= \frac{V_{\mathrm{out}} I_{\mathrm{out}}}{V_{\mathrm{in}}^2}\frac{1}{2\pi f_s q_I},\ C_{\mathrm{rec}} = \frac{I_{\mathrm{out}}}{V_{\mathrm{out}}-V_{\mathrm{in}}}\frac{1}{2\pi f_s q_R} \\ M &= -\frac{q_M V_{\mathrm{in}}}{2\pi f_s I_{\mathrm{out}}},\ L_{\mathrm{inv}} = -M\left(\frac{V_{\mathrm{in}}}{V_{\mathrm{out}}-V_{\mathrm{in}}}\frac{1}{k_I}+1\right) \\ L_{\mathrm{rec}} &= -M\left(\frac{V_{\mathrm{out}}-V_{\mathrm{in}}}{V_{\mathrm{in}}}\frac{1}{k_R}+1\right). \end{aligned} \tag{4}$$

Note that, according to (4), values of k_I, k_R, and q_M are expected to be negative in order to deal with a feasible converter (i.e., whose components have positive values).

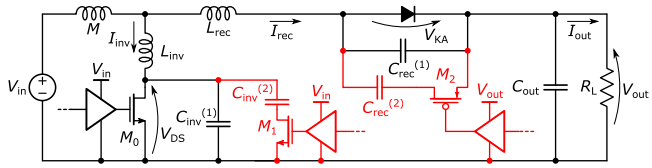

Fig. 3. Schematic of the boost resonant class-E converter allowing dual-frequency control. The additional cost with respect to the standard ON–OFF control in terms of hardware devices is highlighted in red.

B. Dual-Frequency Class-E Converter Design

The dual-frequency control technique we propose is a direct consequence of the multiple possible ways in which (4) can be denormalized starting from the same dimensionless solution $\{k_I, k_R, q_M, q_I, q_R\}$.

In more details, let us assume that, given V_{in}, V_{out}, I_{out}, f_s and the solution $\{k_I, k_R, q_M, q_I, q_R\}$, one obtains from (4) the corresponding values for the circuit components M, L_{inv}, L_{rec}, C_{inv}, and C_{rec}. Let us also assume that, with V_{in} and V_{out} remaining constant, the desired output power must be decreased by a factor $\alpha < 1$ so that the output current has to be set to αI_{out}. According to (4), we have a few possibilities to satisfy the new constraint:

1) The most intuitive one is to maintain f_s constant. In this case, (4) is still satisfied by adopting M/α, L_{inv}/α, L_{rec}/α, αC_{inv}, and αC_{rec} for the values of the circuit components.
2) Another possibility is to increase the switching frequency to f_s/α. In this case, (4) is satisfied if one chooses the same values of M, L_{inv}, and L_{rec} as in the original solution, and decreases the resonant capacitances to $\alpha^2 C_{\mathrm{inv}}$ and $\alpha^2 C_{\mathrm{rec}}$.

The latter approach is extremely interesting from a hardware point of view as it shows that, to decrease the output power, it is enough to increase the oscillating frequency, and decrease the values of the resonant capacitances (e.g., by simply disconnecting part of them from the circuit—assuming, for instance, that they are obtained by more capacitors connected in parallel—via an auxiliary switch). Noticeably, no changes are required to the magnetic elements.

In other words, in a real circuit implementation, we may change the output current by adopting the very simple schematic of Fig. 3. The circuit is designed to work at an operating frequency $f_s = f_s^{(1)}$ with resonant capacitances $C_{\mathrm{inv}} = C_{\mathrm{inv}}^{(1)} + C_{\mathrm{inv}}^{(2)}$ and $C_{\mathrm{rec}} = C_{\mathrm{rec}}^{(1)} + C_{\mathrm{rec}}^{(2)}$, delivering $I_{\mathrm{nom}}^{(1)} = I_{\mathrm{out}}$. When the output current has to be decreased to $I_{\mathrm{nom}}^{(2)} = \alpha I_{\mathrm{out}}$, the switching frequency is increased to $f_s/\alpha = f_s^{(2)}$, and the two

extra capacitors $C_{\rm inv}^{(2)}$ and $C_{\rm rec}^{(2)}$ are disconnected from the circuit so that $C_{\rm inv} = C_{\rm inv}^{(1)}$ and $C_{\rm rec} = C_{\rm rec}^{(1)}$. Since both solutions correspond to the same optimal dimensionless solution $\{k_I, k_R, q_M, q_I, q_R\}$, they both feature ZVS and ZVDS.

The only critical point from the hardware point of view is the design of the auxiliary switches. Our suggestion is to design the switch connecting $C_{\rm inv}^{(2)}$ as an NMOS (M_1 in the figure), driven by a gate driver whose supply voltage is $V_{\rm in}$. The switch connecting $C_{\rm rec}^{(2)}$ can be a PMOS (M_2 in the figure) driven by a gate driver whose supply voltage is $V_{\rm out}$. This solution, based on the observation that the voltage at the drain of M_1 is always positive, and that the one at the drain of M_2 is always lower than $V_{\rm out}$, allows both switches to correctly turn OFF when required.

The dual solution based on a switched inductor approach could also be adopted. Assuming to decrease the output current to $\alpha I_{\rm out}$, it is possible to rely on the same normalized solution by decreasing the switching frequency to αf_s and increasing magnetics to M/α^2, $L_{\rm inv}/\alpha^2$, and $L_{\rm rec}/\alpha^2$, while keeping capacitances constant. The value of the inductance can be changed assuming to implement the inductors as a series of multiple devices, and by shorting some of them when required. Even if possible, this solution is not suggested, as it would be far more complex from the hardware point of view with respect to the switched-capacitor case. First of all, three switches are required instead of two. Then, the implementation of the switches by means of MOS devices would be difficult as it is not possible to identify a configuration where the source terminal voltage is at a constant level, as in the switched capacitor case.

The idea grounding this article is to introduce a dimming mechanism, similar to what happens in the standard ON–OFF approach, based on the architecture of Fig. 3. Instead of alternating the converter in an ON-mode (output current $I_{\rm nom}$, for a fraction of time D) and an OFF-mode (output current 0, for a fraction of time $1-D$), we alternate two converter configurations at different frequencies. In the first one, the converter is operating, for a ratio of time D, at $f_s^{(1)}$, and the two extra capacitors are connected to the circuit so that a current $I_{\rm nom}^{(1)}$ is delivered to the load. In the second one, for a fraction of time $1-D$, the oscillation frequency is $f_s^{(2)}$, the extra capacitors are disconnected, and the current delivered to the load is $I_{\rm nom}^{(2)}$. By *dynamically* alternating the two modes, only the weighted average of the two currents is delivered to the output so that (3) holds. In other words, it is possible to regulate, with the advantages detailed later, the output current in the range $[I_{\rm nom}^{(1)}, I_{\rm nom}^{(2)}]$. Lower values are still obtainable with the standard ON–OFF approach, if needed.

The additional hardware cost with respect to the ON–OFF approach has been highlighted in Fig. 3, in red. Neglecting the control unit (that is required also with the ON–OFF methodology, and whose design is out of the scope of this article), two additional capacitors and two MOS switches only, are required. This is a fairly low cost in terms of hardware devices. Beyond that, even the increase in terms of required energy, or additional losses, is expected to be limited. Some details on this are provided in Section IV.

To show the advantages of our approach, a 5 V-to-10 V converter with dual-frequency control capabilities and $\alpha = 0.5$ has been designed, assuming that $P_{\rm nom}^{(1)} = 1\,{\rm W}$ ($I_{\rm nom}^{(1)} = 100\,{\rm mA}$) at $f_s^{(1)} = 4\,{\rm MHz}$, and $P_{\rm nom}^{(2)} = 0.5\,{\rm W}$ ($I_{\rm nom}^{(2)} = 50\,{\rm mA}$) at $f_s^{(2)} = 8\,{\rm MHz}$.

In the corresponding simulation, we used a model of the NMOS IRLM0030TRPBF by Infineon as main switch M_0, and of a Nexperia PMEG6030ELP Schottky barrier diode as rectifier diode D_0. An additional instance of an IRLM0030TRPBF is used as M_1, whereas a PMOS BSS315PH6327XT by Infineon is used as M_2.

Resonating capacitors are considered ideal, whereas inductors have been considered lossy, with quality factors $Q = 55$ at $4\,{\rm MHz}$ and $Q = 75$ at $8\,{\rm MHz}$. Furthermore, three additional $0.1\,\Omega$ series resistances have been added to emulate current sensing resistors for M, $L_{\rm inv}$, and $L_{\rm rec}$.

The design has been obtained by following the many tradeoffs suggested in [15]. The duty cycle of the main clock is set to 30%, as this value ensures reduced stress on the main switch. The two degrees of freedom k_I and k_R of the dimensionless system should be sufficiently far from 0, to reduce the rms value of the currents in the circuit, and so increase the efficiency. At the same time, the product $k_I k_R$ should be sufficiently lower than 1 to ensure robustness to parameter variations in a real circuit implementation. The operating point $k_I = -0.75$ and $k_R = -0.75$ appears to be a good choice. The optimum class-E condition is obtained for $q_I = 0.23$, $q_R = 0.21$, and $q_M = -0.51$. The dimensionless solution leads to $L_{\rm inv} = L_{\rm rec} = 336\,{\rm nF}$ $M = 1.01\,\mu{\rm H}$, $C_{\rm inv}^{(1)} = 605\,{\rm pF}$, $C_{\rm rec}^{(1)} = 648\,{\rm pF}$, and $C_{\rm inv}^{(2)} = 2.71\,{\rm nF}$, $C_{\rm rec}^{(2)} = 2.83\,{\rm nF}$. These values, with respect to the straightforward conversion given by (4), have been modified to keep into account devices nonidealities. In particular, capacitor values have been slightly decreased to compensate the parasitic capacitances of the IRLM0030TRPBF, the PMEG6030ELP and the BSS315PH6327XT, evaluated to be 125, 180, and 100 pF, respectively.

Simulation results, showing the profile of the drain-to-source voltage $V_{\rm DS}$ and the $L_{\rm inv}$ current $I_{\rm inv}$, are plotted in Fig. 4. Part (a) refers to a standard ON–OFF control for the converter operating at $f_s^{(1)} = 4\,{\rm MHz}$, with dimming ratio $D = 75\%$ to achieve an expected $I_{\rm out} = 75\,{\rm mA}$. Part (b) refers to the proposed dual-frequency approach with dimming ratio $D = 50\%$, to get the same expected $I_{\rm out} = 75\,{\rm mA}$. Both cases feature almost perfect ZVS and ZVDS conditions once transient from one state to the other one is completed.

The most impressive difference is that, in the ON–OFF approach, the turn-OFF transient time is extremely long. This is indeed expected. Roughly speaking, transients are observed since there is an abrupt change in some parameters of the system or in the control function (in this case, the clock), that implies a change in the steady-periodic solution of the system. Switching instantaneously from one steady-periodic solution to another one is generally not possible, as this would imply a discontinuity in the system state variables. To ensure continuity between the old and the new steady-state solution, a transient response is

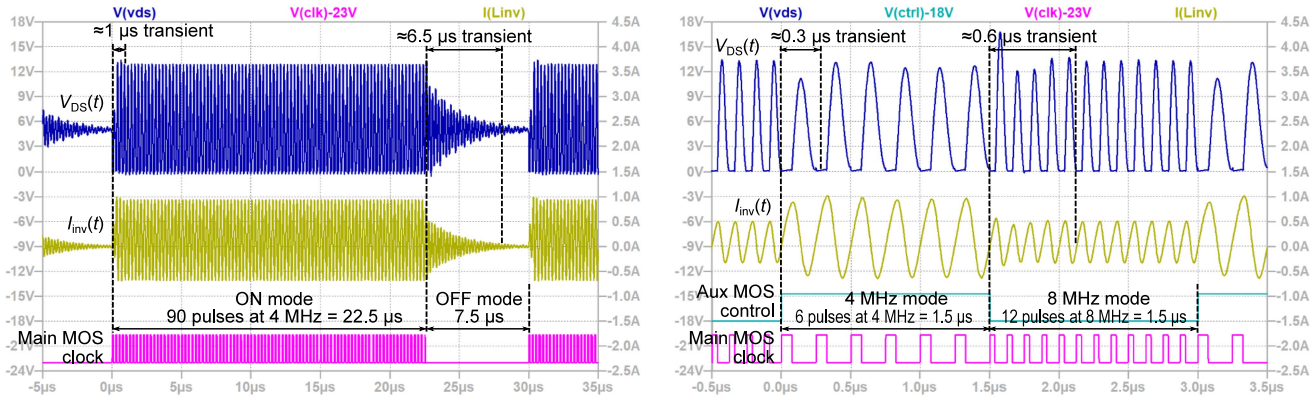

Fig. 4. Drain-to-source voltage $V_{\rm DS}$ and inverter current $I_{\rm inv}$ in a simulation of a controlled class-E boost converter. (a) Time required to turn-OFF the converter under the ON–OFF control is extremely long, setting the upper bound on the dimming frequency f_d. (b) Transients in the proposed dual-frequency control are extremely short, allowing a much higher f_d.

generated. The length of the transient depends both on the entity of the aforementioned discontinuity, and on the capability of the system to dissipate energy, associated with resistive elements of the circuit (mainly the load, but also all parasitic resistances).

By considering this simple model, the complexity of the transient length computation is clear. Hence, it is difficult even to provide an estimation of it; however, we can intuitively say that, in order to turn the converter OFF, all inductor currents should be instantaneously set to zero. Being this not possible, a transient is generated. Furthermore, since in the OFF-mode the load is not powered anymore by the converter, there are no resistive elements (besides the parasitics ones) capable of quickly dissipating the energy associated with the residual oscillations. This slows down the transient.

Since the transient time should be at least shorter, if not negligible, with respect to the converter ON and OFF times, this sets a very low upper bound to the dimming frequency f_d. The consequence, according to (2), is an important low-frequency output ripple or the need for a very large output filter capacitor. Conversely, transient times are much shorter in the dual-frequency example since the load is always receiving energy from the converter, both in the $f_s^{(1)}$-mode and $f_s^{(2)}$-mode, and can. therefore. dissipate the energy associated to the transient response. It implies that a much higher f_d is allowed in this case.

C. Dual-Frequency Class-E Converter Optimization

One important point to be noted in the previous design example is that the two degrees of freedom k_I and k_R were (somehow arbitrarily) set following suggestions in [15] with the only aim of ensuring the good behavior of the converter. No attempt was made to use these degrees of freedom with the aim of optimizing the performance of the converter when working in the dual-frequency mode.

One significant way to do so is to choose k_I and k_R to minimize the transient time from one state to another one, as this would maximize the dimming frequency, and either minimize the output ripple or relax constraints on the output filter capacitance.

To this aim, let us consider the scatter plot in the middle of Fig. 5, which is the normalized solution state space for the degrees of freedom k_I–k_R taken from [15] for the (ideal version) of the converter topology under investigation. Here, a point in the scattered blue area represents a choice of the two degrees of freedom that allows an optimal behavior (both ZVS and ZVDS), whereas orange points correspond to solutions where only the ZVS suboptimal behavior can be achieved. The red line sets the feasibility condition limit in a real system.

The point $(-0.75, -0.75)$, highlighted as "A," is the one considered in the previous example. The evolution of the optimal converter given this choice of the degrees of freedom is plotted on the left, where one shows the voltages $V_{\rm DS}$ and $V_{\rm KA}$, and the currents $I_{\rm inv}$ and $I_{\rm rec}$, both for the $f_s^{(1)} = 4\,\text{MHz}$ and the $f_s^{(2)} = 8\,\text{MHz}$ systems. For $t < 0$, we have reported the waveforms for the 8-MHz configuration, and for $t > 0$ those for the 4-MHz configuration. For the sake of thoroughness, the dual transition, i.e., 4-to-8 MHz, is shown with transparent lines.

The highlighted waveforms are not continuous at $t = 0$ due to a step in $I_{\rm rec}$ (see the yellow line in the left plot of Fig. 5). Indeed, this is the expected discontinuity that, according to the simple model proposed previously, generates a transient response: the larger the discontinuity, the longer the transient.

Yet, the transient time can be shortened by reducing this discontinuity. Ideally, it can be completely removed by decreasing the discontinuity to zero, i.e., by imposing waveform *continuity* at the switching instant $t = 0$. This happens if and only if $I_{\rm rec}(0) = 0$.[1] If we are able to ensure this condition, we can expect a ZT) response.

[1]It has been shown in [15] that the $I_{\rm rec}$ waveforms, for the $f_s^{(1)}$ and the $f_s^{(2)}$ cases, are obtained from their dimensionless counterpart $i_{\rm rec}$ multiplied by two different scaling factors. Accordingly, the only way to ensure the continuity at $t = 0$ is to have $i_{\rm rec}(0) = 0$ so that $I_{\rm rec}(0) = 0$ independently of the scaling factor.

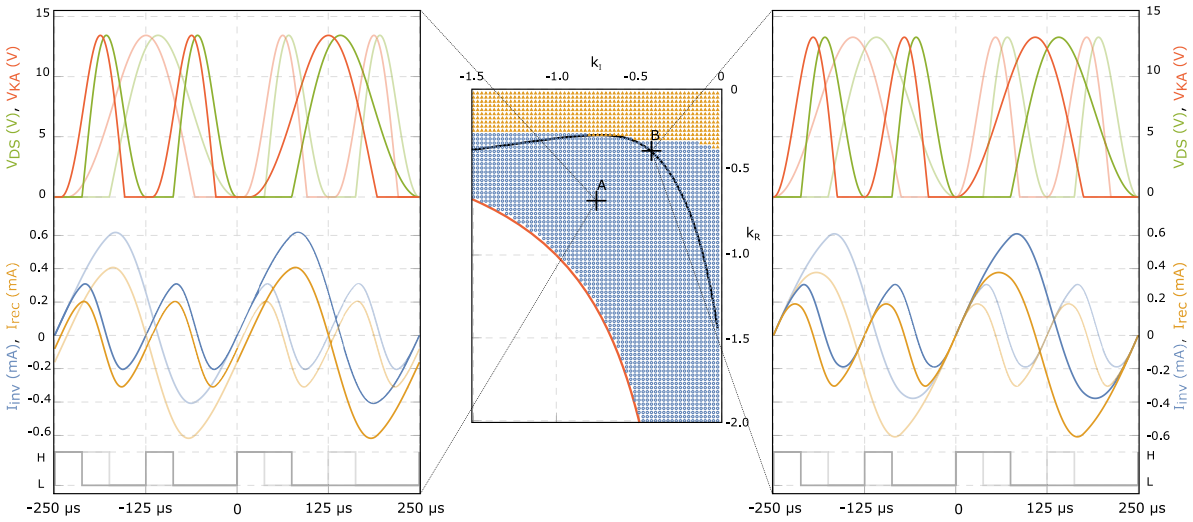

Fig. 5. Space of the solutions of the class-E design problem in the lossless normalized system for main clock duty cycle 30%. Blue points refer to the optimal (ZVS + ZVDS) class-E solution, and orange points to a sub-optimal solution (ZVS only). The points laying on the black line indicate solutions featuring ZT. Two examples of waveforms are also shown, one (on the left) not featuring ZT, and one (on the right) featuring ZT.

It is interesting to wonder whether there are points, among the space of solutions, capable of ensuring a ZT response. Indeed, many points exist, and they have been highlighted with the black line of the center scatter plot in Fig. 5. Regrettably, the computation of all these points has the same complexity and the same drawbacks as the computation of the optimal solution of the normalized class-E converter according to the procedure in [15]. Due to this, it is not possible to provide here a closed-form equation able to identify them, and the easiest way to compute them is by using the tools provided in [15].

As an example, the point $(-0.4, -0.4)$, highlighted as "B," belongs to the ZT locus of the points. The observed behavior for the design of the ideal converter using these values of the degrees of freedom is shown on the right, and the waveforms of the 8-MHz configuration and that of the 4 MHz, one join with no discontinuity at $t = 0$.

With the aim of exploiting ZT in a converter where nonideal components are employed, we consider here a second design with the same specifications as the first one described so far and corresponding to $k_I = -0.4$ and $k_R = -0.4$ in the ideal setting. Indeed, when introducing losses parameters, the ZT line is slightly modified with respect to the one shown in Fig. 5, but we can still approximate k_I and k_R with -0.4 so that optimum soft-switching condition is ensured for $q_I = 0.24$, $q_R = 0.22$, and $q_M = -0.11$.

This dimensionless solution leads to real components given by $L_{\text{inv}} = L_{\text{rec}} = 332\,\text{nF}$ $M = 221\,\text{nH}, C_{\text{inv}}^{(1)} = 558\,\text{pF}, C_{\text{rec}}^{(1)} = 645\,\text{pF}$ and $C_{\text{inv}}^{(2)} = 2.56\,\text{nF}$, and $C_{\text{rec}}^{(2)} = 2.77\,\text{nF}$.

Simulation results are plotted in Fig. 6 and show, as expected, a ZT response, with no visible transient when switching to the 4-MHz configuration to the 8-MHz one, and vice-versa.

This condition is clearly the optimal one for a dimming-based control, as it allows to push the dimming frequency f_d to extremely high values, that can be of almost the same order of magnitude as $f_s^{(1)}$ and $f_s^{(2)}$. More precisely, the upper bound

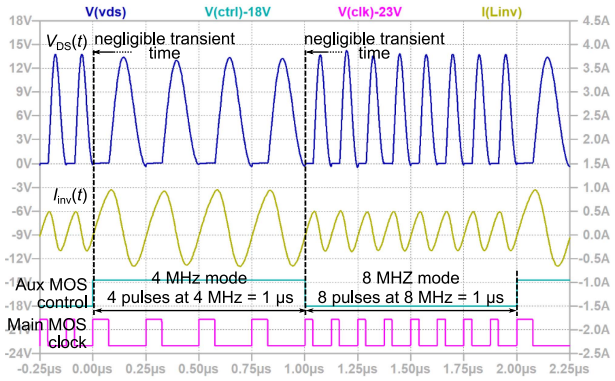

Fig. 6. Simulation of the dual-frequency converter designed to work in a ZT point. Waveforms clearly show no settling time when switching from one state to the other one. Furthermore, ZVS and ZVDS are clearly preserved in both states.

of the dimming frequency can be calculated by considering one only high-frequency and one low-frequency period so that $f_d = 1/(1/f_s^{(1)} + 1/f_s^{(2)})$.

IV. Experimental Results

A prototype of the 5-to-10 V class-E boost converter capable of dual-frequency control and optimized for ZT, described in the previous section, has been assembled and tested.

The values of inductances and capacitances have been approximated to fit values easily achievable with commercial devices. More precisely, $L_{\text{inv}} = L_{\text{rec}} = 330\,\text{nH}$, $M = 220\,\text{nH}$, and $C_{\text{inv}}^{(1)} = 550\,\text{pF}$, $C_{\text{rec}}^{(1)} = 660\,\text{pF}$ and $C_{\text{inv}}^{(2)} = 2.5\,\text{nF}$, $C_{\text{rec}}^{(2)} = 2.8\,\text{nF}$. The output filter capacitance has been set to $20\,\mu\text{F}$.

Ceramic capacitors with a high-quality dielectric (e.g., C0G) have been used for the resonant capacitances to support the assumption of ideality, as they are known to have very high-quality factors ($Q > 1000$). Inductors have been selected as

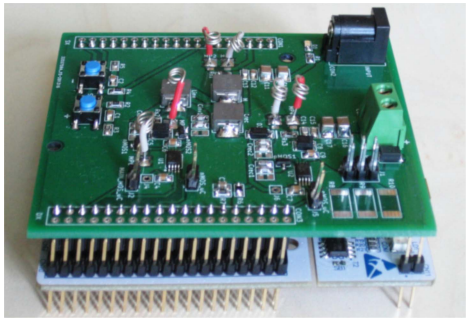

Fig. 7. Picture of the designed prototype that fits on top of the NUCLEO-F334R8 board.

commercial shielded molded inductors from the IHLP-2525CZ-01 series by Vishay Dale. Their quality factors have been measured as $Q_{L_{\text{inv}}} \approx Q_{L_{\text{rec}}} \approx 43$ and $Q_M \approx 42$ at 8 MHz and $Q_{L_{\text{inv}}} \approx Q_{L_{\text{rec}}} \approx 60$ and $Q_M = 58$ at 4 MHz. Finally, all MOS transistors are driven by means of an ISL5510IVZ, a high-speed MOS gate driver by Renesas.

The prototype, which can be seen in Fig. 7, has been designed to fit on top of a Nucleo-F334R8 by STMicroelectronics, used to provide all timing signals. This board is a mainstream 32-bit MCU, based on an ARM microcontroller embedding a high-resolution timer module, used to generate both the main clock signals and the additional MOS control signal. The ARM microcontroller also embeds a very simple feedback loop; however, we consider the design of this feedback, including the stability analysis and bandwidth, out of the scope of this article. In any case, any control specifically designed for the ON–OFF approach is expected to correctly work in dual-frequency one, too.

Measurements are shown in Fig. 8. When the output voltage is regulated at $V_{\text{out}} = 10\,\text{V}$, the system clearly features optimum soft-switching condition (both when operating at 4 and at 8 MHz) and ZT, in agreement with the developed model and with circuit simulation. In our prototype, we were able to rise the dimming frequency to $f_d = 500\,\text{kHz}$, that is a very high value with respect to other solutions in the Literature, in particular when compared to the 4–8 MHz operating frequencies. In fact, the ratio between the operating frequency and the dimming frequency is, in our case, as low as 16–8.[2] The proposed prototype works with a dimming frequency $16\times$ smaller than the higher available switching frequency (i.e., $f_d = 500\,\text{kHz}$ and $f_s^{(2)} = 8\,\text{MHz}$) that is an excellent result with respect to the state-of-the-art examples [23], [25], [26] mentioned in Section II, and in which f_d is between $100\times$ and $1200\times$ smaller than the switching frequency. With such a high value of f_d, the low-frequency component of the output ripple is negligible, and in the figure, the observed output ripple has indeed a high-frequency component only. This is an important result, especially considering that the output filter capacitance is as low as $20\,\mu\text{F}$.

The measured efficiency of the converter (considering the converter alone, i.e., neglecting the Nucleo board and the gate drivers), depends obviously on the output current (and so on the dimming ratio) and ranges from 70% in the high-power, 4 MHz state (it results in $I_{\text{in}} = 270\,\text{mA}$ and $I_{\text{out}} = 95\,\text{mA}$), to 73% in the low-power, 8-MHz state (it results in $I_{\text{in}} = 126\,\text{mA}$ and $I_{\text{out}} = 47\,\text{mA}$) and it is aligned with the expected efficiency given the values of the lossy parameters. By means of a SPICE simulation, it is also possible to investigate how conduction losses are distributed. The main observed contribution is given by the finite-Q of the inductors and by the current sensing resistors, required in our prototype for the verification of the correct behaviour of the circuit. Then, as in the majority of dc–dc converters, the other large source of losses is the rectifying diode (slightly smaller than 20%). A similar amount of power

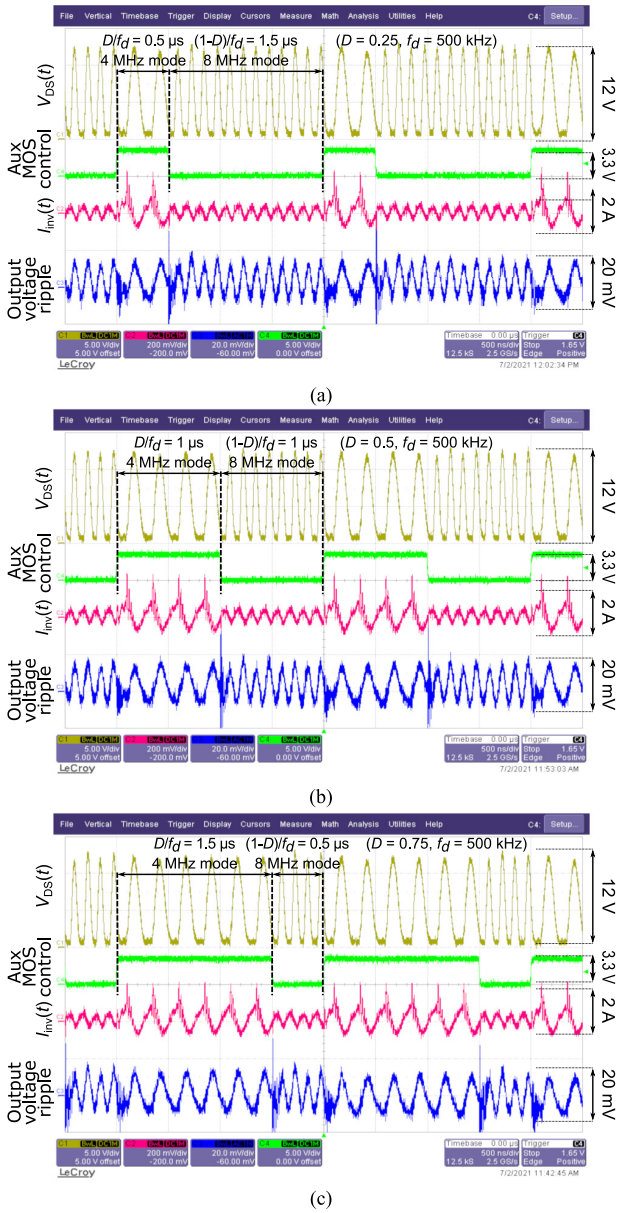

Fig. 8. Measurements from the designed prototype. From top to bottom: Drain-to-source voltage V_{DS}; additional MOS control signal; inverter current I_{inv}; output voltage ripple. (a) Dimming ratio 25%. (b) Dimming ratio 50%. (c) Dimming ratio 75%.

[2]i.e., a number of high-frequency periods between 8 and 16 is observed in a dimming period.

is cumulatively dissipated by the main MOS ($\approx 5\%$) and the two auxiliary ones ($\approx 15\%$). The analysis based on the measured current waveforms of Fig. 8 and the estimation of the main circuit parasitics confirm this distribution.

It is worth stressing that only a negligible increase in the conduction losses can be expected when the proposed dual-frequency technique is employed instead of the standard ON–OFF methodology. To show this, we considered the simulations of the two converters with the same design specifications and the same circuit elements, except for the additional switches and capacitors that are only needed for the dual-frequency control. In order to ensure the same output power, the converter employing the ON–OFF control operates at $4\,\mathrm{MHz}$ with a dimming ratio $D = 0.75$ to achieve the expected output current of $75\,\mathrm{mA}$. On the other hand, the converter employing the ZT dual-frequency control alternates between 4 and $8\,\mathrm{MHz}$ with $D = 0.5$ to get the same output current. In both cases, the power required to drive all MOS devices is not taken into account but, being f_d one order of magnitude lower than the oscillation frequency, driving losses are certainly dominated by the main switch, present in both implementations. Conduction losses are the same for corresponding elements in the two circuits, and therefore, the only additional contribution to losses for the dual-frequency control is given by the two auxiliary MOS devices. This is just a small fraction of the overall conduction losses, evaluated in the proposed prototype to be $\approx 15\%$ of the total value.

V. Conclusion

In this article, a new dual-frequency control for Class-E dc–dc resonant converters has been proposed. The main advantage with respect to the state of the art is that the proposed control allows reaching ZT response when the converter is switched from the state in which it is operating at the first frequency, to the state in which it is operating at the other one. This allows to extremely increase the dimming frequency f_d at which the two states are switched while preserving the class-E optimum condition during all converter operations. As a proof of concept, we presented a dc–dc converter prototype capable of alternatively working either at 4 or $8\,\mathrm{MHz}$ and controlled with f_d of almost the same order of magnitude. The prototype operates with $f_d = 500\,\mathrm{kHz}$, that is $16\times$ smaller than the higher available switching frequency. This is an excellent result compared to the mentioned state-of-the-art examples, where the observed reduction of f_d with respect to the operating frequency is between $100\times$ and $1200\times$, with evident advantages in terms of output voltage ripple. The measurements confirm an almost perfect matching with the expected results by always guaranteeing both the optimal class-E converter behavior and the ZT time when switching from one frequency to the other.

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