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Original
A 0.01mm2, 0.4V-VDD, 4.5nW-Power DC-Coupled Digital Acquisition Front-End Based on Time-Multiplexed Digital Differential Amplification / Crovetti, PAOLO STEFANO; Rubino, Roberto; Pedro, Toledo; Musolino, Francesco; Klimach, Hamilton; Chen, Yong; Richelli, Anna. - ELETTRONICO. - (2022). (Intervento presentato al convegno ESSCIRC 2022-IEEE 48th European Solid State Circuits Conference (ESSCIRC) tenutosi a Milan (Italy) nel 19-22 September 2022) [10.1109/ESSCIRC55480.2022.9911357].

Availability:
This version is available at: 11583/2972539 since: 2022-10-23T09:04Z

Publisher:
IEEE

Published
DOI:10.1109/ESSCIRC55480.2022.9911357

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(Article begins on next page)
A 0.01mm$^2$, 0.4V-$V_{DD}$, 4.5nW-Power DC-Coupled Digital Acquisition Front-End Based on Time-Multiplexed Digital Differential Amplification

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Abstract—A reconfigurable, high-impedance, DC-coupled low-frequency digital acquisition front-end (DAFE) suitable to operate under a power supply voltage ranging from 0.2 to 1V down to 600pW power is presented in this paper. Matching-indifferent DC accuracy over a rail-to-rail input range is uniquely achieved by the new time-multiplexed digital differential amplification technique at ultra-low area and without chopping and auto-zeroing. A 180nm testchip of the proposed DAFE occupies 0.00945 mm$^2$ and draws 4.5 nW at a 0.4 V supply, has a 120 Hz gain-bandwidth product, with an in-band input noise of 11.3 $\mu$V$_{p-p}$, a 137 $\mu$V input offset voltage standard deviation, 65.7 dB CMRR, 63.8 dB PSRR, and provides a 46.5 dB-SFDR, 6.9-bit-ENOB digitized output at -12 dBFS.

Index Terms—DC-coupled digital acquisition front-end (DAFE), time-multiplexed digital differential amplification (TMD$^2$A), CMOS, ECG, IoT.

I. INTRODUCTION

Ultra-compact, energy-quality scalable sensor interfaces operating from a low, extremely variable supply under a < 10 nW power budget are required to enable next-generation sub-millimeter remotely-powered implantable biosensors [1] and energy-autonomous IoT nodes [2]. In this scenario, AC-coupled acquisition front-ends (AFEs) with < 10 nW power [3], [4], [5] and 0.01-mm$^2$-scale area [6], [7] have been demonstrated for ECG, EEG and audio signal acquisition.

DC-coupled AFEs, needed e.g. in electrochemical and temperature sensors acquisition, pose further challenges, and DC accuracy (i.e. low DC offset/drifts, high DC CMRR and PSRR) is achieved by chopping [8], [6] and/or auto-zeroing [9], at the cost of much increased power, area and lower input impedance.

In this paper, a scalable, DC-coupled, biosignal digital AFE (DAFE) with inherent DC offset and drift suppression and direct digitization is demonstrated in 180nm CMOS aiming to simultaneously achieve order-of-nanowatt power, area-efficiency and decent DC accuracy over a wide supply range.

II. TIME-MULTIPLEXED DIGITAL DIFFERENTIAL AMPLIFICATION (TMD$^2$A)

The proposed DAFE entails inherently offset- and drift-free, differential-mode amplification without relying on matching, chopping or auto-zeroing, thanks to the new time-multiplexed digital differential amplification (TMD$^2$A) approach illustrated in Fig.1. Here, the same single-ended comparator is multiplexed in time to compare the non-inverting ($v^+$) and the inverting ($v^-$) differential analog inputs against the same threshold (assumed to be 0 V in the following), and differential-mode signal amplification is achieved as in a Digital-Based Amplifier (DB-Amp) [10].

In details, after $v^+$ and $v^-$ are simultaneously sampled, the switch in Fig.1 is operated in A, so that $v^+$ is in series to the common-mode (CM) compensating floating voltage source (CM-FVS) $v_{CCM}$, and the input voltage

$$v^{(A)} = v^+ + v_{CCM} = \frac{v_D}{2} + v_{CM} + v_{CCM}$$

is applied to the comparator. The comparator digital output is 1 if $v^{(A)} > 0$ and 0 otherwise, and is stored in $D^{(A)}$. Then,
the switch is operated in B, the comparator input is
\[ v^{(B)} = v^- + v_{CCM} = -\frac{v_D}{2} + v_{CM} + v_{CCM} \]
and the corresponding comparator output is stored in \( D^{(B)} \).

Based on \( D^{(A)} \) and \( D^{(B)} \), either \( v_{OUT} \) or \( v_{CCM} \) are updated as in a DB-Amp [10], i.e. if \( (D^{(A)}, D^{(B)}) = (1, 0) \) \( ((D^{(A)}, D^{(B)}) = (0, 1)) \), which implies that \( v_D > 0 \) \( (v_D < 0) \), \( v_{OUT} \) is increased (decreased) by a minimum step, and \( v_{CCM} \) is kept unchanged. On the contrary, if \( (D^{(A)}, D^{(B)}) = (1, 1) \) \( ((D^{(A)}, D^{(B)}) = (0, 0)) \), \( v_{CCM} \) is decreased (increased) by a minimum step so that to track \( v_{CM} \), aiming to enforce \( |v_{CM} + v_{CCM}| < |v_D/2| \), as required to detect the sign of \( v_D \) in the next cycles, while \( v_{OUT} \) is hold.

A. Transistor-Level Design

In the proposed DAFE, TMD\(^2\)A is realized in 180nm CMOS by switched capacitor (SC) techniques [see schematic in Fig.2(a)]. A small standard cell CMOS digital buffer [transistor level details in Fig.2(a)] is used as a single-ended comparator, while the input sampling capacitors, the CM-FVS and the output voltage source are implemented by pF-range Metal-insulator-Metal (MiM) capacitors, and the floating switches are designed by CMOS pass gates operated at bootstrapped voltage. The DB-Amp core is a finite state machine (FSM) automatically synthesized in standard-cell logic, whose state transition graph is shown in Fig.3.

B. Circuit Operation

In state A (B), the input capacitor \( C_{in,P} (C_{in,M}) \), charged at the non-inverting (inverting) input voltage \( v^+ (v^-) \) sampled at the previous cycle (see below), is connected in series to \( C_{CM} \) at the buffer input (Fig.4, states A-B in the left and right column) and its digital output is stored in the D-Flip Flop \( D^{(A)} (D^{(B)}) \) at the next clock edge. Depending on \( (D^{(A)}, D^{(B)}) \), the FSM evolves to states C+/C-, to update the output voltage (left column in Fig.4), or to states E+/E-(right column in Fig.4), to update the voltage \( v_{CCM} \) across \( C_{CM} \).

In order to increase (decrease) the output voltage, the fF-range capacitor \( C_{0,OUT} \) is first pre-charged to \( V_{DD}/2 \) \((-V_{DD}/2)\) in state C+ (C-), and then connected in parallel to \( C_L \) in state D, so that \( v_{OUT} \) is increased (decreased) by:

\[ \Delta V_{OUT} = \frac{C_{0,OUT}}{C_L + C_{0,OUT}} \left( \frac{V_{DD}}{2} - v_{OUT} \right) \]

In the same state D, \( v^+ \) and \( v^- \) are simultaneously sampled on \( C_{in,P} \) and \( C_{in,M} \). In a similar fashion, in E+ (E-), the fF-range capacitor \( C_{0,CM} \) is pre-charged to \( V_{DD}/2 \) \((-V_{DD}/2)\) and then connected in parallel to \( C_{CM} \) in the next state F, to update \( v_{CCM} \) as demanded to compensate the CM input component, as well as drifts and process, voltage and temperature (PVT)-related variations in the CMOS buffer logic threshold. In the
same state F, $v^+$ and $v^-$ are also sampled, as in D. Either state D or state F conclude an operating cycle, and are followed by state A in the next cycle.

As in [10], [11], the circuit operates as an analog differential amplifier with a gain-bandwidth (GBW) product proportional to the clock frequency. When connected in negative feedback under fixed capacitive load [e.g. in the unity-gain configuration as in Fig. 2(b)], the circuit operates as a delta modulator [6], [7] (see Fig. 2(c)), and a digitized version of the output can be retrieved in post-processing from the sequence of the DB-Amp FSM states by infinite impulse response (IIR) digital filtering.

III. EXPERIMENTAL RESULTS

A CMOS test-chip of the proposed DAFE has been fabricated in 180 nm and occupies merely 0.00945 mm$^2$ [micrograph in Fig. 5(a)]. When tested at 25°C in unity-gain feedback configuration [Fig. 2(b)] with $C_L = 50 \text{pF}$, the DAFE operates under a 0.2-V supply voltage range with a rail-to-rail input/output swing, at a clock frequency $f_{\text{clk}}$ ranging from 28 kHz to 15 MHz (upper-limited by the analog pads), corresponding to a scalable GBW from 70 Hz to 40 kHz. From Fig. 5b, the power consumption varies from 600 pW at 0.2 V to 9.58 $\mu$W at 1 V (from 2.0 $\mu$W at 0.25 V to 1.77 $\mu$W at 1 V) under $f_{\text{clk}} = f_{\text{max}}$ ($f_{\text{clk}} = 50$ kHz). At 0.4 V supply ($V_{\text{DD}}$) and $f_{\text{clk}} = 50$ kHz, considered hereafter in the DAFE characterization, the power is 4.5 $\mu$W.

Based on the DC characterization at 25°C, 0.4 V $V_{\text{DD}}$, $C_L = 50 \text{pF}$ and $f_{\text{CLK}} = 50$ kHz (see Tab. I), the input offset voltage of six dice ranges from $-188$ to $+230$ $\mu$V, the open-loop DC gain from 36.3 to 42.7 dB, the CMRR from 60.0 to 74.0 dB and the PSRR from 54.0 to 83.9 dB. These results prove the reasonable DC accuracy of the proposed DAFE. Moreover, the DC input resistance of all dice is above 1 G$\Omega$.

The time-domain analog output of sample #2 in unity-gain feedback [$V_{\text{OUT}}$ in Fig. 2(b)] under 0.1 Hz, 360 mV$_{pk-pk}$ sine-wave input, and under a rail-to-rail square-wave input are shown in Figs. 6(a)-(b). The spectrum of the signal in Fig. 6(a) is shown in Fig. 6(c) and reveals a THD of 1.3%. Based on the open-loop frequency response reported in Fig. 6(c), the DC gain is 39.9 dB and the GBW is 120 Hz. The open-loop input-referred noise spectrum in Fig. 6(e) reveals an in-band noise power spectral density of $1.03 \mu$V/$\sqrt{\text{Hz}}$ and an effective suppression of $1/f$ noise. The integrated input noise in the 0.05-1 Hz (0.05-120 Hz) bandwidth is $1.03 \mu$V$_{\text{rms}}$.

In Figs. 7(a)-(b), the time-domain waveform and the spectrum of a 50 mV$_{pk}$ (i.e. -12 dBFS), 1 Hz sine-wave reconstructed from the digital output stream of the DAFE post-processed off-chip by an IIR filter as in [6] is shown. The results reveal 46.5 dB SFDR, 45.0 dB THD and 43.4 dB SNDR, corresponding to 6.9 ENOB, and demonstrate the operation of the DAFE as an ADC. An ECG signal reconstructed from the digital output is shown in Fig. 7(c) and confirms the suitability of the DAFE to biosignal acquisition.
TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH LOW FREQUENCY SENSOR INTERFACES

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<td>AFE</td>
<td>AFE</td>
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<td>0.006</td>
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<td>Normalized Area</td>
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<td>1.42</td>
<td>47.3</td>
<td>23.1</td>
<td>23.7</td>
<td>43.2</td>
<td>30.9</td>
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<td>0.5</td>
<td>0.6</td>
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<td>1.8</td>
<td>0.2/0.8</td>
<td>0.6/1.2/3.3</td>
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<tr>
<td>Input Range</td>
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<td>N/A</td>
<td>N/A</td>
<td>5°/30°</td>
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<td>N/A</td>
<td>N/A</td>
<td>0.2-1</td>
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<td>Power</td>
<td>nW</td>
<td>3.300</td>
<td>1.275</td>
<td>3</td>
<td>8.3(²)</td>
<td>1.800</td>
<td>378,000</td>
<td>790</td>
<td>990</td>
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<td>Bandwidth</td>
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<td>11,000</td>
<td>1.5-370</td>
<td>470</td>
<td>0.5-100</td>
<td>1,450,000</td>
<td>670</td>
<td>500</td>
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<td>Input Resistance</td>
<td>GΩ</td>
<td>0.05</td>
<td>0.031(¹)</td>
<td>N/A</td>
<td>N/A</td>
<td>0.8(²)</td>
<td>(g)</td>
<td>0.01(²)</td>
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<td>DC Gain</td>
<td>dB</td>
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<td>N/A</td>
<td>32</td>
<td>31-59</td>
<td>40</td>
<td>0</td>
<td>57.8</td>
<td>N/A</td>
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<tr>
<td>Input Offset</td>
<td>μV</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>0.4</td>
<td>N/A</td>
<td>137(²)</td>
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<tr>
<td>In-band Noise (noise BW)</td>
<td>μVRMS(¹)</td>
<td>20(²)</td>
<td>1.150</td>
<td>3.8</td>
<td>26</td>
<td>17</td>
<td>6.7(²)</td>
<td>(0.5-100)</td>
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<td>Noise PSD</td>
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<td>N/A</td>
<td>N/A</td>
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<tr>
<td>NEF(²)</td>
<td>N/A</td>
<td>147(²)</td>
<td>0.036</td>
<td>N/A</td>
<td>N/A</td>
<td>0.2(²)</td>
<td>N/A</td>
<td>0.036</td>
<td>N/A</td>
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<tr>
<td>PEF(³)</td>
<td>13,012(²)</td>
<td>2.4</td>
<td>2.6</td>
<td>4.8</td>
<td>10.9</td>
<td>96</td>
<td>2.1</td>
<td>15.2(³)</td>
<td>6.7(²)</td>
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<tr>
<td>THD</td>
<td>%</td>
<td>1</td>
<td>0.2</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>1.5</td>
<td>N/A</td>
<td>N/A</td>
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<tr>
<td>CMRR</td>
<td>dB</td>
<td>60</td>
<td>60</td>
<td>60</td>
<td>N/A</td>
<td>134</td>
<td>N/A</td>
<td>85</td>
<td>&gt; 78</td>
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<tr>
<td>PSRR</td>
<td>dB</td>
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<td>N/A</td>
<td>63</td>
<td>N/A</td>
<td>120</td>
<td>125</td>
<td>80/75</td>
<td>N/A</td>
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<tr>
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<td>bit</td>
<td>56</td>
<td>60</td>
<td>N/A</td>
<td>N/A</td>
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<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
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</table>

(¹) NEF = Vr,n,μ/√BW, where Vr,n,μ is the rms input noise, IΔ is the supply current and BW is the bandwidth; (²) PEF = VDD · NEF²; (³) includes ADC quantization noise (and ADC current for NEF/PEF), (⁴) with DC servo loop, (⁵) LNA+ADC power considered, (⁶) estimated. (⁷) Total input current; (⁸) Input rms noise in the 0.05-120 Hz BW estimated from the measured open-loop input-referred noise spectral density n0 in Fig.6(²) as n0 = VΔBW; (⁹) Average of 6 samples; (¹⁰) StDev. of 6 samples; (¹¹) Open-loop gain; (¹²) Under 0.1 Hz, 90% rail-to-rail input; Best in bold.

IV. COMPARISON AND CONCLUSIONS

Compared with the state of the art of low-frequency AFEs in Table II, the proposed DAFE occupies the lowest normalized area (2.2X less than [7]) and works at the minimum voltage and over the widest supply range (4X wider than [3]) with rail-to-rail input/output swing, uniquely offering power-quality scalability. At 0.4 V, the power is comparable with AC-coupled AFEs [3], [5] (1.5X more than [3], in 65 nm, and 1.8X less than [5], also in 180nm), which have 3.1X-3.9X larger bandwidth and 2.3X-1.5X more in-band rms noise.

Compared to DC-coupled AFEs with similar bandwidth [6]–[8], [13], the DAFE has an inherently high input resistance (> 1 GΩ), consumes 1.2X-106X less area and 175X-733X less power, while providing a digitized output as [6], [7]. The offset, although 137X-342X larger than [8], [9], is the only reported in sub-μW AFEs. The in-band rms noise is 1.8X less than [6] and 4X more than [7], which inherently include quantization noise as the DAFE, while it is 12X more than the best [13]. The noise efficiency factor (NEF)/power efficiency factor (PEF) metrics, defined in Table II, are 1.2X worse/2.3X better than [7] and 36X/1,942X better than [6], while they are 2.6X/3.2X worse than [13], the best in Table II. The digitized output of the DAFE is slightly worse in terms of effective resolution (-0.8/-2.8 bit ENOB) compared to [3], [5], [7].

The measured results confirm that the performance of the DAFE are suitable to DC-coupled sensor interfaces for next-generation microscale biosensing and energy-autonomous IoT nodes.

REFERENCES