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A 0.01mm^2, 0.4V-V_{DD}, 4.5nW-Power DC-Coupled Digital Acquisition Front-End Based on Time-Multiplexed Digital Differential Amplification

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***Abstract*—A reconfigurable, high-impedance, DC-coupled low-frequency digital acquisition front-end (DAFE) suitable to operate under a power supply voltage ranging from 0.2 to 1V down to 600 pW power is presented in this paper. Matching-indifferent DC accuracy over a rail-to-rail input range is uniquely achieved by the new time-multiplexed digital differential amplification technique at ultra-low area and without chopping and auto-zeroing. A 180 nm testchip of the proposed DAFE occupies 0.00945 mm^2 and draws 4.5 nW at a 0.4 V supply, has a 120 Hz gain-bandwidth product, with an in-band input noise of 11.3 $\mu\mathrm{V_{rms}}$, a 137 μV input offset voltage standard deviation, 65.7 dB CMRR, 63.8 dB PSRR, and provides a 46.5 dB-SFDR, 6.9 bit-ENOB digitized output at -12 dBFS.**

***Index Terms*—DC-coupled digital acquisition front-end (DAFE), time-multiplexed digital differential amplification (TMD^{2}A), CMOS, ECG, IoT.**

I. Introduction

Ultra-compact, energy-quality scalable sensor interfaces operating from a low, extremely variable supply under a $< 10\,\mathrm{nW}$ power budget are required to enable next-generation sub-millimeter remotely-powered implantable biosensors [1] and energy-autonomous IoT nodes [2]. In this scenario, AC-coupled acquisition front-ends (AFEs) with $< 10\,\mathrm{nW}$ power [3], [4], [5] and 0.01-mm^2-scale area [6], [7] have been demonstrated for ECG, EEG and audio signal acquisition.

DC-coupled AFEs, needed e.g. in electrochemical and temperature sensors acquisition, pose further challenges, and DC accuracy (i.e. low DC offset/drifts, high DC CMRR and PSRR) is achieved by chopping [8], [6] and/or auto-zeroing [9], at the cost of much increased power, area and lower input impedance.

In this paper, a scalable, DC-coupled, biosignal digital AFE (DAFE) with inherent DC offset and drift suppression and direct digitization is demonstrated in 180nm CMOS aiming to simultaneously achieve order-of-nanowatt power, area-efficiency and decent DC accuracy over a wide supply range.

II. Time-Multiplexed Digital Differential Amplification (TMD^{2}A)

The proposed DAFE entails inherently offset- and drift-free, differential-mode amplification without relying on matching, chopping or auto-zeroing, thanks to the new time-multiplexed digital differential amplification (TMD^{2}A) approach illustrated in Fig.1. Here, the same single-ended comparator is multiplexed in time to compare the non-inverting (v^+) and the inverting (v^-) differential analog inputs against the same threshold (assumed to be 0 V in the following), and differential-mode signal amplification is achieved as in a Digital-Based Amplifier (DB-Amp) [10].

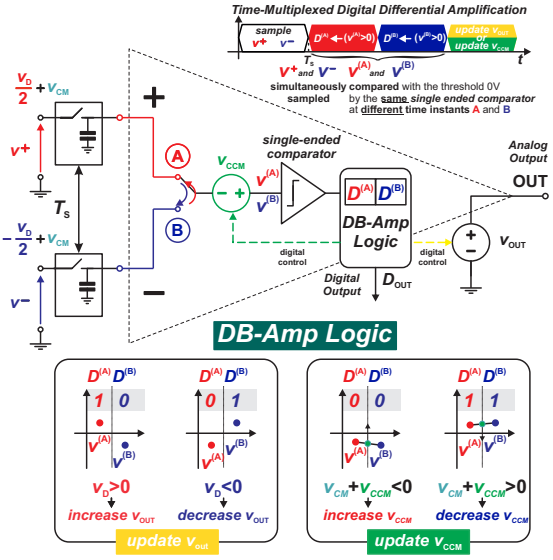


Fig. 1. Concept diagram of the Time-Multiplexed Digital Differential Amplification principle.

In details, after v^+ and v^- are simultaneously sampled, the switch in Fig.1 is operated in A, so that v^+ is in series to the common-mode (CM) compensating floating voltage source (CM-FVS) v_{CCM}, and the input voltage

$$v^{(\mathrm{A})} = v^+ + v_{\mathrm{CCM}} = \frac{v_{\mathrm{D}}}{2} + v_{\mathrm{CM}} + v_{\mathrm{CCM}}$$

is applied to the comparator. The comparator digital output is 1 if $v^{(\mathrm{A})} > 0$ and 0 otherwise, and is stored in $D^{(\mathrm{A})}$. Then,

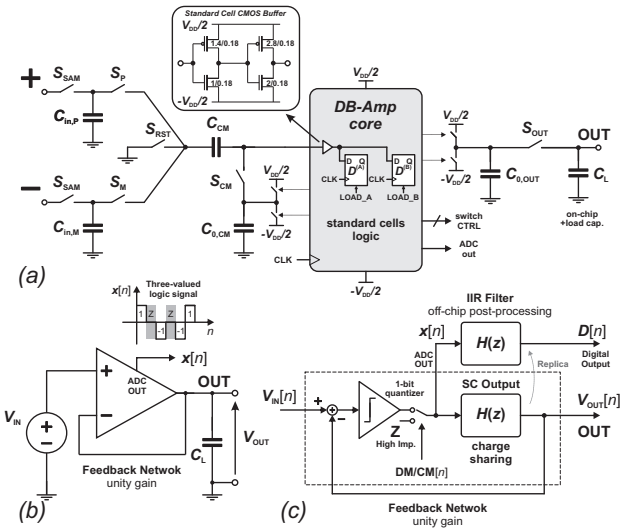


Fig. 2. Proposed SC TMD^{2}A DAFE: (a) schematic, (b) unity-gain configuration considered for input signal digitization, (c) equivalent block diagram of the configuration in (b).

the switch is operated in B, the comparator input is

$$v^{(\mathrm{B})} = v^- + v_{\mathrm{CCM}} = -\frac{v_{\mathrm{D}}}{2} + v_{\mathrm{CM}} + v_{\mathrm{CCM}}$$

and the corresponding comparator output is stored in $D^{(\mathrm{B})}$.

Based on $D^{(\mathrm{A})}$ and $D^{(\mathrm{B})}$, either v_{OUT} or v_{CCM} are updated as in a DB-Amp [10], i.e. if $(D^{(\mathrm{A})}, D^{(\mathrm{B})}) = (1,0)$ ($(D^{(\mathrm{A})}, D^{(\mathrm{B})}) = (0,1)$), which implies that $v_{\mathrm{D}} > 0$ ($v_{\mathrm{D}} < 0$), v_{OUT} is increased (decreased) by a minimum step, and v_{CCM} is kept unchanged. On the contrary, if $(D^{(\mathrm{A})}, D^{(\mathrm{B})}) = (1,1)$ ($(D^{(\mathrm{A})}, D^{(\mathrm{B})}) = (0,0)$), v_{CCM} is decreased (increased) by a minimum step so that to track v_{CM}, aiming to enforce $|v_{\mathrm{CM}} + v_{\mathrm{CCM}}| < |v_{\mathrm{D}}/2|$, as required to detect the sign of v_{D} in the next cycles, while v_{OUT} is hold.

A. Transistor-Level Design

In the proposed DAFE, TMD^{2}A is realized in 180nm CMOS by switched capacitor (SC) techniques [see schematic in Fig. 2(a)]. A small standard cell CMOS digital buffer [transistor level details in Fig. 2(a)] is used as a single-ended comparator, while the input sampling capacitors, the CM-FVS and the output voltage source are implemented by pF-range Metal-insulator-Metal (MiM) capacitors, and the floating switches are designed by CMOS pass gates operated at boot-strapped voltage. The DB-Amp core is a finite state machine (FSM) automatically synthesized in standard-cell logic, whose state transition graph is shown in Fig. 3.

B. Circuit Operation

In state A (B), the input capacitor $C_{\mathrm{in,P}}$ ($C_{\mathrm{in,M}}$), charged at the non-inverting (inverting) input voltage v^+ (v^-) sampled at the previous cycle (see below), is connected in series to C_{CM} at the buffer input (Fig.4, states A-B in the left and right column) and its digital output is stored in the D-Flip Flop $D^{(\mathrm{A})}$ ($D^{(\mathrm{B})}$) at the next clock edge. Depending on $(D^{(\mathrm{A})}, D^{(\mathrm{B})})$, the FSM evolves to states C+/C-, to update the output voltage (left column in Fig.4), or to states E+/E-(right column in Fig.4), to update the voltage v_{CCM} across C_{CM}.

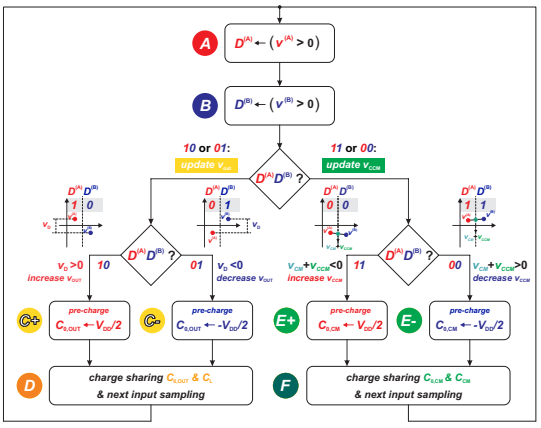


Fig. 3. State transition graph of the DB-Amp control unit.

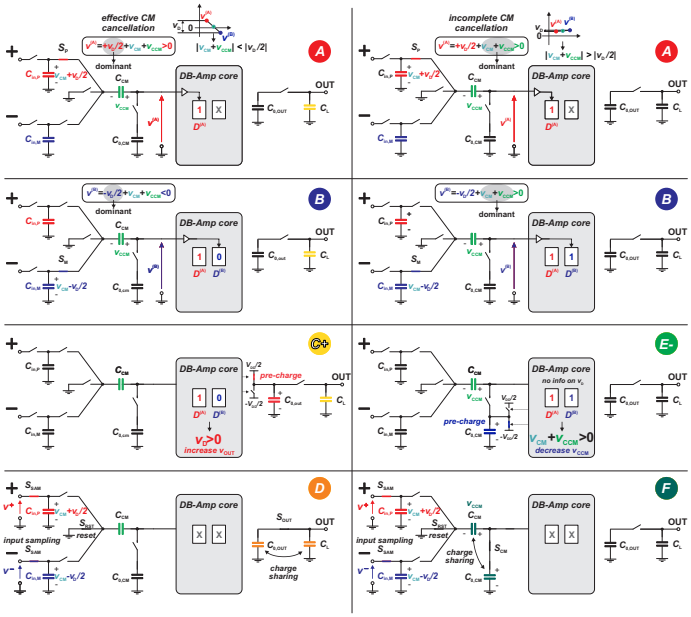


Fig. 4. Sequence of switch configurations corresponding to the states in Fig.3: for $|v_{\mathrm{CM}}+v_{\mathrm{CCM}}| < |v_{\mathrm{D}}/2|$, i.e. dominant differential component (left) and for $|v_{\mathrm{CM}}+v_{\mathrm{CCM}}| > |v_{\mathrm{D}}/2|$, i.e. dominant CM component (right).

In order to increase (decrease) the output voltage, the fF-range capacitor $C_{0,\mathrm{OUT}}$ is first pre-charged to $V_{\mathrm{DD}}/2$ ($-V_{\mathrm{DD}}/2$) in state C+ (C−), and then connected in parallel to C_{L} in state D, so that v_{OUT} is increased (decreased) by:

$$\Delta v_{\mathrm{OUT}} = \frac{C_{0,\mathrm{OUT}}}{C_{\mathrm{L}} + C_{0,\mathrm{OUT}}} \left(\overset{+}{(-)} \frac{V_{\mathrm{DD}}}{2} - v_{\mathrm{OUT}} \right).$$

In the same state D, v^+ and v^- are simultaneously sampled on $C_{\mathrm{in,P}}$ and $C_{\mathrm{in,M}}$. In a similar fashion, in E+ (E-), the fF-range capacitor $C_{0,\mathrm{CM}}$ is pre-charged to $V_{\mathrm{DD}}/2$ ($-V_{\mathrm{DD}}/2$) and then connected in parallel to C_{CM} in the next state F, to update v_{CCM} as demanded to compensate the CM input component, as well as drifts and process, voltage and temperature (PVT)-related variations in the CMOS buffer logic threshold. In the

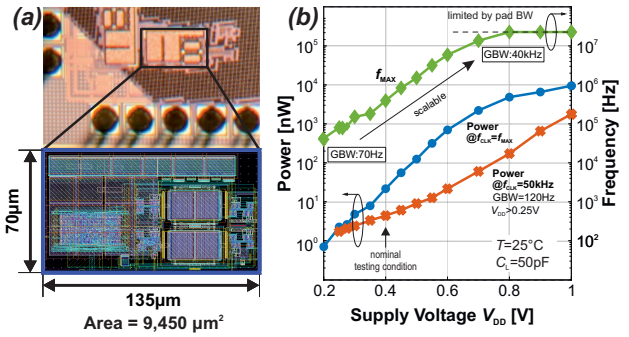


Fig. 5. Test chip micrograph (a) and (b) maximum clock frequency $f_{\max}$ and power ($@f_{\rm clk} = f_{\max}$ and $@f_{\rm clk} = 50\,$kHz) versus supply voltage $V_{\rm DD}$.

TABLE I
MEASURED DC PERFORMANCE OF SIX DICE AT 25° C, $V_{\rm DD} = 0.4\,$V

	Unit	#1	#2	#3	#4	#5	#6	μ	σ
Input Offset	μV	+83	+19	+54	+230	-20	-188	+30	137
DC Gain	dB	40.8	39.9	39.6	38.0	42.7	36.3	39.6	2.2
CMRR	dB	68.0	74.0	68.5	60.4	60.0	63.4	65.7	5.4
PSRR	dB	83.9	55.3	54.0	60.6	69.0	60.1	63.8	11.1

same state F, v^+ and v^- are also sampled, as in D. Either state D or state F conclude an operating cycle, and are followed by state A in the next cycle.

As in [10], [11], the circuit operates as an analog differential amplifier with a gain-bandwidth (GBW) product proportional to the clock frequency. When connected in negative feedback under fixed capacitive load [e.g. in the unity-gain configuration as in Fig. 2(b)], the circuit operates as a delta modulator [6], [7] [see Fig. 2(c)], and a digitized version of the output can be retrieved in post-processing from the sequence of the DB-Amp FSM states by infinite impulse response (IIR) digital filtering.

III. Experimental Results

A CMOS test-chip of the proposed DAFE has been fabricated in 180 nm and occupies merely $0.00945\,\text{mm}^2$ [micrograph in Fig. 5(a)]. When tested at 25°C in unity-gain feedback configuration [Fig. 2(b)] with $C_{\rm L} = 50$pF, the DAFE operates under a 0.2-1 V supply voltage range with a rail-to-rail input/output swing, at a maximum clock frequency $f_{\max}$ ranging from 28 kHz to 15 MHz (upper-limited by the analog pads), corresponding to a scalable GBW from 70 Hz to 40 kHz. From Fig.5b, the power consumption varies from 600 pW at 0.2 V to 9.58 μW at 1 V (from 2.0 nW at 0.25 V to 1.77 μW at 1 V) under $f_{\rm clk} = f_{\max}$ ($f_{\rm clk} = 50\,$kHz). At 0.4 V supply ($V_{\rm DD}$) and $f_{\rm clk} = 50\,$kHz, considered hereafter in the DAFE characterization, the power is 4.5 nW.

Based on the DC characterization at 25°C, 0.4 V $V_{\rm DD}$, $C_{\rm L} = 50$pF and $f_{\rm CLK} = 50\,$kHz (see Tab. I), the input offset voltage of six dice ranges from -188 to $+230\,\mu$V, the open-loop DC gain from 36.3 to 42.7 dB, the CMRR from 60.0 to 74.0 dB and the PSRR from 54.0 to 83.9 dB. These results prove the reasonable DC accuracy of the proposed DAFE. Moreover, the DC input resistance of all dice is above 1GΩ.

The time-domain analog output of sample #2 in unity-gain feedback [$v_{\rm OUT}$ in Fig. 2(b)] under 0.1 Hz, 360 $\text{mV}_{\text{pk-pk}}$ sine-wave input, and under a rail-to-rail square-wave input are shown in Figs. 6(a)-(b). The spectrum of the signal in Fig. 6(a) is shown in Fig. 6(c) and reveals a THD of 1.3%. Based on the open-loop frequency response reported in Fig. 6(c), the DC gain is 39.9 dB and the GBW is 120 Hz. The open-loop input-referred noise spectrum in Fig. 6(e) reveals an in-band noise power spectral density of $1.03\,\mu\text{V}/\sqrt{\text{Hz}}$ and an effective suppression of $1/f$ noise. The integrated input noise in the 0.05-1 Hz (0.05-120 Hz) bandwidth is $1.03\,\mu\text{V}_{\rm rms}$ ($11.3\,\mu\text{V}_{\rm rms}$).

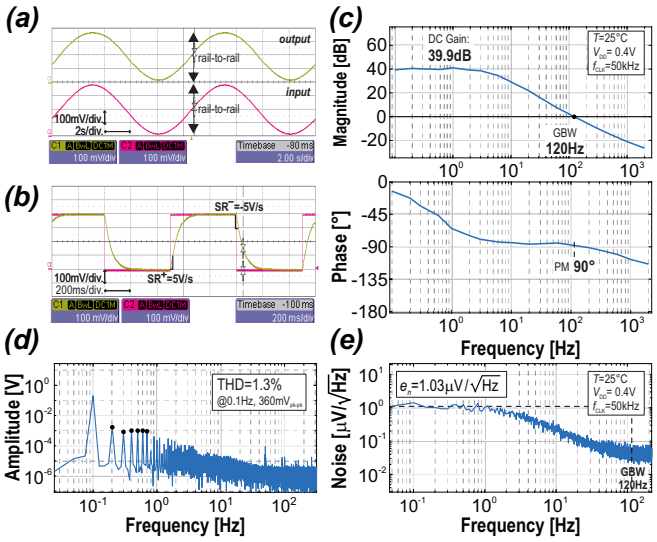


Fig. 6. Analog output testing: time-domain response in unity-gain closed-loop configuration for rail-to-rail sine (a) and square wave (b) input; (c) open-loop differential gain frequency response (magnitude and phase); (d) output voltage spectrum (test conditions as in (a)), (e) input noise spectrum (from output noise spectrum measured with $v^+ = v^- = 0$, considering 39.9 dB DC gain).

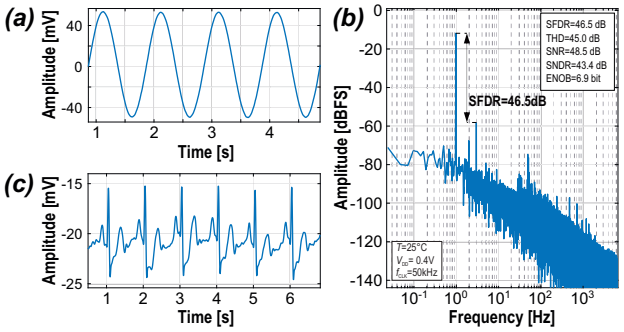


Fig. 7. ADC output testing: time-domain waveform reconstructed from the ADC output stream [Figs. 2(b)-(c)] under 1 Hz, 50 mV_{pk} (-12 dBFS) sine input (b) spectrum of the reconstructed output in (a) and ADC dynamic performance; (c) reconstructed ECG waveform (ECG-20 mV electrode offset).

In Figs. 7(a)-(b), the time-domain waveform and the spectrum of a 50 mV_{pk} (i.e. -12 dBFS), 1 Hz sine-wave reconstructed from the digital output stream of the DAFE post-processed off-chip by an IIR filter as in [6] is shown. The results reveal 46.5 dB SFDR, 45.0 dB THD and 43.4 dB SNDR, corresponding to 6.9 ENOB, and demonstrate the operation of the DAFE as an ADC. An ECG signal reconstructed from the digital output is shown in Fig. 7(c) and confirms the suitability of the DAFE to biosignal acquisition.

TABLE II
PERFOMANCE SUMMARY AND COMPARISON WITH LOW FREQUENCY SENSOR INTERFACES

Reference	Unit	[6]	[12]	[3]	[5]	[8]	[9]	[13]	[7]	**This Work**
Architecture		AFE	ATC	AFE	AFE	CCIA	Buffer	LNA	Δ-ADC	DAFE
Coupled		DC	DC	AC	AC	DC	DC	DC	DC	DC
Technology	nm	40	65	65	180	65	180	180	180	180
Area	mm^2	0.015	**0.006**	0.200	0.75	0.100	1.4	1	0.011	0.00945
Normalized Area	$10^6 \cdot \mathrm{F}^2$	9.37	1.42	47.3	23.1	23.7	43.2	30.9	0.65	**0.291**
Supply Voltage	V	0.6	0.5	0.6	1.2/0.6	1	1.8	0.2/0.8	0.6/1.2/3.3	**0.4**
Supply Range	V	N/A	N/A	0.5-0.7	N/A	N/A	N/A	N/A	N/A	**0.2-1**
Input Range	% V_{DD}	50	0.8	N/A	N/A	N/A	N/A	N/A	**91**	90
Power	nW	3,300	1,275	**3**	$8.3^{(e)}$	1,800	378,000	790	990	4.5
Bandwidth	Hz	150	11,000	1.5-370	470	0.5-100	**1,450,000**	670	500	$120^{(i)}$
Input Resistance	GΩ	0.05	$0.031^{(f)}$	N/A	N/A	$0.8^{(f)}$	***(g)***	$0.01^{(f)}$	2.96	> 1
DC Gain	dB	N/A	N/A	32	31-59	40	0	**57.8**	N/A	$39.6^{(i,k)}$
Input Offset	μV	N/A	N/A	N/A	N/A	1	**0.4**	N/A	N/A	$137^{(j)}$
In-band Noise (noise BW)	$\mu\mathrm{V}_{\mathrm{rms}}$ (Hz)	$20^{(c)}$ (1-150)	3.8	26 (1.5-370)	17	$6.7^{(d)}$ (0.5-100)	N/A	**0.94** 1-500	$2.6^{(c)}$	$11.3^{(c,h)}$ (0.05-120)
Noise PSD	$\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$	N/A	0.036	N/A	N/A	0.021	**0.02**	0.036	N/A	1.03
NEF$^{(a)}$		$147^{(c)}$	2.2	2.1	2	3.3	7.3	**1.6**	$3.5^{(c)}$	$4.1^{(c)}$
PEF$^{(b)}$		$13,012^{(c)}$	2.4	2.6	4.8	10.9	96	**2.1**	$15.2^{(c)}$	$6.7^{(c)}$
THD	%	1	**0.2**	N/A	N/A	1.5	N/A	N/A	N/A	$1.3^{(l)}$
CMRR	dB	60	60	60	N/A	**134**	N/A	85	> 78	$65.7^{(i)}$
PSRR	dB	N/A	N/A	63	N/A	120	**125**	80/75	N/A	$63.8^{(i)}$
SFDR	dB	56	**60**	N/A	N/A	N/A	N/A	N/A	N/A	46.5
ENOB	bit	N/A	N/A	9.2	7.7	N/A	N/A	N/A	**9.7**	6.9

$^{(a)}$ $NEF = V_{\mathrm{n,rms}}\sqrt{\frac{2I_{\mathrm{B}}}{4\pi kTV_{\mathrm{T}}\mathrm{BW}}}$, where $V_{\mathrm{n,rms}}$ is the rms input noise, I_{B} is the supply current and BW is the bandwidth; $^{(b)}$ $PEF = V_{\mathrm{DD}} \cdot NEF^2$; $^{(c)}$ includes ADC quantization noise (and ADC current for NEF/PEF), $^{(d)}$ with DC servo loop, $^{(e)}$ LNA+ADC power considered, $^{(f)}$ estimated. $^{(g)}$ <1pA total input current; $^{(h)}$ Input rms noise in the 0.05-120 Hz BW estimated from the measured open-loop input-referred noise spectral density e_n in Fig.6(e) as $e_n \cdot \sqrt{BW}$; $^{(i)}$Average of 6 samples; $^{(j)}$Std. Dev. of 6 samples; $^{(k)}$ Open-loop gain; $^{(l)}$ Under 0.1 Hz, 90% rail-to-rail input; Best in **bold**.

IV. COMPARISON AND CONCLUSIONS

Compared with the state of the art of low-frequency AFEs in Table II, the proposed DAFE occupies the lowest normalized area (2.2X less than [7]) and works at the minimum voltage and over the widest supply range (4X wider than [3]) with rail-to-rail input/output swing, uniquely offering power-quality scalability. At 0.4 V, the power is comparable with AC-coupled AFEs [3], [5] (1.5X more than [3], in 65 nm, and 1.8X less than [5], also in 180nm), which have 3.1X-3.9X larger bandwidth and 2.3X-1.5X more in-band rms noise.

Compared to DC-coupled AFEs with similar bandwidth [6]–[8], [13], the DAFE has an inherently high input resistance ($> 1\,\mathrm{G}\Omega$), consumes 1.2X-106X less area and 175X-733X less power, while providing a digitized output as [6], [7]. The offset, although 137X-342X larger than [8], [9], is the only reported in sub-μW AFEs. The in-band rms noise is 1.8X less than [6] and 4X more than [7], which inherently include quantization noise as the DAFE, while it is 12X more than the best [13]. The noise efficiency factor (NEF)/power efficiency factor (PEF) metrics, defined in Table II, are 1.2X worse/2.3X better than [7] and 36X/1,942X better than [6], while they are 2.6X/3.2X worse than [13], the best in Table II. The digitized output of the DAFE is slightly worse in terms of effective resolution (-0.8/-2.8 bit ENOB) compared to [3], [5], [7].

The measured results confirm that the performance of the DAFE are suitable to DC-coupled sensor interfaces for next-generation microscale biosensing and energy-autonomous IoT nodes.

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