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Direct Digital Sensing Potentiostat targeting Body-Dust / Rubino, R., Carrara, S., Crovetti, P.. - ELETTRONICO. - (2022). (2022 IEEE Biomedical Circuits and Systems Conference (BioCAS2022) Taipei (Taiwan) 13-15 October 2022) [10.1109/BioCAS54905.2022.9948649].

Availability:
This version is available at: 11583/2972538 since: 2022-10-23T09:00:17Z

Publisher:
IEEE

Published
DOI:10.1109/BioCAS54905.2022.9948649

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13 October 2026

Direct Digital Sensing Potentiostat targeting Body-Dust

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***Abstract*—In this paper, an innovative Direct Digital Sensing Potentiostat integrated circuit for enzymeless blood glucose sensing and direct digitization is proposed to address the requirements of Body Dust. The circuit occupies a silicon area of 460 μm^2 in 180nm CMOS and operates down to 0.4 V power supply voltage with 4.7 nW power consumption. The functionality of the proposed circuit and its performance under typical conditions and under process and temperature variations is tested by post-layout simulations.**

***Index Terms*—Body Dust, potentiostat, glucose sensing, Digital-Based Amplifier (DB-Amp)**

I. Introduction

The concept of Body Dust (BD) [1] envisions the integration of micrometer-scale sensors embedded in bio-compatible, wirelessly powered CMOS integrated circuits (ICs), with a size comparable to human blood cells ($< 100\mu m$ diameter), small enough to ubiquitously circulate in tissues and blood as swarms of particles and able to exchange data from within the human body to the outside world for diagnosis and health-monitoring purposes.

Turning BD into reality demands analog CMOS ICs with micrometer-scale dimensions and nanowatt power [1], which are hard to be designed by traditional techniques. In this context, digital-based analog design, which has recently been proposed to address the requirements of Internet of Things (IoT) applications [3], [4], is more and more emerging as a viable option to meet the area and power requirements of BD applications. Even though quasi-digital potentiostats have been proposed in [2], fully digital potentiostats have never been presented so far. In this paper, a Direct Digital Sensing Potentiostat (DDSP) for the enzymeless detection of species in a physiological solution is presented, aiming to glucose detection within the framework of the Body Dust research.

The paper is structured as follows: in Section II, a model of the micrometer-scale electrode interface for the enzymeless glucose detection is devised, extrapolating electrode parameters from literature-derived measured characterizations. In Section III, the DDSP electronic architecture is presented, and its working principle is explained, focusing on its direct digital acquisition capability. Section IV follows, in which the performance of the DDSP is tested by post-layout simulations, both under nominal conditions and in the presence of process and temperature variations, and compared with the state-of-the-art. Some conclusions are finally drawn in Section V.

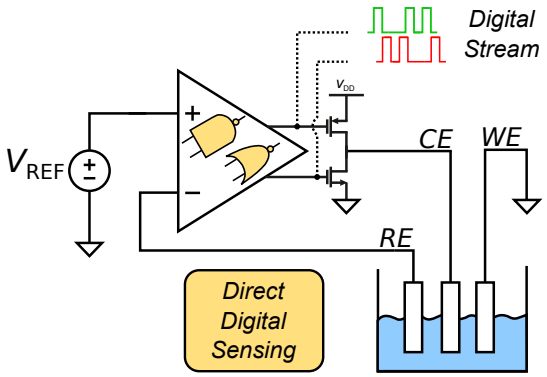

Fig. 1. Direct Digital sensing Potentiostat.

II. Electrochemical sensor

The Direct Digital Sensing Potentiostat (DDSP) performs non-enzymatic glucose detection employing a potentiostat-based current sensing topology, as in Fig.1, fixing the potential of the solution at the reference (RE) electrode while measuring the reduction or oxidation current flowing between the counter (CE) and working (WE) electrodes. The chronoamperometric (CA) method is considered from now on.

A. Sensor design and modeling

To electrically simulate the sensing architecture, a model of the electrochemical interface is developed. A square WE with platinum-nanospheres nanostructures as in [5] is considered, having a sensitivity

$$S_0 = 4\mu A/(mM \cdot cm^2) \tag{1}$$

in enzymeless detection of glucose [6].

The WE geometry is chosen to be $45\mu m$-side platinum square as in Fig.2a, suitable to BD particles in the order of $100\mu m$ lateral size. The sensitivity of the WE faradaic current with respect to glucose concentration, denormalised with respect to the electrode area is, from (1)

$$S = \frac{4\mu A}{cm^2 \cdot mM} \cdot (0.0045cm)^2 = 0.081 \frac{nA}{mM}. \tag{2}$$

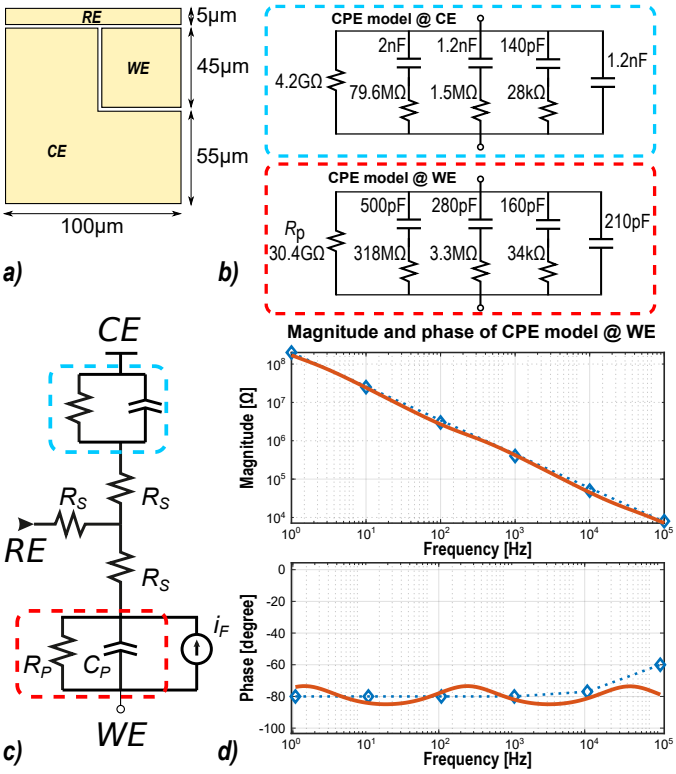

Fig. 2. Considered electrodes geometry (a), WE and CE electrical CPE model (b), high-level electrical model of the sensor (c), magnitude and phase of the CPE impedance at the WE (d).

Taking into account the usual glucose physiological range being in between 3mM and 8mM, a full-range current of 0.8nA (up to 10mM) is expected.

Along with the faradaic current, which is conveniently modelled by a concentration-driven current generator (i_F at the WE) the Randles circuit model of each electrode is extracted as in Fig.2c, including the solution resistance R_S, a constant phase element (CPE) and the charge transfer resistance R_P. Focusing of preliminary *in vitro* testing, the value of R_S is set considering the conductivity of a commercially available $0.01\,\text{M}$ phosphate buffer saline (PBS) solution, being $\sigma_\text{PBS} = 12\,\text{mS}/\text{cm}$.

A cubic volume of solution of $45\mu\text{m}$ side has been considered to estimate the solution resistance. The value of R_S is thus derived:

$$R_\text{S} = \left(\sigma_\text{PBS} \cdot \frac{A}{d}\right)^{-1} \simeq 18.5\,\text{k}\Omega \qquad (3)$$

where $A = (45\,\mu\text{m})^2$ and $d = 45\,\mu\text{m}$. The charge transfer resistance R_P and the CPE C_P electrical models (highlighted in dashed boxes in Fig.2c) for the WE and CE are extrapolated from the magnitude and phase impedance characterization of platinum electrodes reported in [7].

The reference magnitude and phase curves chosen to model the WE (blue diamonds curve in Fig.2d) are fit with the parallel RC model in Fig.2d, according to the algorithm

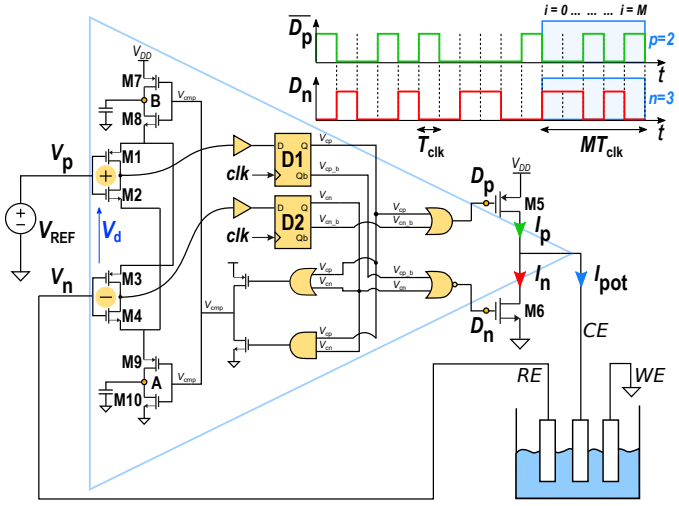

Fig. 3. Proposed digital-based potentiostat schematic and digital acquisition pulses.

presented in [8], resulting in the WE model in Fig.2b (dashed red box).

An analogous procedure is employed to model the CE, resulting in the RC model in Fig.2b (dashed blue box) while just the solution resistance is considered for the RE, being its current negligible thanks to the potentiostat high input impedance.

III. Direct Digital Sensing Potentiostat

The proposed DDSP takes advantage of the digital-based amplifier (DB-Amp) principe [3], [9], [10] for potentiostat readout, as schematically depicted in Fig.1. The schematic of the DB-Amp adopted in this work is reported in Fig.3. Compared to [10] and [3], [9], where a resistive summing network, and a Muller C element are used for the input common-mode (CM) compensation, floating inverters [11] are employed in the input stage of the DB-Amp proposed in this work to further enhance energy efficiency.

The non-inverting (v_p) and inverting (v_n) analog input signals of the DB-Amp in the DDSP, to be connected to V_REF and to the RE, respectively, are applied to the inputs of the CMOS floating inverters M1-M2 and M3-M4, which do not draw any DC current. The digital outputs of such inverters are sampled by the D Flip-Flops D1 and D2, respectively, on the active clock edge.

As in [10], when D1=0 and D2=1 (D1=1 and D2=0), which implies that $v_\text{d} = v_\text{p} - v_\text{n} > 0$ ($v_\text{d} \leq 0$), the output stage M5-M6 is operated to increase (decrease) the output voltage, i.e. the pMOS device M5 (the nMOS device M6) is turned on for one clock cycle T_clk, thus sourcing (sinking) a nearly constant current I_P (I_N) in the CE capacitance, corresponding to a positive (negative) charge packet $I_\text{P}T_\text{clk}$ ($I_\text{N}T_\text{clk}$).

When D1 and D2 have the same logical value, the sign of v_d cannot be detected and the output stage M5-M6 is kept in high impedance. Moreover, when D1=0 and D2=0 (D1=1 and D2=1) the negative (positive) supply of the input inverters is

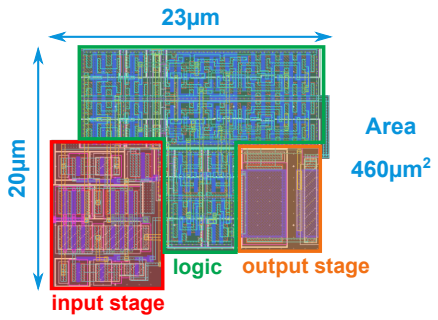

Fig. 4. Layout view of the DDSP.

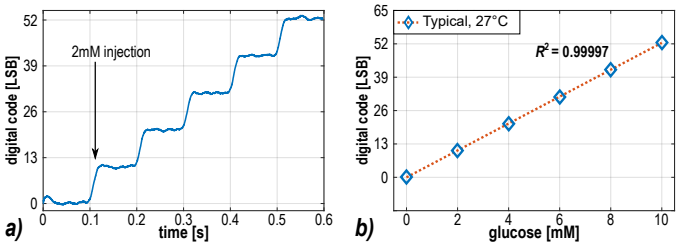

Fig. 5. Digital acquisition under staircase concentration increase of 2mM (a) and the corresponding calibration curve (b).

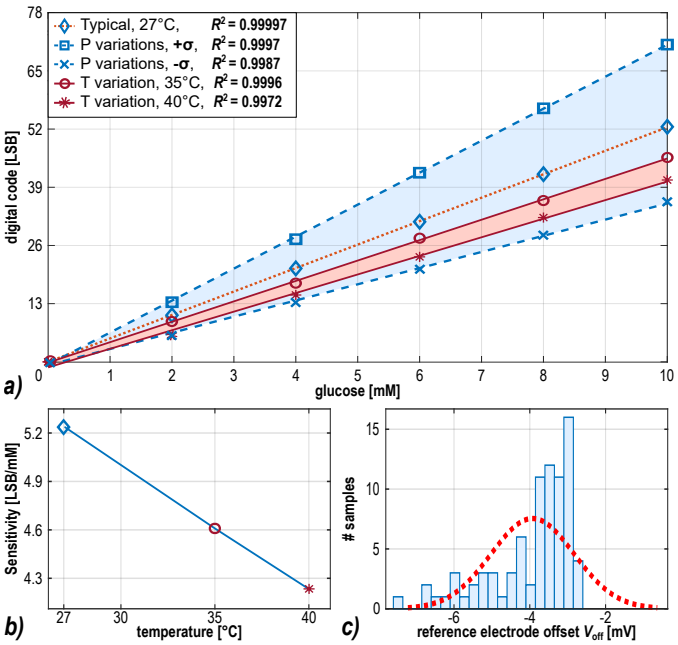

Fig. 6. Calibration curve spread against process ($\pm\sigma$) and temperature (35°C to 40°C) variations(a), sensitivity variation with temperature (b) and reference electrode offset variation with mismatch (c).

tied by M9 to node A (by M8 to node B), which was pre-discharged to 0 V via M10 (pre-charged to $V_{\rm DD}$ via M7) in the previous cycle. Such reconfiguration provides the input inverters with a dynamic bias, as required to asymmetrically discharge (charge) their output and to detect the sign of $v_{\rm d}$, resulting in D1=0 and D2=1 or D1=0 and D2=1 in the next cycle(s).

Thanks to negative feedback and to the filtering effect of the CE capacitance, the RE potential is forced by the DB-Amp to the non-inverting input voltage $V_{\rm REF}$ (ripple below 2.3mV rms) by injecting discrete charge packets in the CE. Since the charge in each packet is nearly constant, the time average of the CE current $I_{\rm pot}$, which turns out to be equal to the faradaic current $I_{\rm F}$, is directly estimated counting the number of the positive (negative) digital pulses p (n) over the last M clock cycles as follows:

$$I_{\rm F} = \frac{pI_{\rm P} - nI_{\rm N}}{M} \tag{4}$$

Based on (4), a digitized version of $I_{\rm F}$ is directly obtained post-processing the digital streams $D_{\rm p}$ and $D_{\rm n}$ driving the gates of M5 and M6 in Fig.3, thus suppressing the analog to digital converter (ADC) which is needed in conventional implementations.

IV. Post-Layout Simulations and Comparison

The proposed DDSP has been designed in 180nm CMOS and tested by post-layout simulations, performed connecting the DDSP to the electrochemical cell equivalent circuit described in Sec.II, fixing the WE potential at $-V_{\rm REF} = -0.2\,{\rm V}$, which corresponds to the first oxidation peak of the glucose in [5].

The layout of the DDSP cell, reported in Fig.4, occupies merely $460\,\mu{\rm m}^2$. Based on post-layout simulations at 27°C under 0.4 V supply, 50 kHz clock, and typical process conditions, the power consumption of the DDSP is 4.7 nW, the input current ranges from -22 nA to +33 nA, and the total input-referred noise, averaging DDSP binary streams over $M = 3,600$ clock cycles, is $65\,{\rm pA_{rms}}$ including quantization noise, resulting in a 58 dB dynamic range.

The simulated chronoamperogram and digital code/concentration curve under a staircase glucose concentration increase of 2 mM steps are reported in Fig.5a and Fig.5b respectively, and reveal a sensitivity of 5.2 LSB/mM and a high linearity $R^2 = 0.99997$.

Based on Monte Carlo simulations under process variations, the standard deviation of the DDSP sensitivity is $\sigma = 1.8\,{\rm LSB/mM}$, as shown in Fig.6a. The digital code/concentration curves of simulated samples at $\pm\sigma$ sensitivity reported in Fig.6a reveal a linearity degradation from $R^2 = 0.99997$ to $R^2 = 0.9987$. The simulated sensitivity versus temperature is reported in Fig.6b in the range 27°C-40°C and the simulated calibration curves at the extreme temperatures are shown in Fig.6a. A worst-case linearity degradation from $R^2 = 0.99997$ to $R^2 = 0.9972$ is observed at 40°C with respect to 27°C. These results reveal how process and temperature variations can be effectively compensated by linear calibration.

The distribution of the RE potential offset due to device mismatch has been obtained by Monte Carlo simulations and is reported in Fig.6c. The offset mean value and standard deviations are $V_{\rm off} = 3.9\,{\rm mV}$ and $\sigma_{V_{\rm off}} = 1.1\,{\rm mV}$, respectively.

Compared to potentiostat front-ends proposed over the last

TABLE I
POTENTIOSTAT PERFORMANCE COMPARISON

	Units	[12]	[13]	[14]	[15]	[16]	This Work
Method	-	CV,CA,EIS†	CA,CV	CA,CV	CA,CV	CA,CV	CA
Measured	-	yes	yes	yes	yes	yes	no
Current Range	μA	± 0.2	± 5	± 15	$\{-7, +10\}$	± 1.5	$\{-0.022, +0.033\}$
Dyn. Range	dB	104	108	73	58	105	58
Linearity	R^2	-	0.998	-	0.999	0.9990	0.99997
Current Noise	pA (rms)	7.76	41	-	25000	-	65
Bandwidth	Hz	10,000	-	200	50,000	1	7⋆
Technology	nm	180	180	180	180	65	180
Area	mm^2	0.208	0.78	2.25	3.17	0.07	0.00046
Supply	V	1.8	> 1.1	1.8	1.2	1.2	0.4
Power	μW	311.4	16	73.9	19	25	0.0047
Digital out	-	no	yes	yes	yes	yes	yes

†EIS: electrochemical impedance spectroscopy.
⋆ Limited by M, traded with noise.

years for chronoamperometry and cyclic voltammetry, whose performance is summed up in Tab.I, the proposed DDSP operates at the lowest supply voltage (3× less than [15] and [16]) while dissipating the smallest power (3,400× less than [13]) at the smallest area (150× less than [16], which is though fabricated in a more scaled technology).

The DDSP reports the best linearity $R^2 = 0.99997$, with an rms current noise of $65\,\mathrm{pA_{rms}}$ (more than the $41\,\mathrm{pA_{rms}}$ of [13]) while showing a smaller dynamic range of $58\,\mathrm{dB}$ (comparable to [15]).

These results are establishing the DDSP as a promising solution for Body Dust applications, thanks to its ultra low power and area, low supply voltage and robustness against process, temperature and mismatch variations.

V. CONCLUSION

In this paper, an original fully digital potentiostat designed in 180nm CMOS technology has been presented as an acquisition front-end for chronoamperometric electrochemical detection of glucose.

Based on post-layout simulations, the digital potentiostat operates down to $0.4\,\mathrm{V}$ power supply voltage (3× less than [15] and [16]) having $58\,\mathrm{dB}$ dynamic range, with a significant advantage in terms of power ($4.7\,\mathrm{nW}$, 3,400× less than [13]) and area ($460\,\mu\mathrm{m}^2$, 150× less than [16]) compared to recent alternatives, thus meeting the requirements of Body Dust applications.

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