Abstract

Design of transmitters with the main building block of power amplifier (PA) has a significant effect on the wireless mobile network. Therefore, high-efficiency PAs to increase the lifetime, and high integration using silicon-based technologies for the low size and cost are getting into account. High power is another requirement for PA design, which needs to adopt technologies with high breakdown voltage. This major part of this thesis is based on analyzing and designing power amplifiers for mobile broadband networks to address the above challenges and limitations and is divided into two main parts. The first part performs the implementation of the hybrid transistor level power amplifier for 5G applications. In order to achieve high power and high-efficiency performance especially at the 6 dB power back-off, Doherty power amplifiers are designed, simulated, and measured. Broadband techniques, as well as the class J operation mode, are applied to improve the bandwidth. Designed PAs employ packaged 10 W GaN transistor from Cree for the S-band operation.

The second architecture is a Watt-level high linearity power amplifier using Silicon-based technology. The aim of this implementation is to design and analysis a high power power amplifier at millimeter wave (mm-wave) frequencies, with a center frequency of 28 GHz for 5G application. Moreover, in other to have low loss in the output stage, a waveguide power combiner is adopted. This power amplifier is taped out using Qubic4 0.25 μm silicon-germanium (SiGe) bipolar complementary metal oxide semiconductor (BiCMOS) technology from NXP Semiconductor and performs output power around 28 dBm at 28 GHz with high linearity.

Concerning the high-frequency digital field, the design of a digital interface in the monolithic microwave integrated circuits (MMICs) core-chip is presented in this thesis. Core-chip is the main block for beam-shaping in the phased array system, and consists of n-bits phase shifters, attenuators, and switches which are controlled by the serial-input parallel-output interface. However, the absence of complementary

devices and also limited metal layers in the compound technologies such as Gallium Arsenide (GaAs), make challenges to design this digital interface, especially when high yield and low power consumption are required. Therefore, the most suitable solutions for the key digital blocks will be reviewed and compared, and based on this approach, the best option for our goal which is low power consumption is defined and fabricated. In fact, this analysis paved the way for the design and realization of an ultra-low-power 18-bits serial to parallel converter for X-band core-chip in $0.25\,\mu m$ pHEMT GaAs WIN technology, fully working and exhibiting a record current consumption of 13 mA (0.72 mA/bit) at -3.3 V supply voltage. The power consumption and occupied area have been improved with a physical layout and resistive pull-ups.